TEXAS
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PERFORMANCE AND TESTING OF THE COLUTA ADC ASIC

for the ATLAS HL-LHC Liquid Argon Calorimeter Readout

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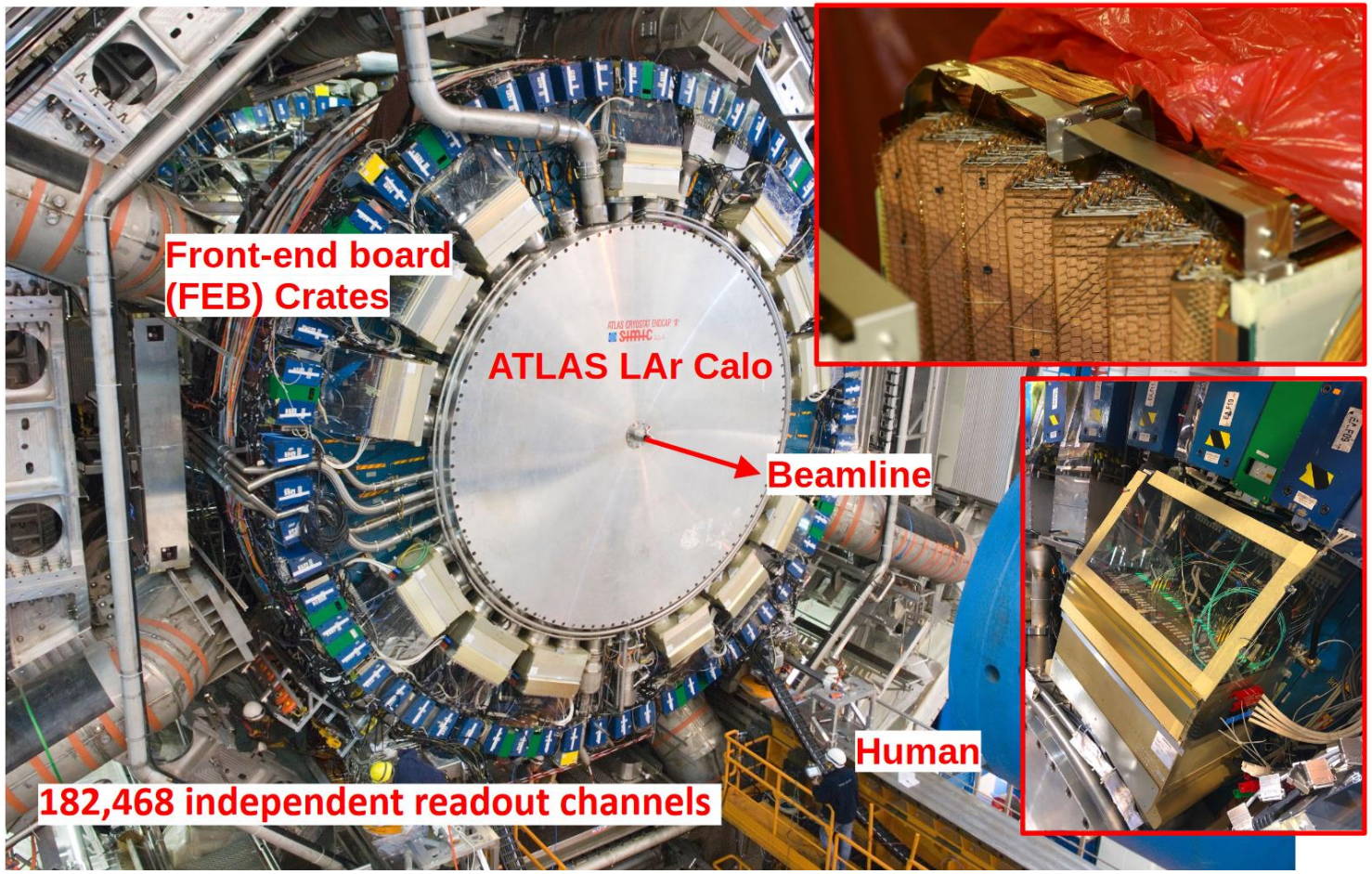
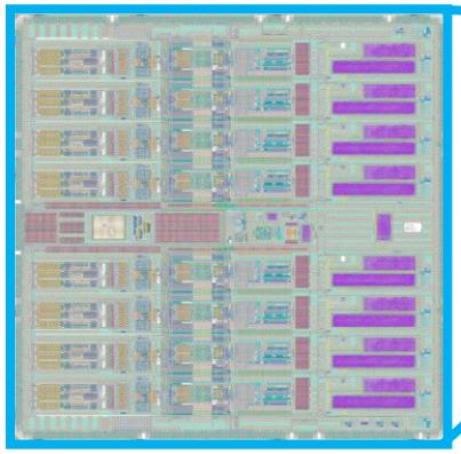
Outline and Context

- **COLUTAv4 ADC**
  - ATLAS HL-LHC Upgrade
- *Verification of:*
  - Radiation hardness
  - Precision Performance
- *Preliminary production QC testing results*

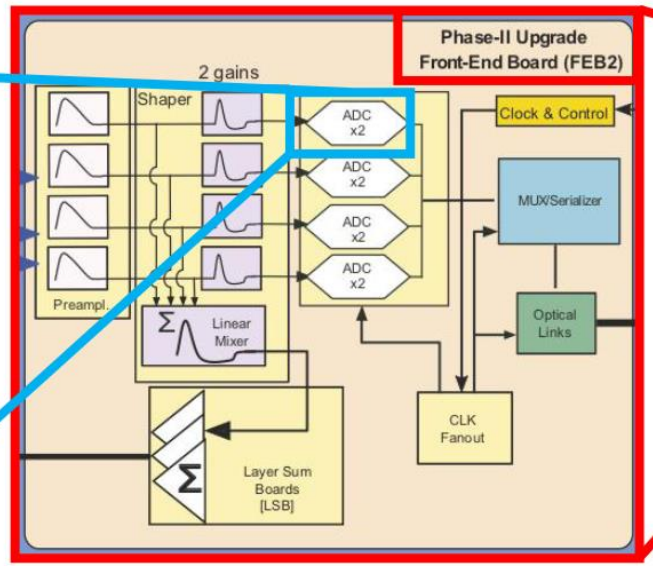


Upgrade: LAr Calorimeter Readout

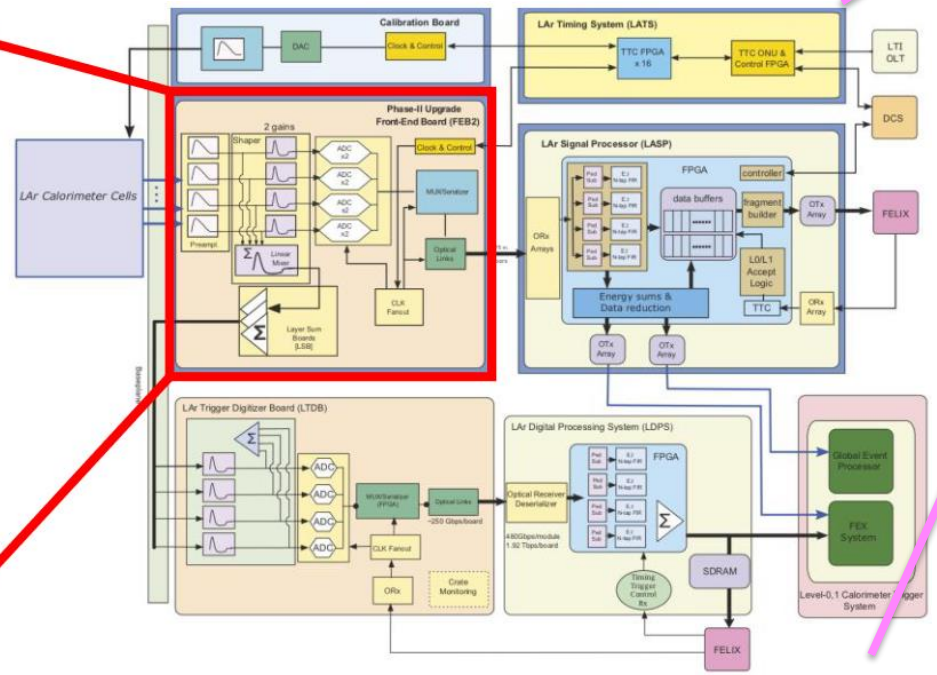
- Readout of the ATLAS LAr calorimeter at the HL-LHC will be provided by 1524 on-detector Front-End Board boards.
  - ATLAS trigger HL-LHC requirement: ≤1 MHz L1 trigger rate, 10 μS latency, radiation hardening.
- Original readout architecture cannot handle the full HL-LHC ATLAS trigger requirement.
- This talk will focus on the performance of the COLUTAv4 LAr ADC.



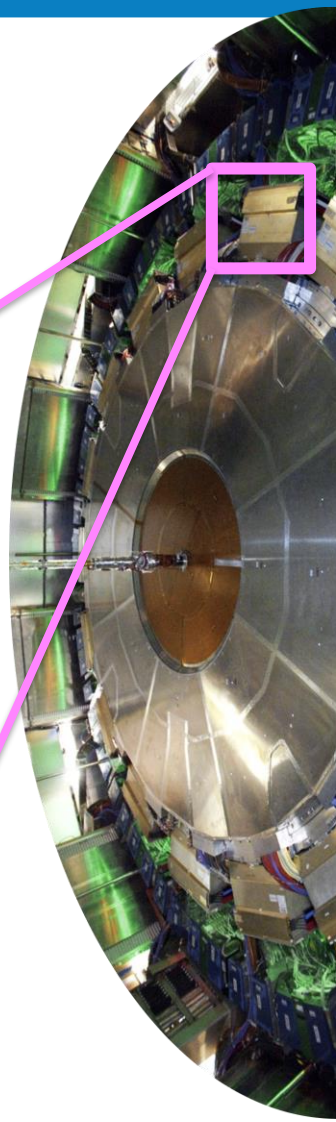
COLUTA ADC



Front-End Board 2 (FEB2)

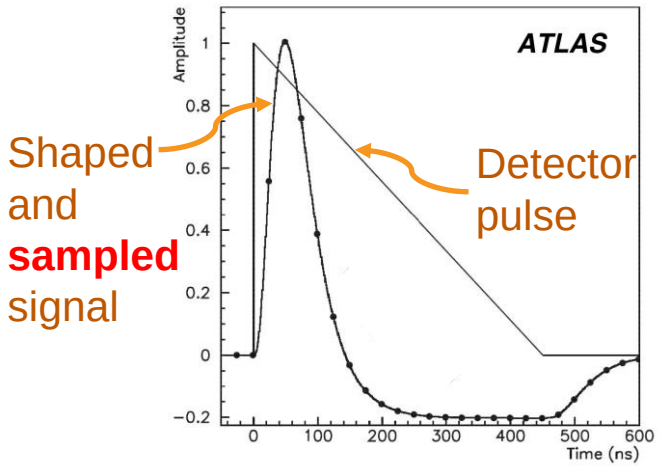


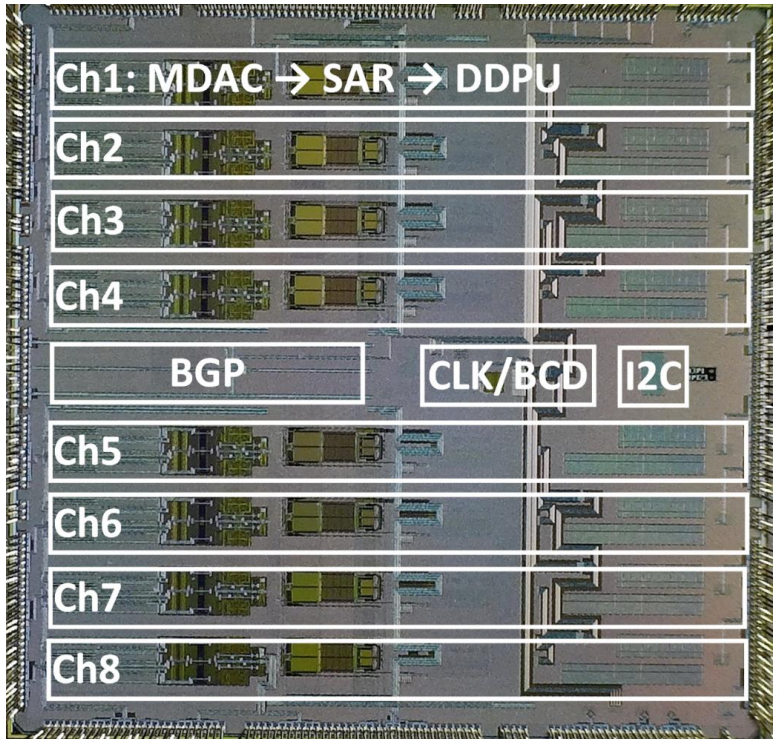
LAr Calorimeter Readout Architecture



COLUTAv4 ADC Overview

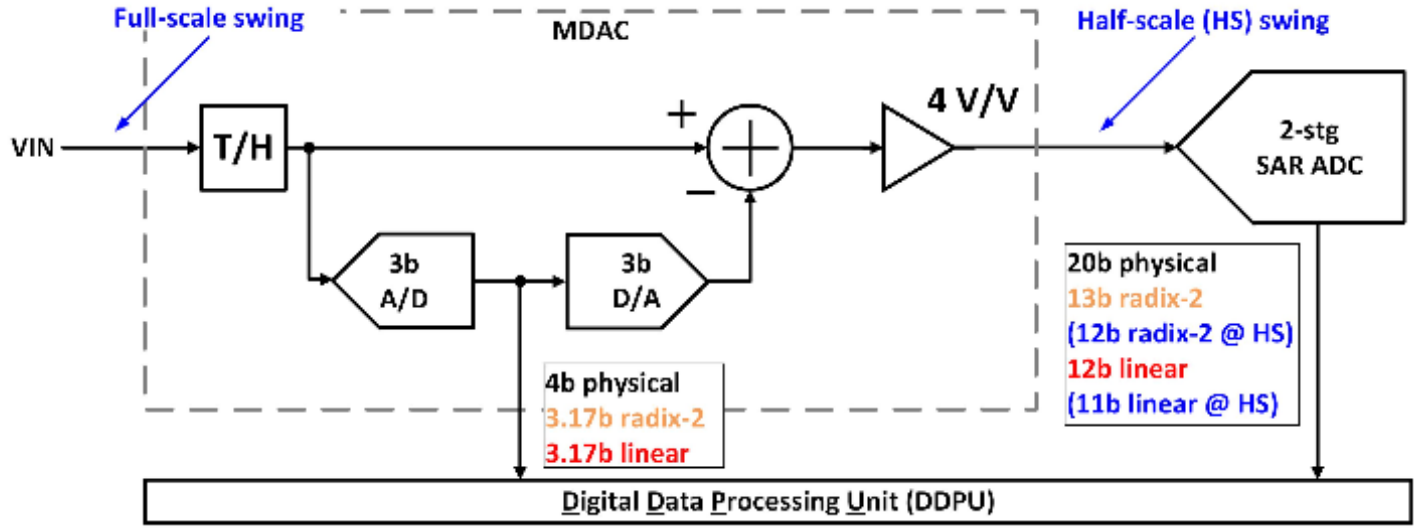
- Final prototype (4th iteration) of full custom COLUTA ADC ASIC.
- 8-channel, 15-bit, A/D converter.
  - 3.5-bit Multiplying DAC (MDAC) followed by 12-bit Successive Approximation Register (SAR).
  - Digital Data Processing Unit (DDPU) applies calibration bit weights and serially transmits data at 640 MBPS.
- Digitize at 40 MSPS.
- Fabricated in TSMC 65 nm CMOS.
  - 5.585 x 5.454 mm^2 chip die.
  - 4.3 million transistors.
  - 1.2V operation with 2 $V_{pk\text{-}pk}$ differential inputs.
- ≥14-bit dynamic range and >11-bit ENOB precision.
- Radiation tolerance design for HL-LHC.
- Packaged in Ball Grid Array.

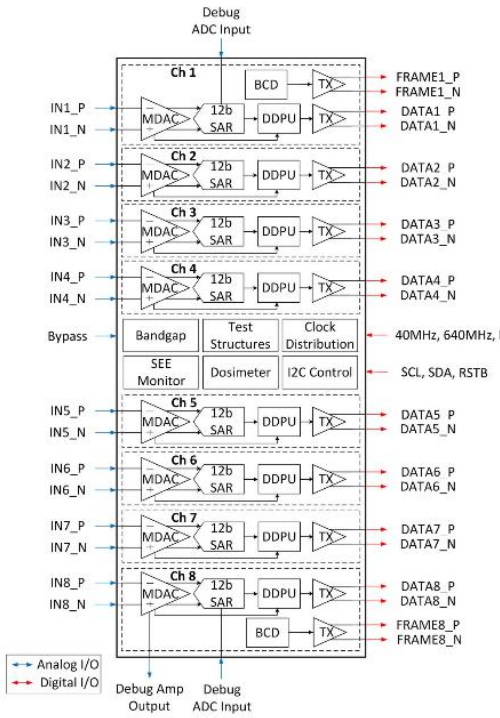


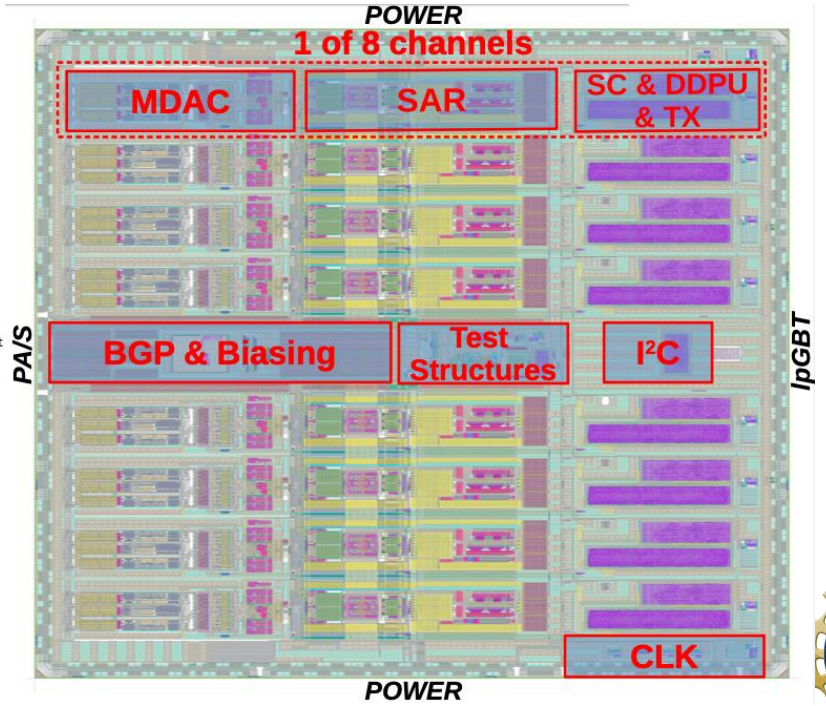


COLUTAv4 ADC Design

- Single channel architecture
  - 3.5-bit Multiplying DAC (MDAC) followed by 12-bit Successive Approximation Register (SAR).
  - ENOB and dynamic range specifications are met by using an MDAC to “extend” the dynamic range of a SAR ADC to 15-bits.
- Chip architecture
  - Eight independent and identical channels implemented.
  - Seamless interface between PA/S and lpGBT.
  - On-chip calibration circuit for MDAC and SAR

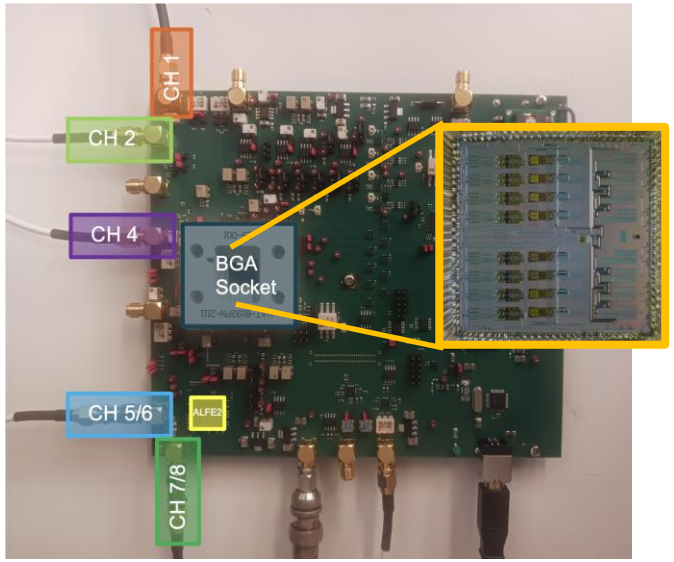


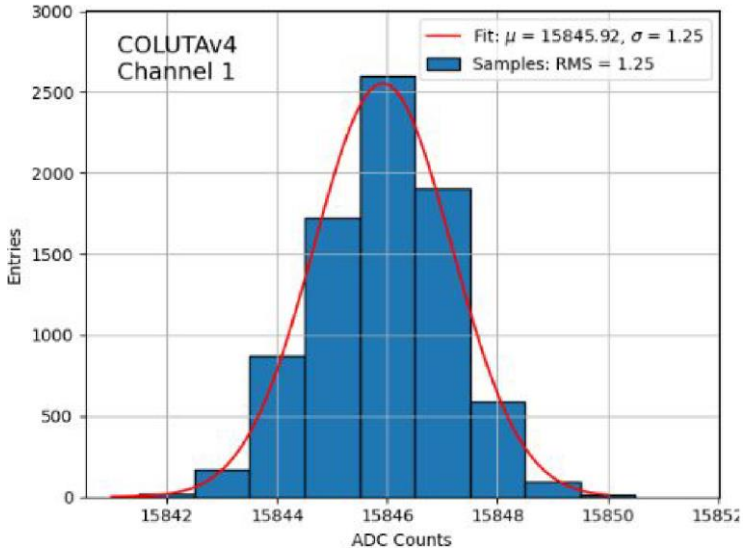


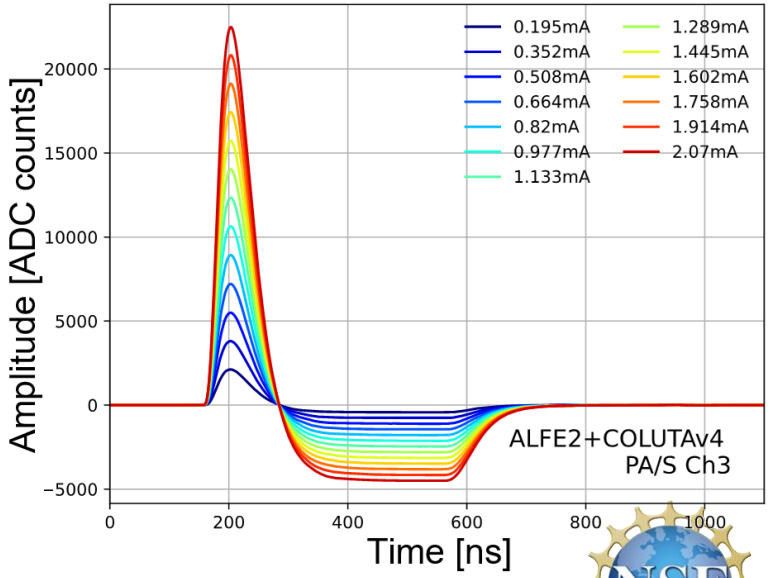


Precision Measurement Setup

- Socketed board used for QA/QC; soldered test boards used for precision analog tests.
  - Ch1,4: passive transformer input.
  - Ch2: commercial amplifier input.
  - Ch3: 16-bit DAC input.
  - Ch5,6,7,8: Pre-amp shaper (ALFE2) input.
- Feature-less pedestal; ~1.2 ADC counts RMS of noise out of 2^{15}.
  - CV4 meets dynamic range spec (*c.f.* ≥ 14 bits)
- For large pulses, achieve an energy resolution σ(E)/E < 0.25% and a time resolution < 100 ps

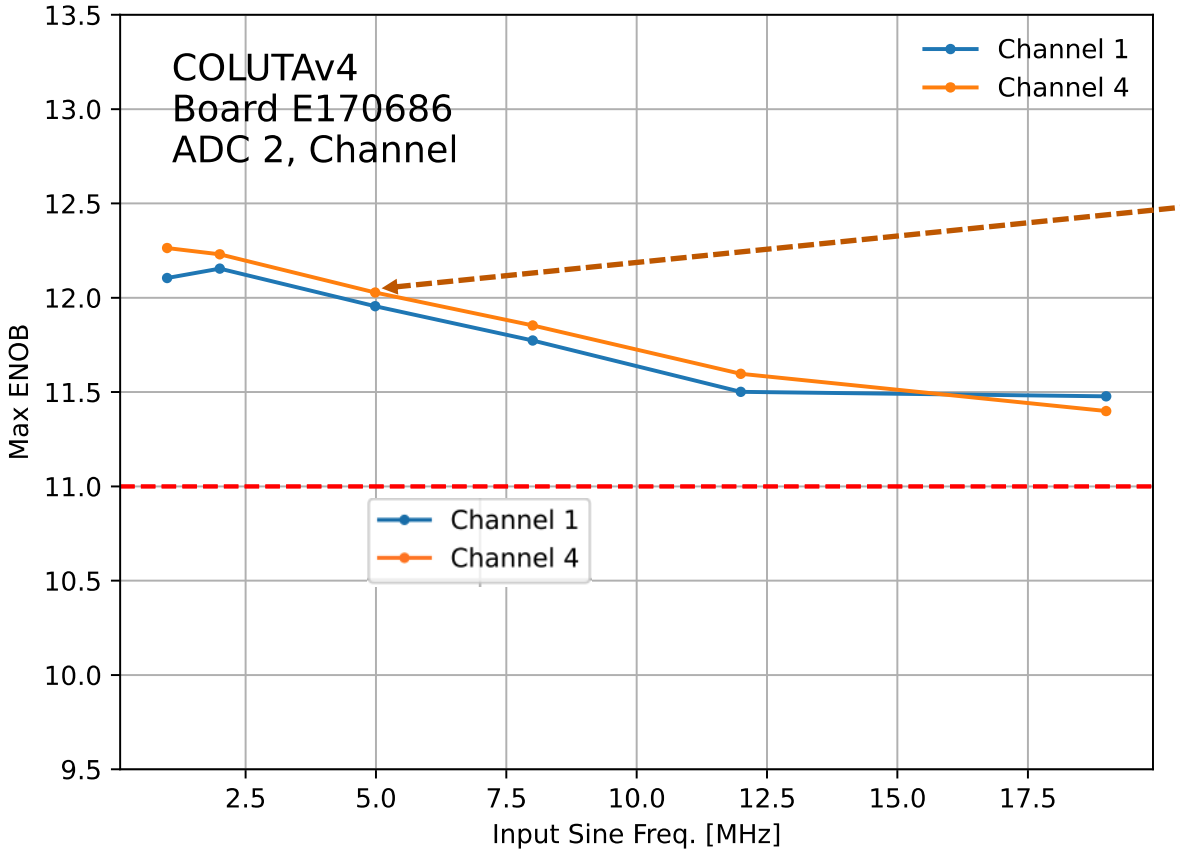


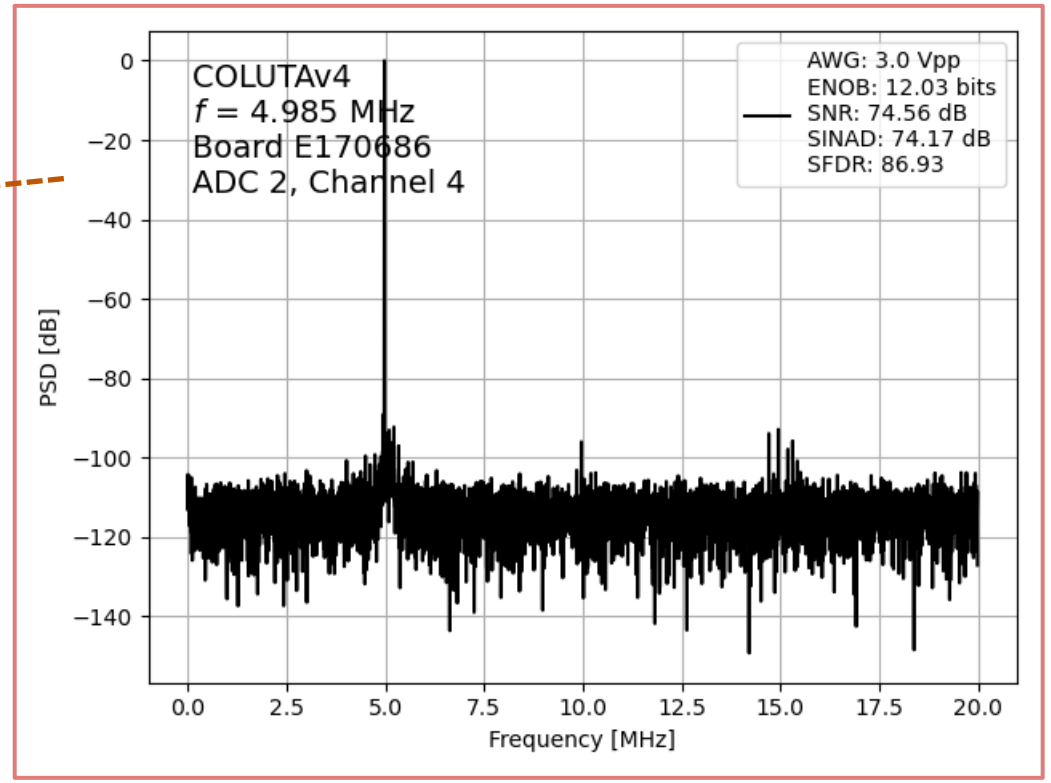




Performance - Sine Wave Sweeps

- Sine wave sweeps across amplitude and frequency show well-behaved performance exceeding specifications.



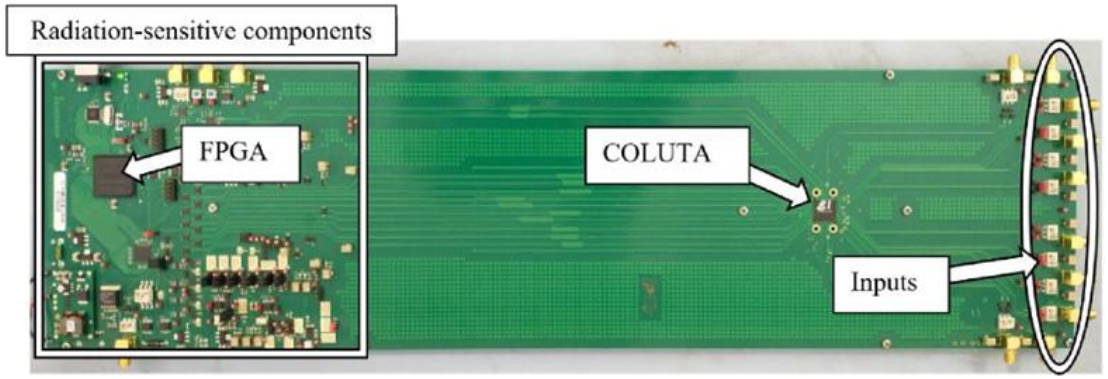


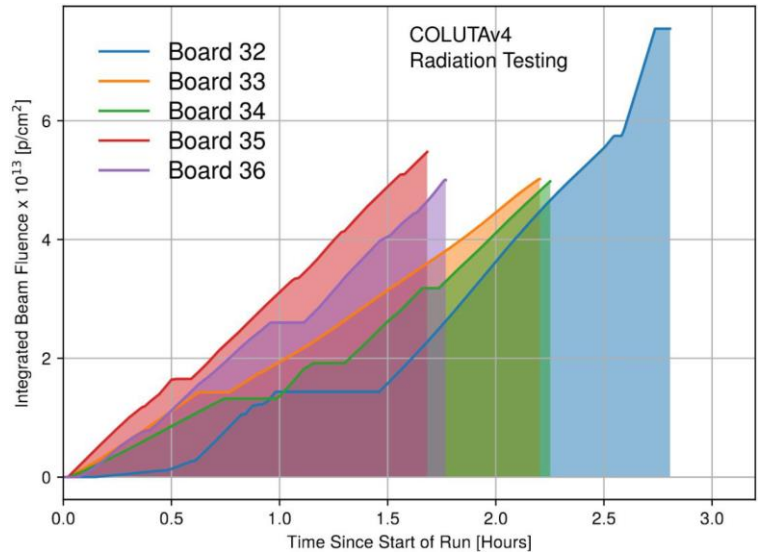
Radiation Hardness Verification

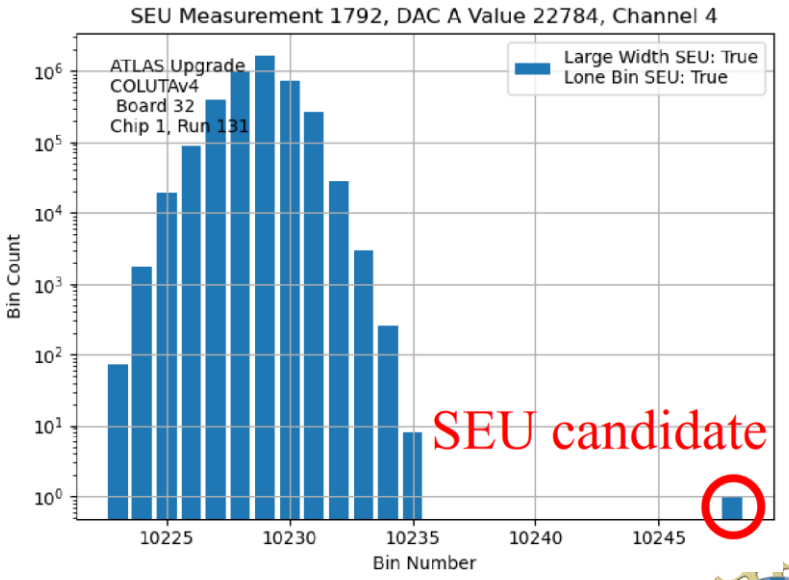
- All on-detector electronics must meet radiation hardness requirements:

TID [Gy]	NIEL [n_{eq}/cm^2]	SEE [$h_{>20\,MeV}/cm^2$]
1400 (1.5)	4.1×10^{13} (2)	1.0×10^{13} (3)

- Radiation test of COLUTAv4
  - Carried out on Aug. 6 & 7th 2022 at Boston Massachusetts General Hospital using 229 MeV proton beam.
    - Additional test (BGA packaged chips) planned.
  - 5 chips irradiated beyond spec (~5 x 10^{13} p/cm^2) with no chip latch-ups.
  - Elongated test board with 8-ch passive inputs:

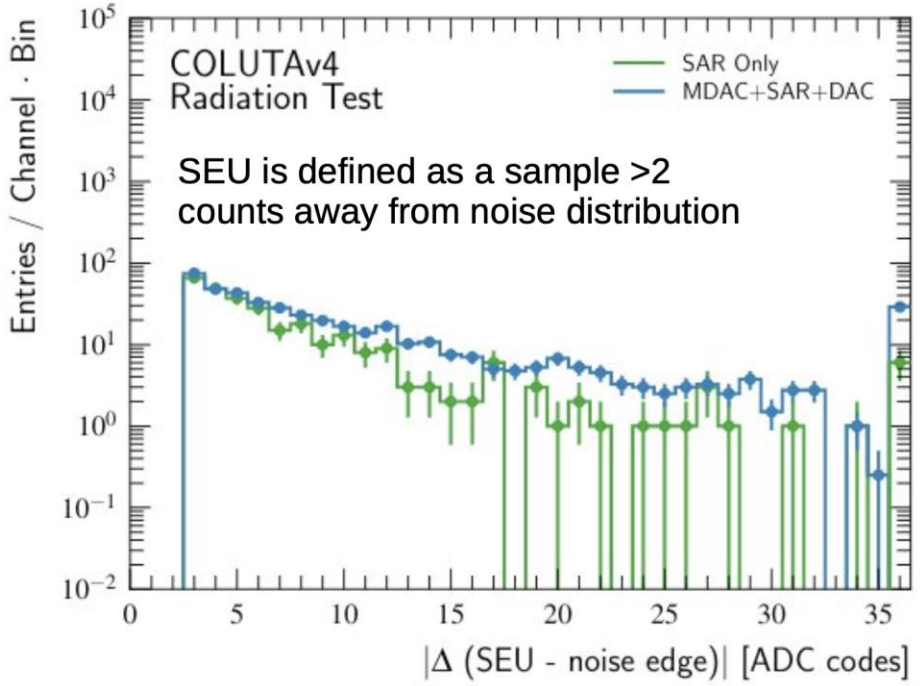


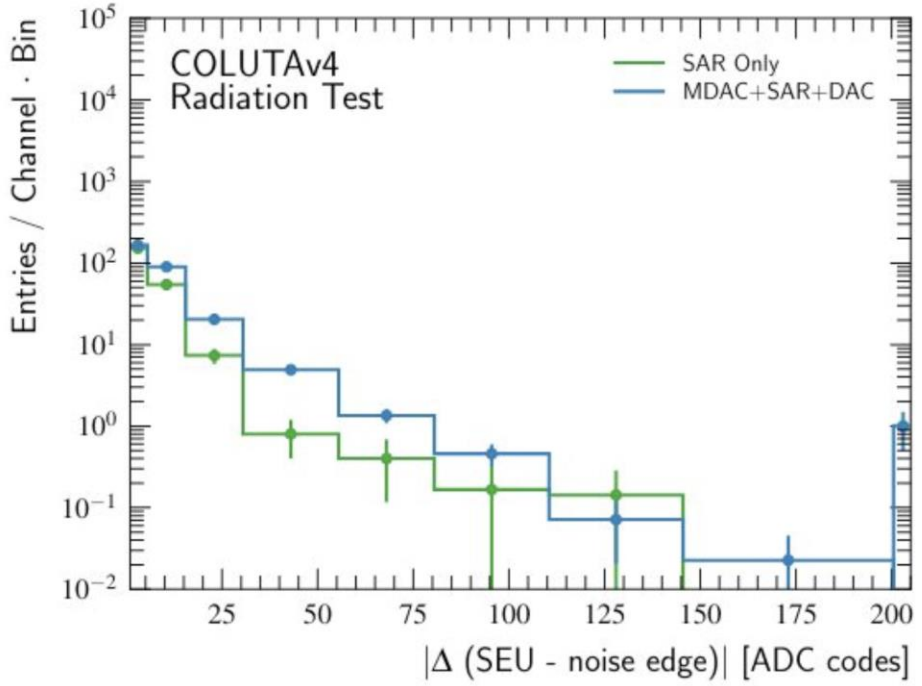




Radiation Hardness Verification

- SEU's near the noise distribution are probably "analog" errors.
  - *E.g.* ionizing particle disturbing charge in the sample/hold capacitors.
- SEU's far from the noise distribution are probably "digital" errors.
  - *E.g.* ionizing particle flipping a bit.



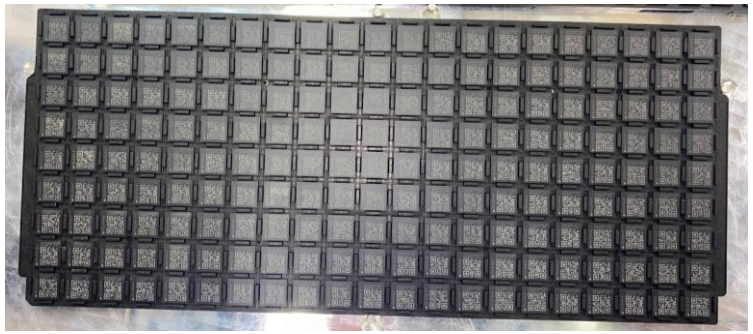


- **Over the course of the HL-LHC, we expect a total of 6140 SEU's per channel. 75% will be within 20 ADC counts of the correct code; less than 1% will be greater than 100 counts away.**

Robotic Test Stand

- Required on detector (plus spares): ~ 60k COLUTA chips. **Automated testing required!**
  - Two test sites planned
- Automated Robotic Tester for Mass Inspections of COLUTA ASIC (ARTEMICA).
  - Pre-production engineering run ASIC under test now.
- Robot arm functionalities:
  - Read and decode ASIC QR code.
  - Pick chip from tray and place the chip in the socket.
  - Remove chip from the socket and place it back on the tray.
  - Move chips between trays.
- Robot control and operation integrated with data acquisition software.
  - GUI can control the robot arm, power supply, signal generators.
- Automated test procedure:

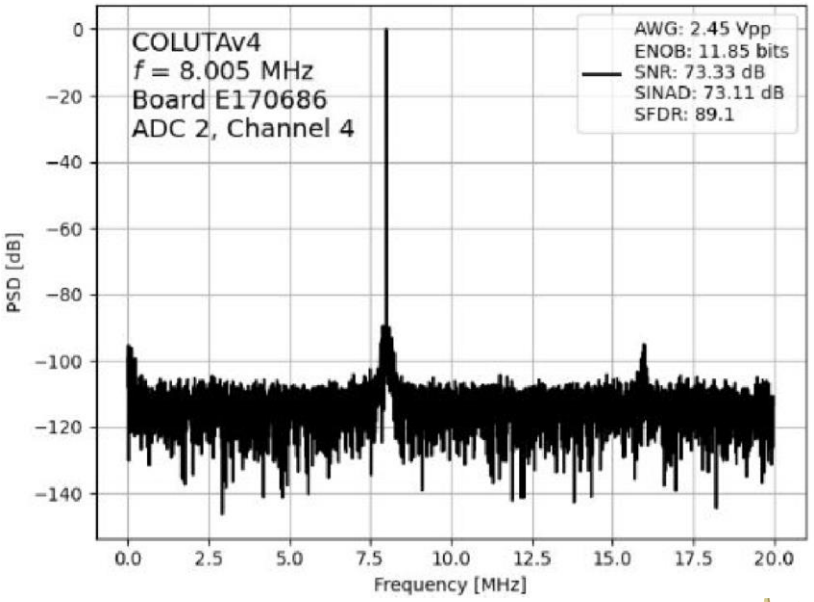
1. Move the robot arm over a chip and decode the QR code to obtain chip ID.
2. Socket the chip.
3. Perform a “dead-or-alive” test to ensure chip is functional.
4. Perform a “performance” test and classify the chip-performance.
5. Based on its performance, sort the chip-under-test into the graded-chips tray.
6. Repeat



Chip Classification

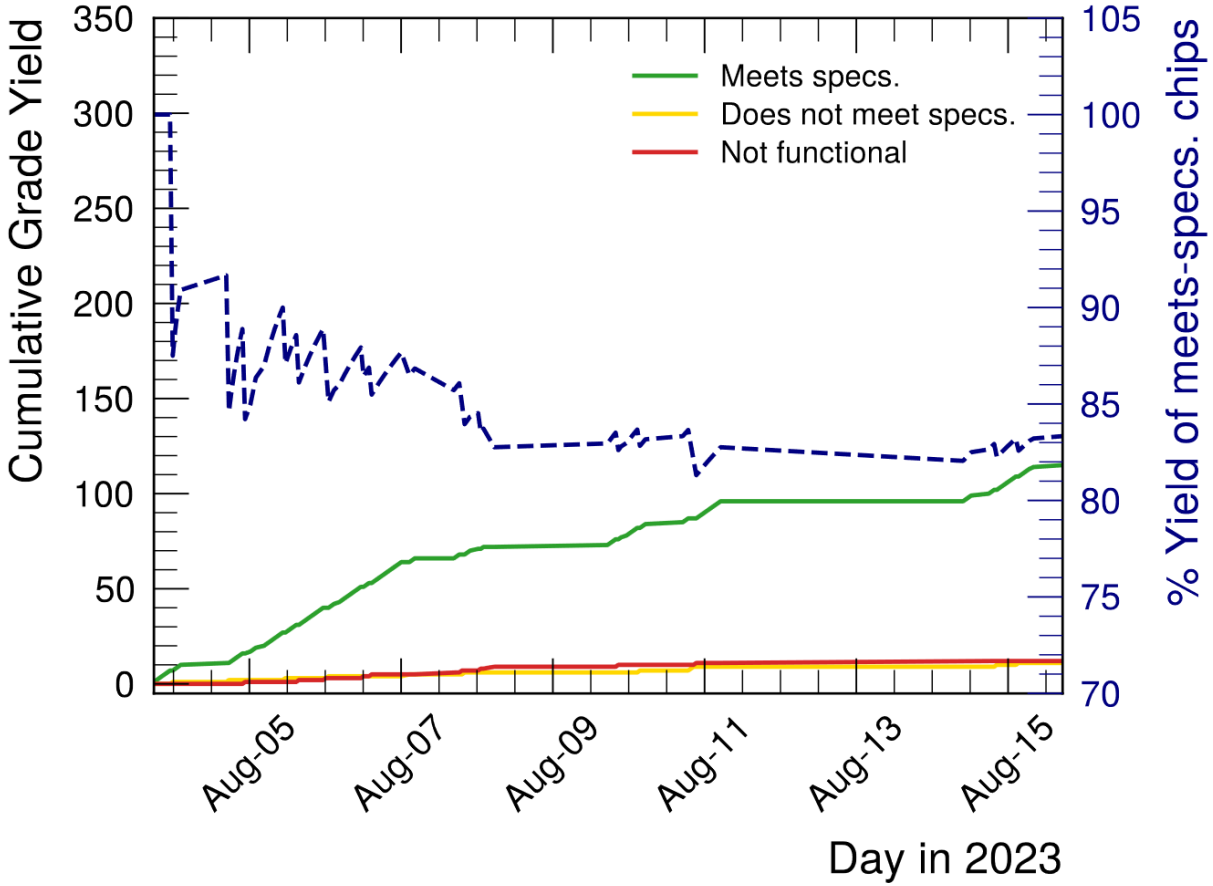
- Perform two set of tests on the chip-under-test:
  - Dead-or-Alive test to measure chip health.
  - Performance test to calibrate the channels and measure chip performance.
  - Chip is discarded if dead-or-alive test fails
    - All chips tested so far are functional, no “dead” chips observed yet.
- Chips sorted into three categories:
  - Functional & meets specs.
  - Functional & does not meet specs.
  - Not functional.
- Sine-wave performance with f_{sine}= 8MHz and amplitude near ADC full scale.
  - Minimum ENOB grade is used to decide the chip grade.

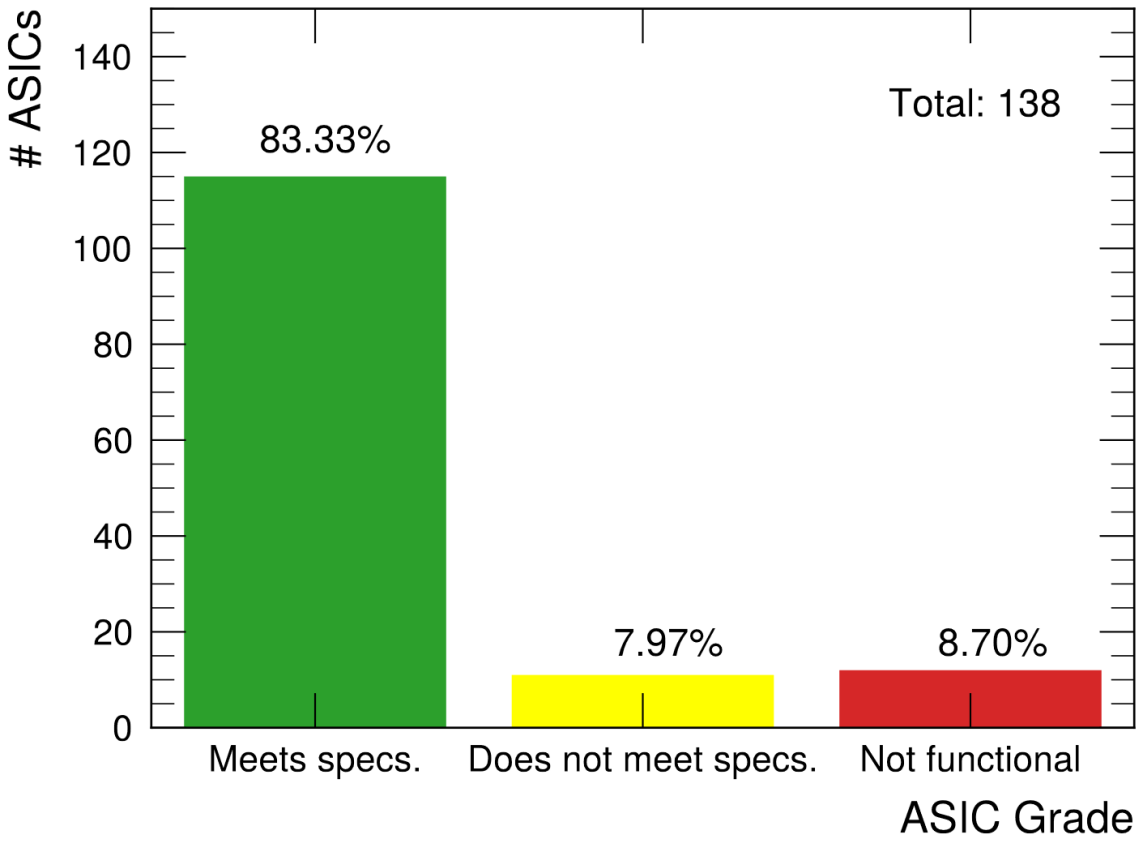
Chip Quality	min(Ch. 1, Ch. 4) ENOB [transformer_enob]	Ch. 2 ENOB [amplifier_enob]
Functional & meets specs.	≥ 11.5 [11.0, 11.5)	≥ 10.5 [10.0, 10.5)
Functional, does not meet specs.	[10.5, 11.0) [10.0, 10.5)	[9.8, 10.0) [9.6, 9.8)
Not functional	≤ 10.0	≤ 9.6



Preliminary Mass Testing Results

Mass testing with preproduction (engineering run) ASICs

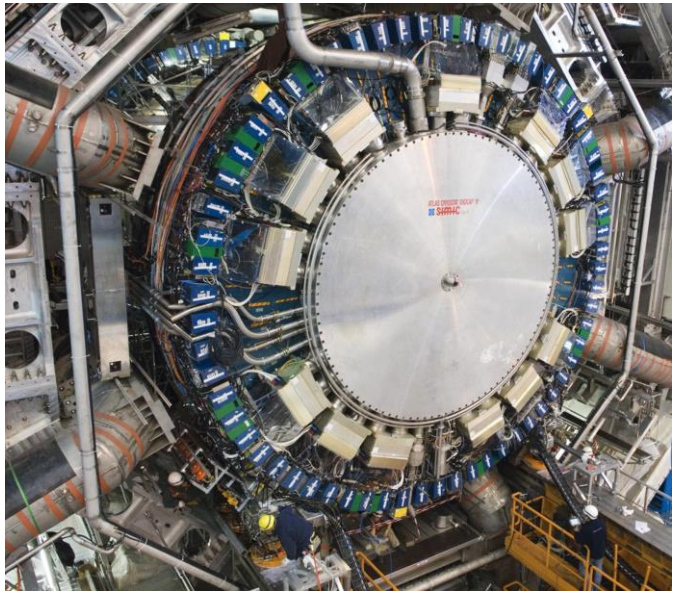




Developing new testboard with identical inputs to measure uniformly the channel performance.

Summary

- The LAr calorimeter is vital to the success of the physics program at ATLAS in the HL-LHC.
  - Current LAr readout does not meet HL-LHC trigger requirements, nor will it survive full HL-LHC radiation dose.
  - All LAr electronics (on- and off-detector) will be replaced by **2029** for HL-LHC operation (except cold preamp/summing in HEC).
  - Designed to run through **2041**.
- Major progress on COLUTA ADC for LAr HL-LHC upgrade.
  - Full custom LAr-specific ADC ASIC in pre-production. Meet specifications for analog performance.
  - Preparing for mass testing of 60,000 chips required on detector.
- On schedule for installation into ATLAS cavern beginning in **2026**, after the end of LHC Run 3.



Backup

Performance – INL/DNL

Slow sine wave/histogramming used to test DNL; linear DAC ramp used to test INL;

$$DNL_j = \frac{V_{j+1} - V_j}{1\ LSB} - 1$$

$$INL_j = \frac{V_j - V_{fit,j}}{1\ LSB}$$