The hardware platform for ATLAS readout during High Luminosity LHC

TWEPP 2023, Geremeas, Sardinia
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FELIX

Outline

- LHC Upgrades
- TDAQ & ATLAS Upgrades
- PHASE II FELIX
  - Hardware Prototyping
  - FLX 182: Built in Self Test
  - FELIX Firmware
  - FELIX Software
- Prototyping & Integration
- Summary

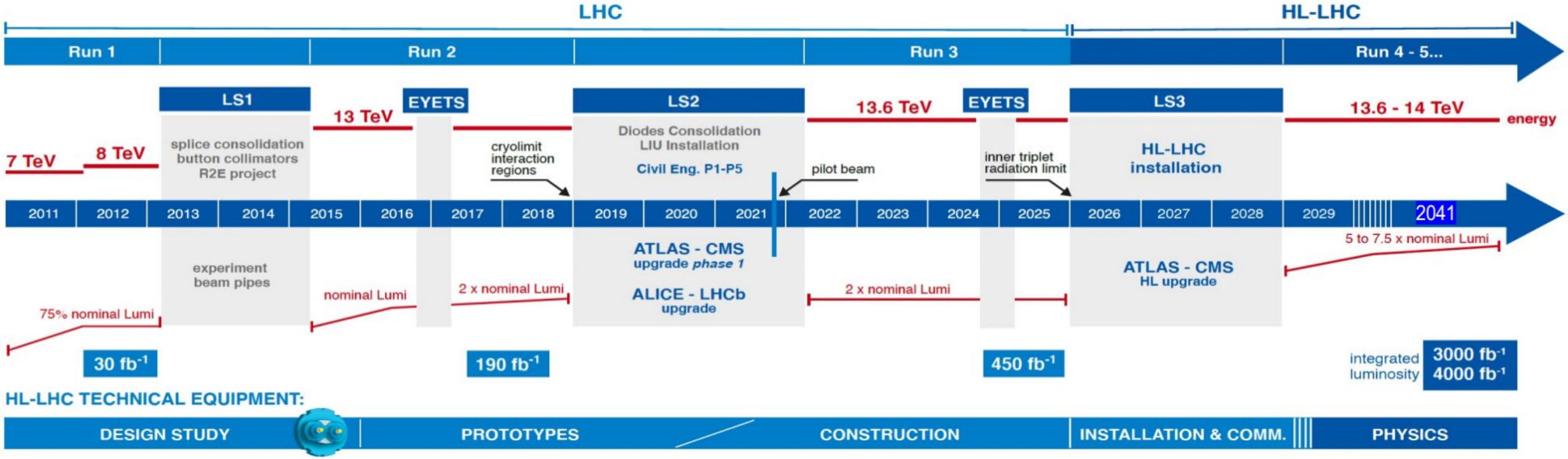
LHC Upgrades

PHASE I Upgrades

- New Small Wheel, Muon Barrel (BIS7/8), LAr Calorimeter Trigger & FLX 712
- integrated luminosity 450 fb^{-1}, instantaneous luminosity $2x10^{34}$ $s^{-1}cm^{-2}$, pileup 06

Phase II Upgrades - High-Luminosity LHC

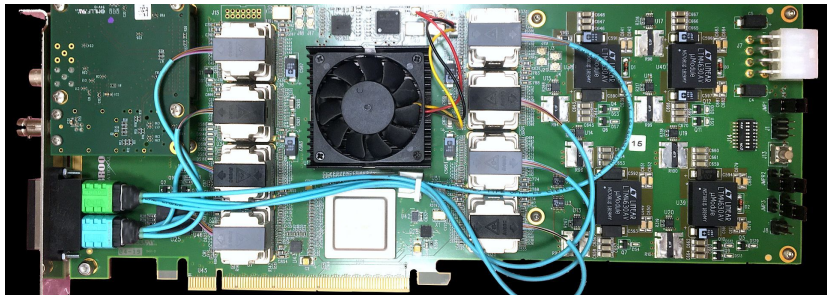
- Inner Tracker, High Granularity Timing Detector (HGTD), New Muon Chambers & FLX 182
- integrated luminosity 3000 fb^{-1}, instantaneous luminosity $7.5x10^{34}$ $s^{-1}cm^{-2}$, pileup up 200



TDAQ : Phase I

Front-End Link eXchange (FELIX)

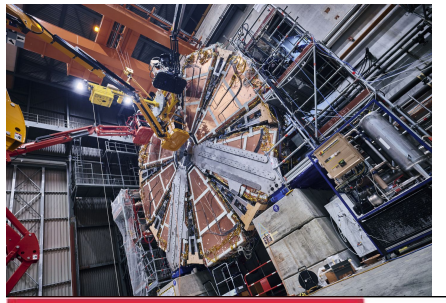
- Custom FPGA-based PCIe card that aggregates custom front-end links and passes it to Software Readout Drivers (SW ROD)
- FELIX distributes the LHC clock/trigger/control information to sub-detector front-ends
- SW ROD builds & aggregates events
- FELIX is generic for all detectors, SW ROD software is specific to sub-detectors



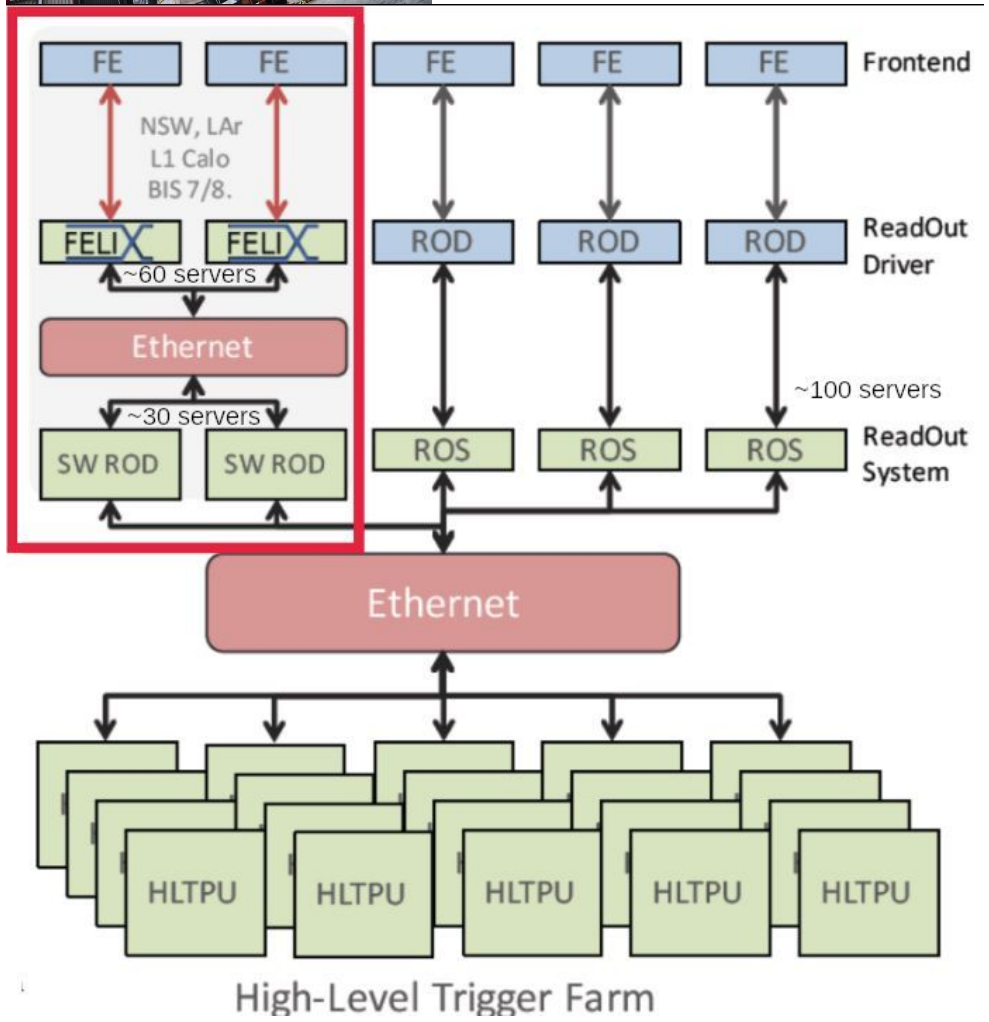
100 FLX 712 cards
up to 48 links, 4.8G and 9.6G
Kintex Ultrascale FPGA
PCIe Gen 3x16 lanes

60 Host Servers
Intel Xeon E5-1660 v4

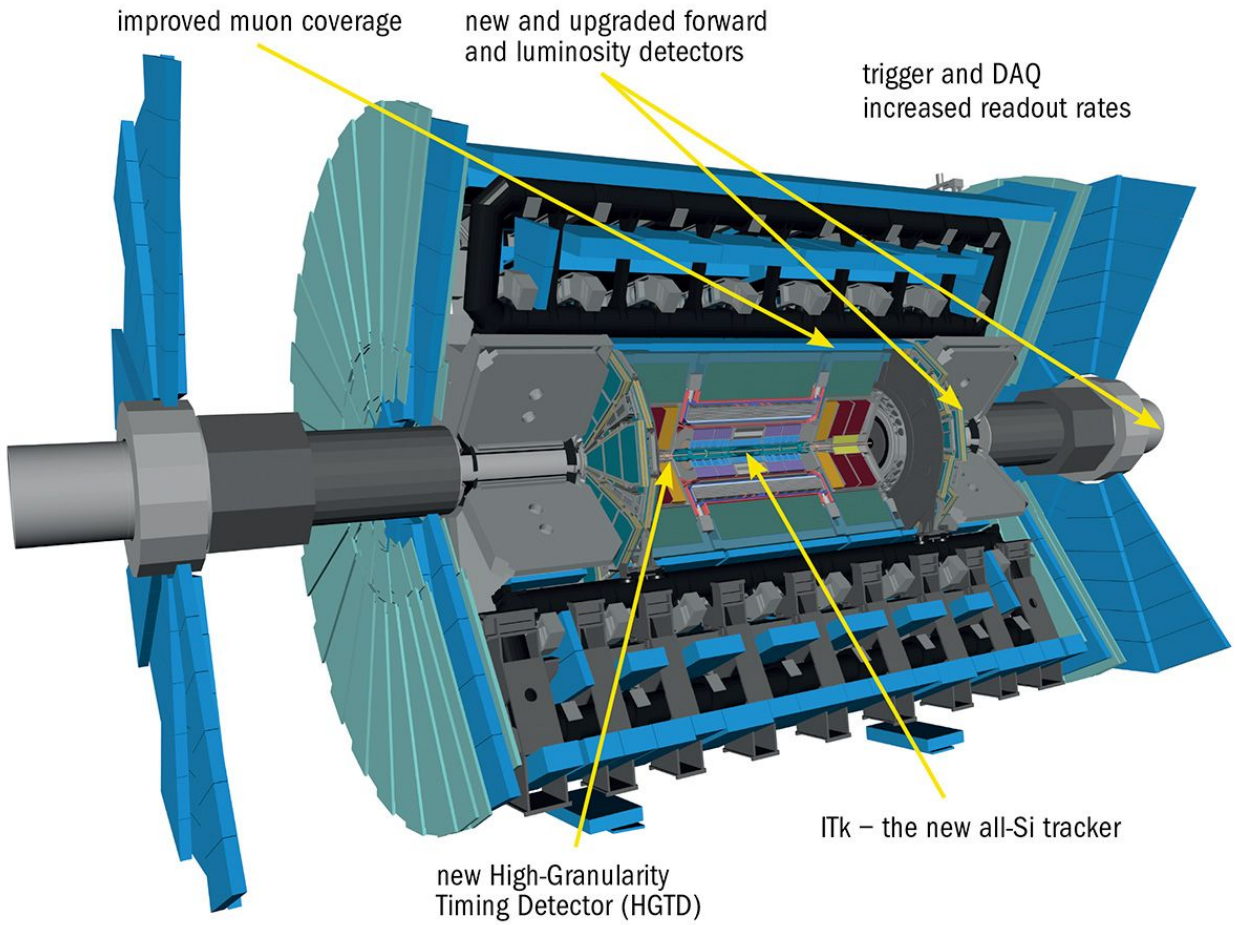
+30 SW RODs

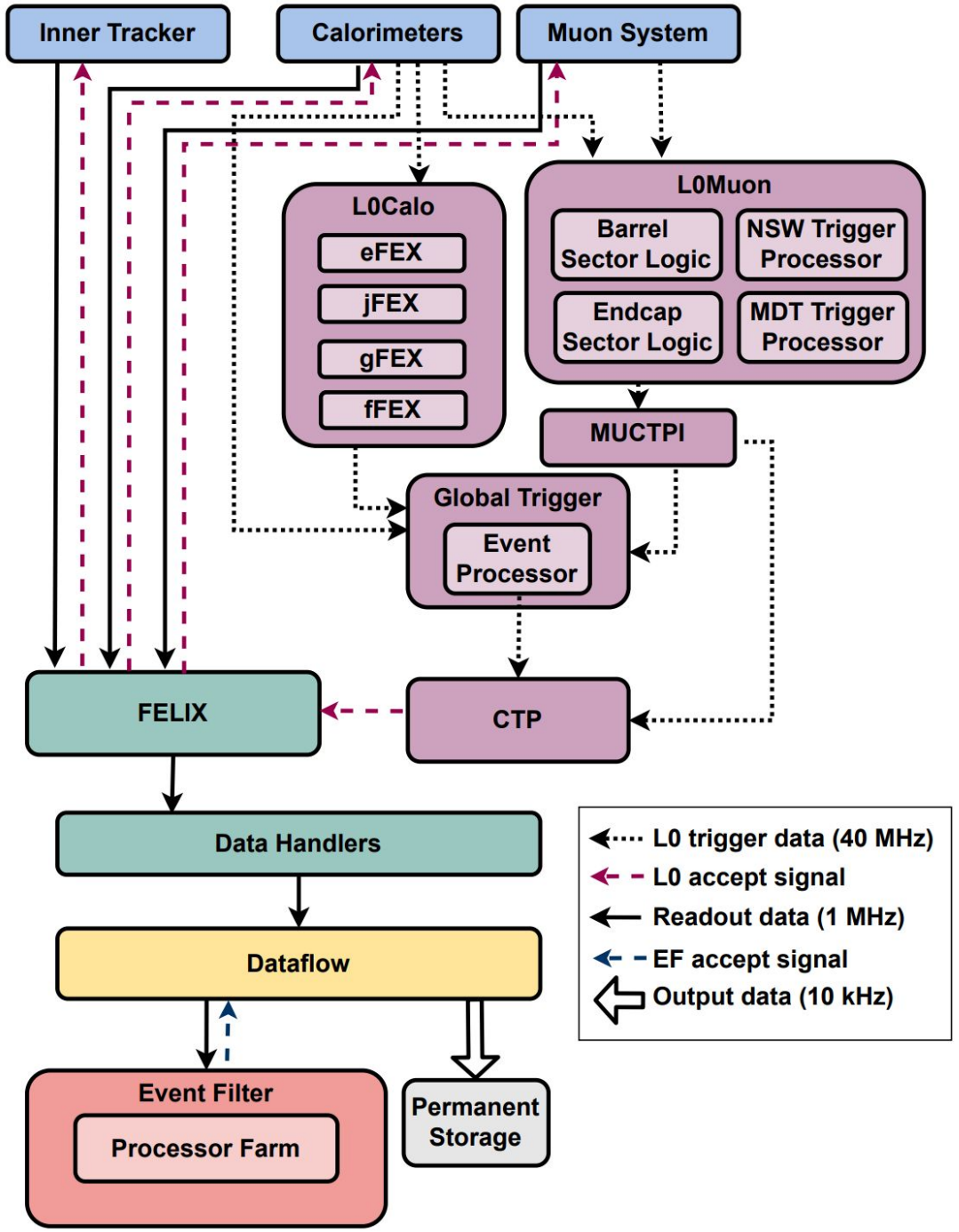


FELIX removes layer of custom electronics (RODs)



ATLAS Phase II Upgrades





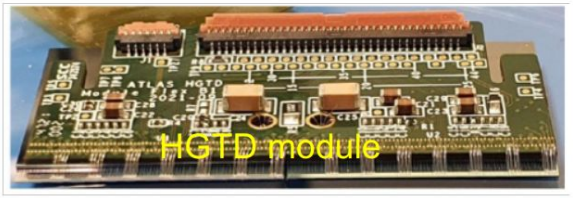
TDAQ: Phase II

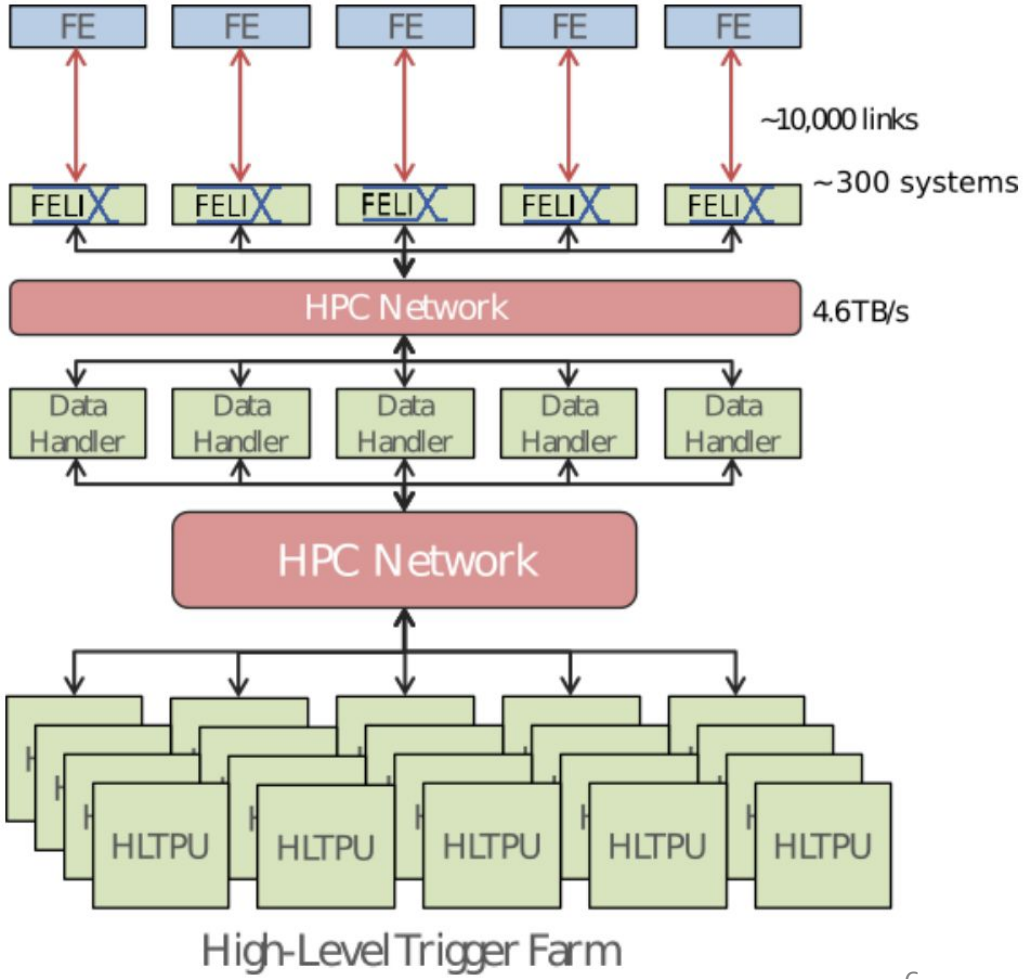
FELIX system will be used to readout all sub-detectors, and need to accommodate

- x10 trigger rate (1MHz)
- x20 readout rate (4.6 TB/s)
- Will build on Phase I functionalities

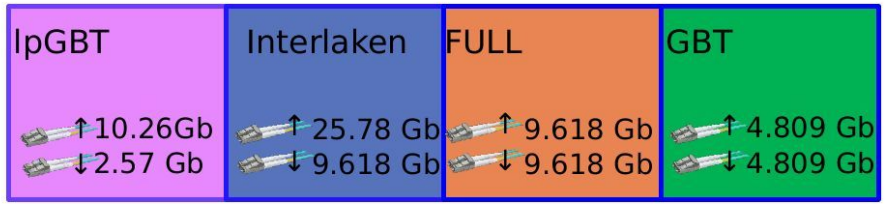
Data Handlers build and aggregate events, communicate with higher level trigger farm

- Will build on SW ROD functionalities



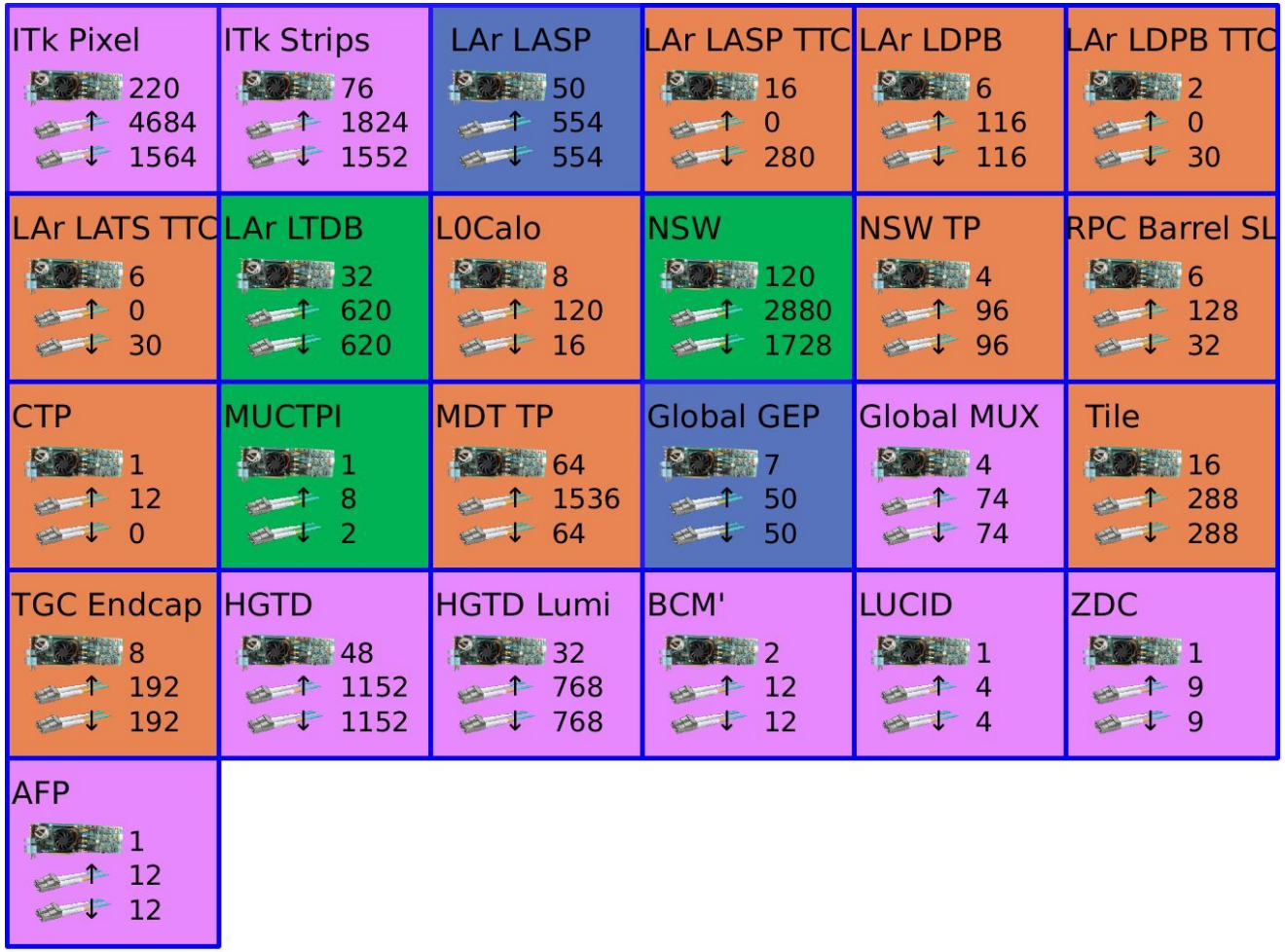


ATLAS Sub-detector Protocols



4 link protocols supported

- lpGBT & GBT - custom ASIC on detector electronics
  - Logical links (e-links) supporting 8b10b, 6b8b, HDLC, TTC 1, Aurora & Endeavour encoding
- FULL (8b10b) and Interlaken
  - Distribution of Timing/trigger/control



Phase II Hardware Prototype

FELIX 182

- FPGA: AMD Versal Prime VM1802
- 16 lane PCIe Gen4 interface (240 Gb/s)
- 4 FireFly transceivers with 3 possible configurations
  - 24 links up to 25 Gb/s
  - 24 links up to 10 Gb/s (CERN-B FireFly)
- One duplex FireFly transceiver with 2 possible configurations with 14 or 25 Gb/s FireFly TRx
  - new protocol for Timing Trigger & Control (LTI)
- Versal Processing system, runs PetaLinux
  - Monitor temperatures & voltages, update flash memory, perform build-in self test (BIST)
- Using Host server for testing, AMD Epyc 9004 CPU, PCIe Gen5

FELIX 155

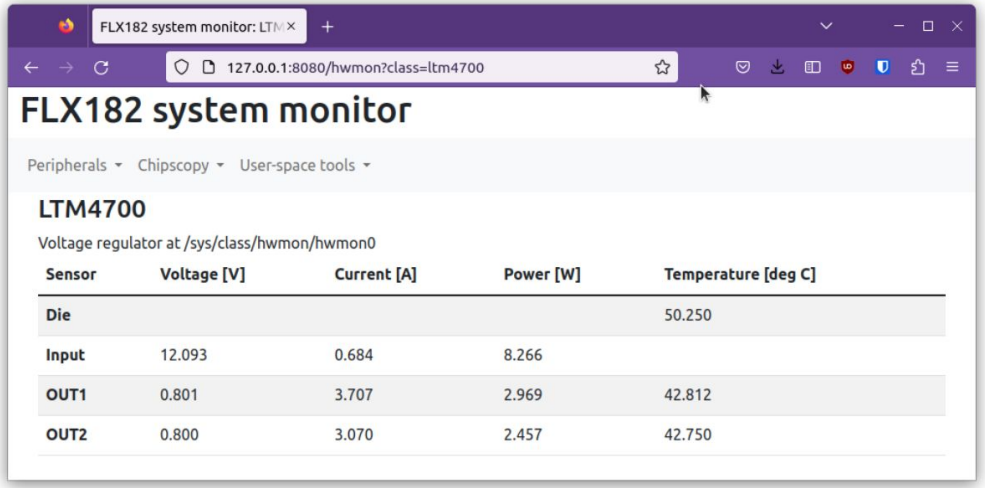
- AMD Versal Premium VP1552 FPGA, PCIe Gen5x16 interface (482 Gb/s) , up to 48 bidirectional links

FELIX 182: Built in Self Test (BIST)

- Automated self tests allow for
  - Testing the board at the assembly facility
  - Fast board diagnostics and repair
- BIST Uses Versal programming logic, running PetaLinux
- Web application can be used to monitor sensors & peripheral configuration
- Developed in python & provides flexible configurations for support of any board

Testing capabilities:

- Monitor I2C peripherals on the board
- Xilinx chipscope tests (IBERT, PCIe loopback eyescans, DDRMC)
- Linux software tests (DRAM, ethernet, QSPI flash)
- Generate a test report published in database

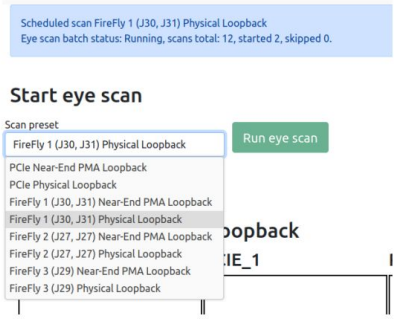


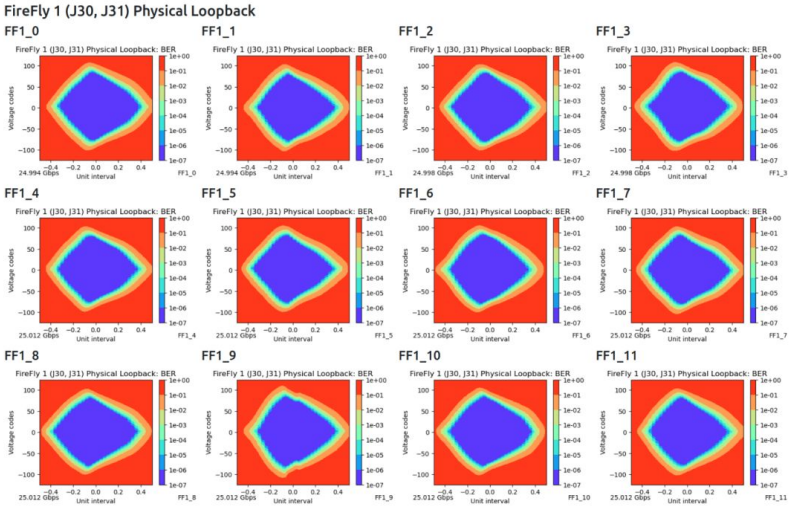
Voltage monitor

Input	Value
gty_avcc_103	0.876 V
gty_avcc_104	0.875 V
gty_avcc_105	0.876 V
gty_avcc_106	0.876 V
gty_avcc_200	0.879 V
gty_avcc_201	0.879 V
gty_avcc_202	0.879 V
gty_avcc_203	0.878 V
gty_avcc_204	0.879 V
gty_avcc_205	0.880 V
gty_avcc_206	0.880 V
gty_avccaux_103	1.499 V
gty_avccaux_104	1.500 V

FELIX 182: Built in Self Test (BIST)

- Eyescans





SFP & Firefly report

Name	Type	Temperature [deg C]	Vendor name	Part number	Serial number
FireFly_J27	CERN-B-Y12 Receiver	41.000	SAMTEC	ECUOR12251000513	UA2136014E
FireFly_J28	CERN-B-Y12 Transmitter	61.000	SAMTEC	ECUOT12251000513	UA220600UX
FireFly_J29	SAMTEC FireFly ECUO 25G/28G Transceiver	35.000	Samtec Inc	OTP-200941-01	UA190200K3
FireFly_J30	CERN-B-Y12 Receiver	44.000	SAMTEC	ECUOR12251000513	UA2136012M
FireFly_J31	CERN-B-Y12 Transmitter	45.000	SAMTEC	ECUOT12251000513	UA211205QU

SI53156 report

Device	Output enabled? 0	1	2	3	4	5	Set amplitude? (uncheck for default amplitude)	Amplitude
PCIe clk buffer (U37)	☑	☑	☑	☑	☑	☑	☑	800 mV

Update all

DDRMC Calibration Report

```
DDRMC Status
--------------------
Calibration Status:  PASS
Overall Health:  GOOD
Message:  No errors detected during calibration.

--------------------
Status Registers
--------------------
DDRMC ISR Table
  ddrmc_isr_ce0_ecc0:  0
  ddrmc_isr_ce0_ecc1:  0
  ddrmc_isr_ce1_ecc0:  0
  ddrmc_isr_ce1_ecc1:  0
  ddrmc_isr_ch0_data_par:  0
  ddrmc_isr_ch1_data_par:  0
  ddrmc_isr_dc_cmd0_fatal:  0
  ddrmc_isr_dc_cmd1_fatal:  0
  ddrmc_isr_dram_parity0:  0
  ddrmc_isr_dram_parity1:  0
  ddrmc_isr_dram_parity_fatal_0:  0
  ddrmc_isr_dram_parity_fatal_1:  0
  ddrmc_isr_na_cmd:  0
  ddrmc_isr_na_cmd0:  0
  ddrmc_isr_na_cmd1:  0
  ddrmc_isr_na_cmd_fatal:  0
  ddrmc_isr_nsu_0:  0
  ddrmc_isr_nsu_1:  0
  ddrmc_isr_nsu_2:  0
  ddrmc_isr_nsu_3:  0
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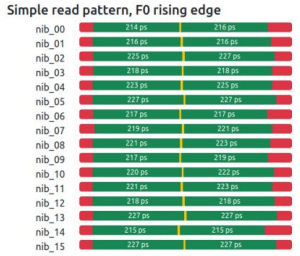
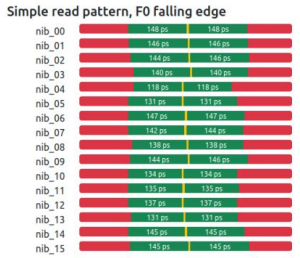
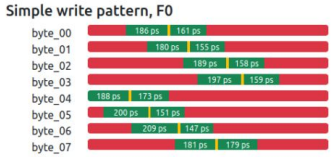
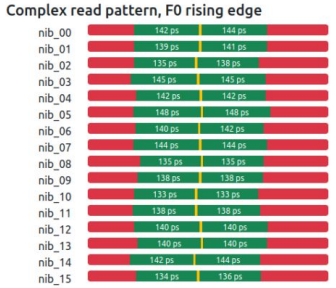
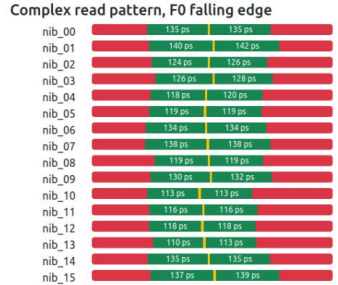




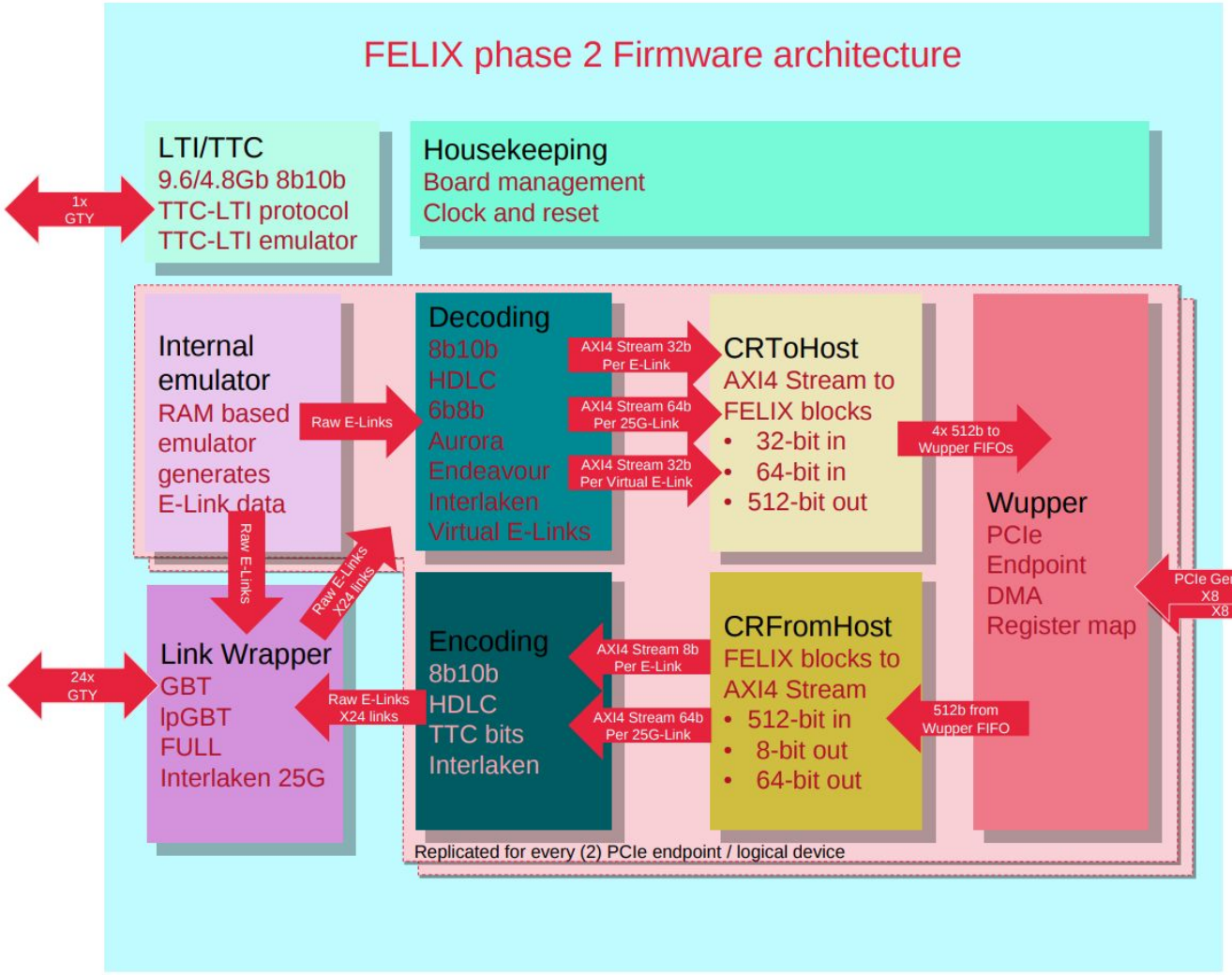






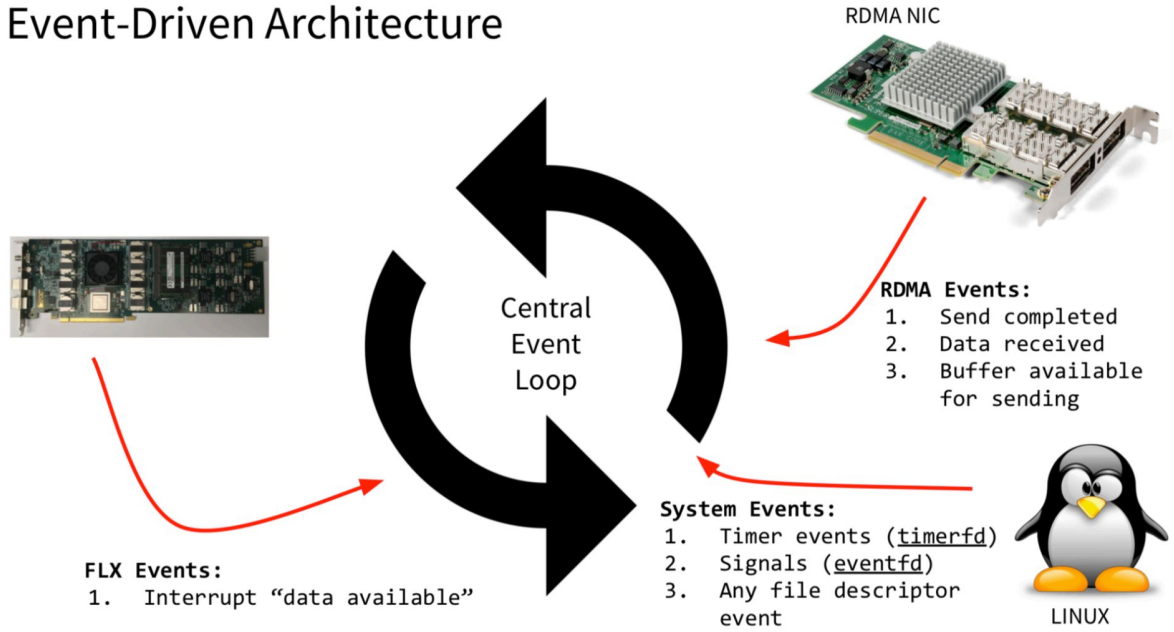
FELIX 182 Firmware

- Interface for Trigger/Control/Timing for both LTI/TTC
  - LTI distributes the LHC clock/trigger/control information to FELIX
  - FELIX redistributes clock to front-end electronics using GBT, lpGBT or LTI-FE format
  - Some sub-detectors need clock distribution with < 5 ps precision - achieved with additional phase detector (DDMTD) that ensures consistent startup phase determination
- Link Wrapper sends/receives data
- Encoding/Decoding blocks support lpGBT & 25 Gb/s & Interlaken
  - lpGBT e-links support 6b8b, 8b10b, HDLC, Aurora & Endeavour
- Wupper provides interface to PCIe DMA core (2 PCIe endpoints per card)
  - Supports Gen4 & Gen5
  - Internal emulator generates e-link data for testing fw blocks



FELIX Software

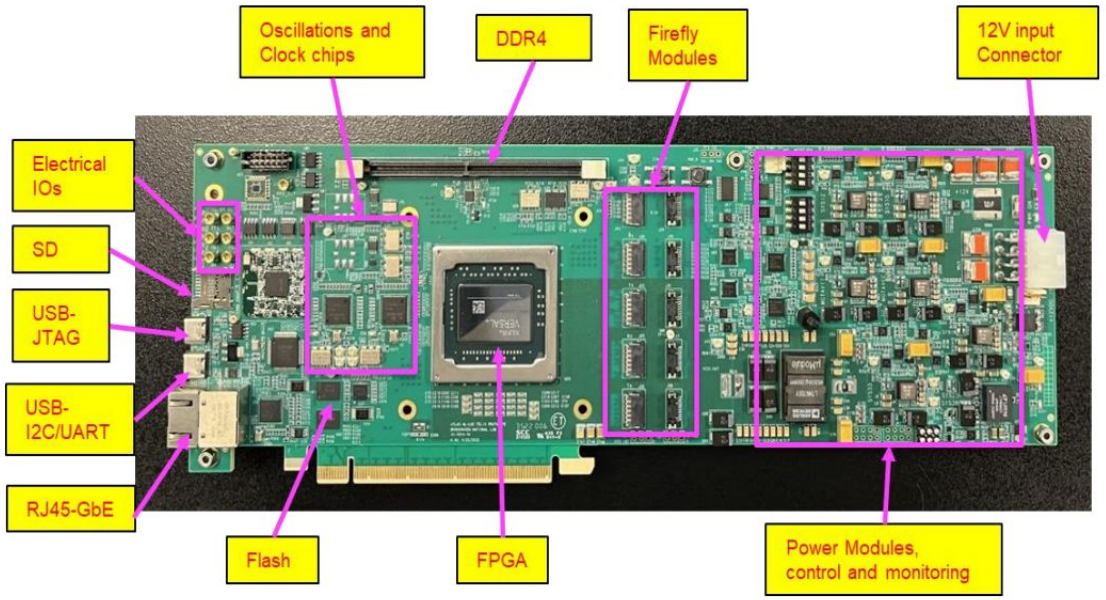
- Access to the FELIX hardware controlled via device drivers
- Basic configuration/monitoring (f-tools suite, e-link configuration, felix-monitoring)
- Felix-star readout application
  - Parallel readout of up to 10 DMA buffers per PCIe cards
  - Uses RDMA network technology for high-throughput, low-overhead data transfers
  - Will support TCP/IP for monitoring/slow control traffic
  - A simple API provides network protocol agnostic interface



- Dataflow for Detector Control System has dedicated buffers/threads and uses TCP/IP rather than RDMA

Prototyping status & Integration

- Successfully tested the first FLX-182 prototypes
- 10 FELIX 182 prototypes are in production and will be ready in Fall of 2023 for integration/testing with sub-detectors
- Operation with FELIX fw at PCIe Gen4 speeds was verified
- Integration with ATLAS Global Trigger has been successfully tested
- BIST features demonstrated
- FELIX also used in ProtoDUNE SP, NA62, sPHENIX, SPIDR4

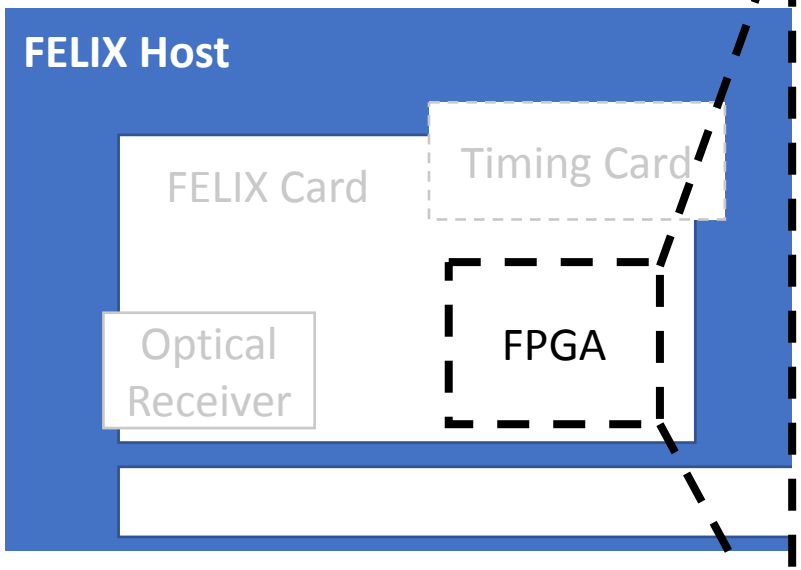


Summary

- FELIX for Phase I ATLAS upgrades was installed and commissioned successfully
- FELIX for Phase II ATLAS under development
- Support for FLX-182 firmware and software under development
- Early prototypes tested successfully, more coming in Fall of 2023

Backup

FLX-712 Fw

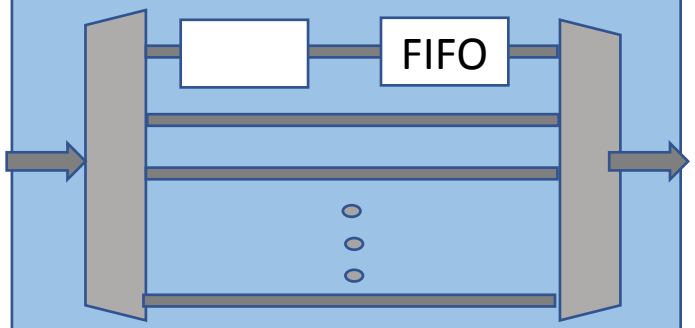


TTC & BUSY:
Decode trigger data and recover LHC clock

GBT Wrapper:
Send/receive GBT Data

Central Router: Map GBT data to E-link format

Demultiplex GBT link into data streams, decode data stream (8b/10b or HDLC), form 1 kbyte blocks read by DMA



Wupper PCIe/ DMA Engine:
Push data to the memory

GBT Mode: 24 bi-directional radiation-hard, GBT links (4.8Gb/s – 3.2Gb/s with error correction)

FULL Mode: 12 links, custom light-weight protocol from front-end-path (9.6Gb/s)