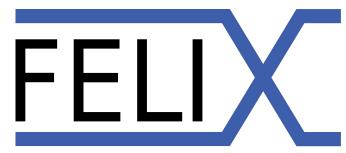


The hardware platform for ATLAS readout during High Luminosity LHC

TWEPP 2023, Geremeas, Sardinia Nikolina Ilic on behalf of the TDAQ ATLAS Collaboration IPP & University of Toronto





Outline

- LHC Upgrades
- TDAQ & ATLAS Upgrades
- PHASE II FELIX
 - Hardware Prototyping
 - FLX 182: Built in Self Test
 - FELIX Firmware
 - FELIX Software
- Prototyping & Integration
- Summary

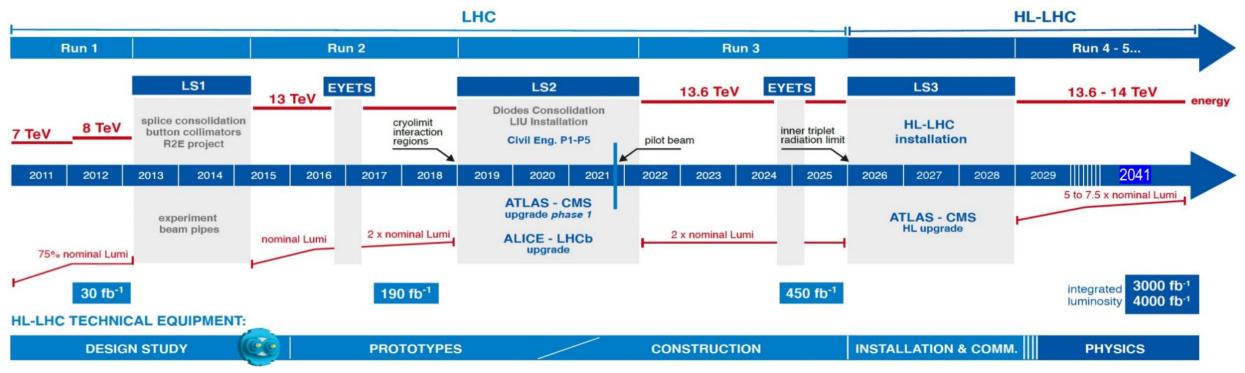
LHC Upgrades

PHASE I Upgrades

- New Small Wheel, Muon Barrel (BIS7/8), LAr Calorimeter Trigger & FLX 712
- integrated luminosity 450 fb⁻¹, instantaneous luminosity 2x10³⁴ s⁻¹cm⁻², pileup 06

Phase II Upgrades - High-Luminosity LHC

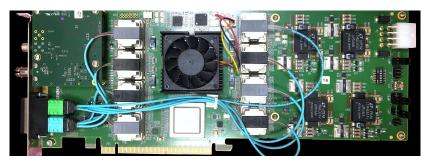
- Inner Tracker, High Granularity Timing Detector (HGTD), New Muon Chambers & FLX 182
- integrated luminosity 3000 fb⁻¹, instantaneous luminosity 7.5x10³⁴ s⁻¹cm⁻², pileup up 200



TDAQ : Phase I

Front-End Link eXchange (FELIX)

- Custom FPGA-based PCIe card that aggregates custom front-end links and passes it to Software Readout Drivers (SW ROD)
- FELIX distributes the LHC clock/trigger/control information to sub-detector front-ends
- SW ROD builds & aggregates events
- FELIX is generic for all detectors, SW ROD software is specific to sub-detectors

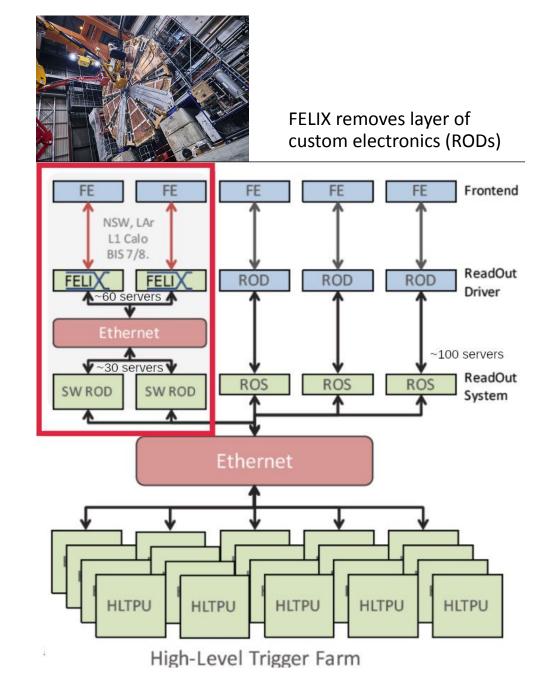


100 FLX 712 cards

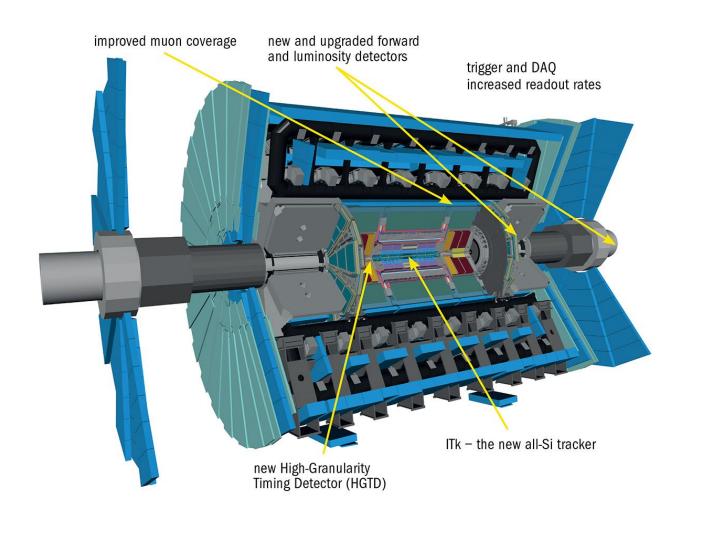
up to 48 links, 4.8G and 9.6G Kintex Ultrascale FPGA PCIe Gen 3x16 lanes

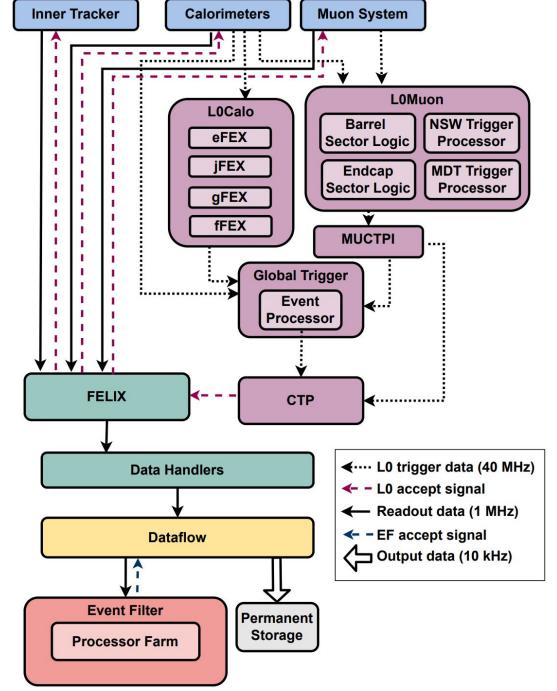
60 Host Servers Intel Xeon E5-1660 v4

+30 SW RODs



ATLAS Phase II Upgrades





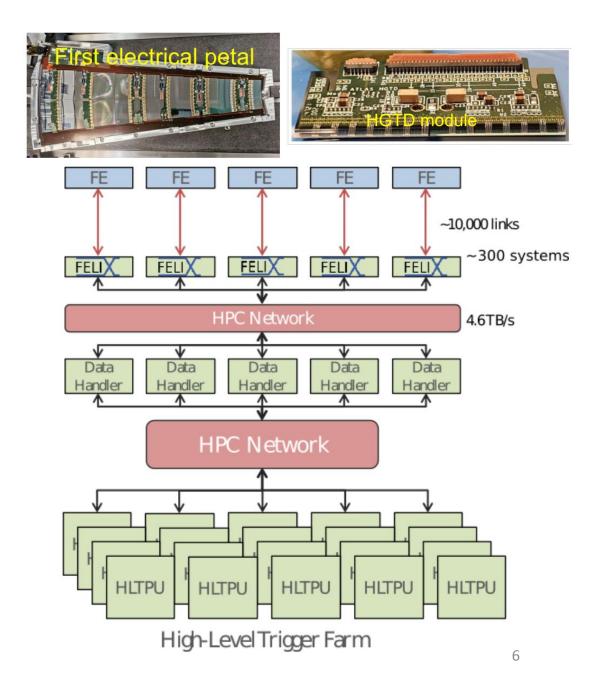
TDAQ: Phase II

FELIX system will be used to readout all sub-detectors, and need to accommodate

- x10 trigger rate (1MHz)
- x20 readout rate (4.6 TB/s)
- Will build on Phase I functionalities

Data Handlers build and aggregate events, communicate with higher level trigger farm

• Will build on SW ROD functionalities



ATLAS Sub-detector Protocols

lpGBT	Interlaken	FULL	GBT
			● 1 4.809 Gb ● ↓ 4.809 Gb

4 link protocols supported

- IpGBT & GBT custom ASIC on detector electronics
 - Logical links (e-links) supporting 8b10b, 6b8b, HDLC, TTC 1, Aurora & Endeavour encoding
- FULL (8b10b) and Interlaken
 - Distribution of
 - Timing/trigger/control

ITk Pixel 220 4684 1564	ITk Strips 76 1824 1552	LAr LASP 50 554 554 554	LAr LASP TTC 16 0 280	200 6 →↑ 116	LAr LDPB TTC 2 0 30
LAr LATS TTC 6 0 30	LAr LTDB 32 620 620	L0Calo 8 120 16	NSW 120 2880 1728	201 4 →1 96	RPC Barrel SL
CTP 1 12 0	MUCTPI 1 8 2	MDT TP 64 1536 64	Global GEP 7 50 50 50	Global MUX 4 74 74 74	Tile 16 288 288 288
TGC Endcap 8 192 192 192	HGTD 48 1152 1152	HGTD Lumi 32 768 768 768	BCM' 2 12 12	LUCID 1 4 4 4 4	ZDC 1 9 2 9
AFP 1 12 12 12					

Phase II Hardware Prototype

FELIX 182

- FPGA: AMD Versal Prime VM1802
- 16 lane PCIe Gen4 interface (240 Gb/s)
- 4 FireFly transceivers with 3 possible configurations
 - 24 links up to 25 Gb/s
 - 24 links up to 10 Gb/s (CERN-B FireFly)
- One duplex FireFly transceiver with 2 possible configurations with 14 or 25 Gb/ FireFly TRx
 - new protocol for Timing Trigger & Control (LTI)
- Versal Processing system, runs PetaLinux
 - Monitor temperatures & voltages, update flash memory, perform build-in self test (BIST)
- Using Host server for testing, AMD Epyc 9004 CPU, PCIe Gen5

FELIX 155

• AMD Versal Premium VP1552 FPGA, PCIe Gen5x16 interface (482 Gb/s) , up to 48 bidirectional links



FELIX 182: Built in Self Test (BIST)

- Automated self tests allow for
 - Testing the board at the assembly facility
 - Fast board diagnostics and repair
- BIST Uses Versal programming logic, running PetaLinux
- Web application can be used to monitor sensors & peripheral configuration
- Developed in python & provides flexible configurations for support of any board

Testing capabilities:

- Monitor I2C peripherals on the board
- Xilinx chipscope tests (IBERT, PCIe loopback eyescans, DDRMC)
- Linux software tests (DRAM, ethernet, QSPI flash)
- Generate a test report published in database

FLX182 system monitor: LTM× + × - □ ×										
\rightarrow G	0 🗅 127.0.0.	.1:8080/hwmon?class=ltm4	700	☆		₹	ID 🙂	U	ப	
LX182 system monitor										
Peripherals - Chipscopy - User-space tools -										
LTM470	00									
Voltage regulator at /sys/class/hwmon/hwmon0										
voicage regi	ulator at /sys/class/hw	mon/hwmon0								
Sensor	Voltage [V]	mon/hwmon0 Current [A]	Power [W]	Tempe	erature	[deg	C]			
			Power [W]	Tempe 50.250		e [deg	c]			_
Sensor			Power [W] 8.266			e [deg	c]			
Sensor Die	Voltage [V]	Current [A])	e [deg	c]			

Voltage monitor

Input	Value
gty_avcc_103	0.876 V
gty_avcc_104	0.875 V
gty_avcc_105	0.876 V
gty_avcc_106	0.876 V
gty_avcc_200	0.879 V
gty_avcc_201	0.879 V
gty_avcc_202	0.879 V
gty_avcc_203	0.878 V
gty_avcc_204	0.879 V
gty_avcc_205	0.880 V
gty_avcc_206	0.880 V
gty_avccaux_103	1.499 V
gty_avccaux_104	1.500 V

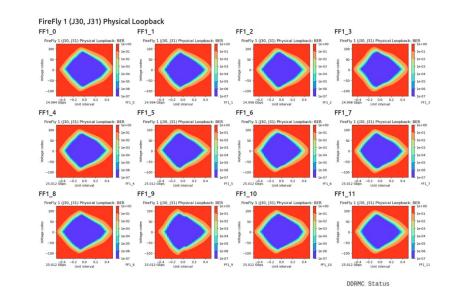
FELIX 182: Built in Self Test (BIST)

-Eyescans

Scheduled scan FireFly 1 (J30, J31) Physical Loopback Eye scan batch status: Running, scans total: 12, started 2, skipped 0.

Start eye scan





SFP & Firefly report

Name	Туре	Temperature [deg C]	Vendor name	Part number	Serial number
FireFly_J27	CERN-B-Y12 Receiver	41.000	SAMTEC	ECUOR12251000513	UA2136014E
FireFly_J28	CERN-B-Y12 Transmitter	61.000	SAMTEC	ECUOT12251000513	UA220600UX
FireFly_J29	SAMTEC FireFly ECUO 25G/28G Transceiver	35.000	Samtec Inc	OTP-200941-01	UA190200K3
FireFly_J30	CERN-B-Y12 Receiver	44.000	SAMTEC	ECUOR12251000513	UA2136012M
FireFly_J31	CERN-B-Y12 Transmitter	45.000	SAMTEC	ECUOT12251000513	UA211205QU

DDRMC Calibration Report

SI53156 report

		C	Output	enab	ed?		Set amplitude?	
Device	0	1	2	3	4	5	(uncheck for default amplitude)	Amplitude
PCIe clk buffer (U37)								800 mV 🗸
Update all								

Message: M	lo errors d	letect	ed du	iring	calibra	tion.
Status Reg	isters					
DDRMC ISR T	able					
ddrmc_isr	_ce0_ecc0:	0				
ddrmc_isr	_ce0_ecc1:	Θ				
ddrmc_isr	_ce1_ecc0:	Θ				
ddrmc_isr	_ce1_ecc1:	Θ				
ddrmc_isr	_ch0_data_	par:	Θ			
ddrmc_isr	_ch1_data_	par:	0			
ddrmc_isr	_dc_cmd0_f	atal:	Θ			
ddrmc_isr	_dc_cmd1_f	atal:	Θ			
ddrmc_isr	_dram_pari	ty0:	Θ			
ddrmc_isr	_dram_pari	ty1:	Θ			
ddrmc_isr	_dram_pari	ty_fa	tal_G): 0		
ddrmc_isr	_dram_pari	ty_fa	tal_1	L: 0		
ddrmc_isr	_na_cmd:	Θ				
ddrmc_isr	_na_cmd0:	Θ				
ddrmc_isr	_na_cmd1:	Θ				
ddrmc_isr	_na_cmd_fa	tal:	Θ			
ddrmc_isr	_nsu_0: 0)				
ddrmc_isr	_nsu_1: 0)				
ddrmc_isr	_nsu_2: 6)				
ddrmc_isr	_nsu_3: 6)				

Calibration Status: PASS Overall Health: GOOD

1 00	214 ps	216 ps			
nib_00	214 ps 216 ps	216 ps			
nib_01	210 ps 225 ps	210 ps			
nib_02	218 ps	218 ps	Simple write p	attern FO	
nib_03	223 ps	225 ps	-		
nib_04	227 ps	227 ps	byte_00	186 ps 161 p	
nib 06	217 ps	217 ps	byte_01		155 ps
nib_07	219 ps	221 ps	byte_02		189 ps
nib 08	221 ps	223 ps	byte_03		197 ps
nib_09	217 ps	219 ps	byte 04 18	8 ps 173 ps	
nib_10	220 ps	222 ps	byte 05	200 ps 151 ps	
nib_11 💻	221 ps	223 ps	byte 06	209 ps 147	7 ps
nib_12 📕	218 ps	218 ps	byte 07	181	ps 175
nib_13 📒	227 ps	227 ps	bycc_or		
nib_14 📕	215 ps	215 ps			
-16 45	227 ps	227 ps			
nib_15			Conselemented	bb TO -!	-1
nib_15			Complex read	pattern, F0 ri	-
			Complex read	pattern, FO ri 142 ps	-
	attern, F0 fallin				144
			nib_00 nib_01	142 ps	144
ple read pa	attern, F0 fallin	ig edge	nib_00 nib_01 nib_02	142 ps 139 ps	144 141 138 p
ple read pa	attern, FO fallin 148 ps	ng edge	nib_00 nib_01 nib_02 nib_03	142 ps 139 ps 135 ps	144 141 138 p 145
ple read pa nib_00 nib_01	attern, FO fallin 148 ps 146 ps	148 ps	nib_00 nib_01 nib_02 nib_03 nib_04	142 ps 139 ps 135 ps 145 ps 142 ps	144 141 138 p 145 142
ple read pa nib_00 nib_01 nib_02	attern, FO fallin 148 ps 146 ps 144 ps	ng edge 148 ps 146 ps 146 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps	144 141 138 p 145 142 142
nib_00 nib_01 nib_02 nib_03	148 ps 146 ps 146 ps 144 ps 140 ps	g edge 148 ps 146 ps 146 ps 140 ps 140 ps 118 ps 118 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06	142 ps 139 ps 135 ps 145 ps 142 ps 142 ps 148 ps 148 ps 140 ps	144 141 138 p: 145 145 142 148
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06	attern, FO fallin 148 ps 146 ps 144 ps 140 ps 180 ps 131 ps 147 ps	148 ps 148 ps 146 ps 146 ps 140 ps 140 ps 118 ps 131 ps 147 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_06	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 140 ps 144 ps	144 141 138 p: 145 142 148 142 p 144
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07	148 ps 148 ps 144 ps 144 ps 140 ps 140 ps 131 ps 147 ps 142 ps	148 ps 148 ps 146 ps 146 ps 140 ps 140 ps 131 ps 131 ps 131 ps 144 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 140 ps 140 ps 144 ps 135 ps	144 141 138 p 145 142 142 142 144 144
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_05 nib_06 nib_07 nib_08	148 ps 148 ps 146 ps 146 ps 140 ps 140 ps 140 ps 147 ps 147 ps 147 ps 147 ps 147 ps 147 ps 148 ps	ng edge 148 ps 146 ps 140 ps 118 ps 118 ps 131 ps 147 ps 138 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_06	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 140 ps 140 ps 144 ps 135 ps 138 ps	144 141 138 p 145 142 142 142 144 135 138
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_06 nib_07 nib_08 nib_09	144 ps 146 ps 146 ps 144 ps 140 ps 140 ps 131 ps 147 ps 147 ps 147 ps 147 ps 147 ps 147 ps	g edge 148 ps 146 ps 146 ps 140 ps 140 ps 118 ps 131 ps 144 ps 138 ps 138 ps 144 ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 140 ps 140 ps 144 ps 135 ps	144 141 138 p 145 142 142 144 142 144 135 138 133 p
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_06 nib_07 nib_08 nib_09 nib_10	Attern, FO fallin 148 ps 146 ps 146 ps 146 ps 146 ps 147 ps 147 ps 142 ps 148 ps 148 ps 148 ps	g edge 148ps 146ps 146ps 140ps 118ps 118ps 118ps 144ps 138ps 138ps 138ps	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_08 nib_09	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 140 ps 140 ps 144 ps 135 ps 138 ps	144 141 138 p 145 142 142 142 144 135 138 133 p 138 p
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_08 nib_09 nib_10 nib_11	144 ps 144 ps 144 ps 144 ps 144 ps 148 ps 118 ps 147 ps 147 ps 142 ps 144 ps 144 ps 144 ps 144 ps 144 ps 144 ps 145 ps 145 ps	g edge 148.05 146.05 146.05 140.05 140.05 140.05 140.05 141.05 144.05 144.05 144.05 133.05 135.05 135.05	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_09 nib_09 nib_09	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 148 ps 148 ps 144 ps 144 ps 135 ps 136 ps 138 ps	144 141 138 p 145 142 142 142 144 135 138 133 p 138 p
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_09 nib_10 nib_10 nib_12	148 ps 148 ps 148 ps 149 ps 149 ps 149 ps 147 ps 147 ps 142 ps 148 ps 14	ng edge 148pt 146pt 146pt 146pt 180pt 180pt 181pt 181pt 184pt 184pt 184pt 184pt 184pt 184pt 184pt 184pt 184pt 184pt	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_09 nib_10 nib_11	142 ps 139 ps 135 ps 145 ps 142 ps 148 ps 148 ps 140 ps 144 ps 135 ps 138 ps 139 ps	144 141 138 p 145 142 142 144 135 138 133 p 138 p 138 p 138 p 138 p
ple read pa nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_08 nib_09 nib_10 nib_11	144 ps 144 ps 144 ps 144 ps 144 ps 148 ps 118 ps 147 ps 147 ps 142 ps 144 ps 144 ps 144 ps 144 ps 144 ps 144 ps 145 ps 145 ps	g edge 148.05 146.05 146.05 140.05 140.05 140.05 140.05 141.05 144.05 144.05 144.05 133.05 135.05 135.05	nib_00 nib_01 nib_02 nib_03 nib_04 nib_05 nib_06 nib_07 nib_08 nib_09 nib_10 nib_10 nib_11 nib_11	142 ps 139 ps 135 ps 145 ps 145 ps 142 ps 140 ps 140 ps 135 ps 138 ps 138 ps 139 ps 140 ps	144 141 138 p: 145 145 142 148

nib 00	135 ps	135 ps
nib 01	140 ps	142 ps
nib 02	124 ps	126 ps
nib 03	126 ps	128 ps
nib_04	118 ps	120 ps
nib_05	119 ps	119 ps
nib_06	134 ps	134 ps
nib_07	138 ps	138 ps
nib_08	119 ps	119 ps
nib_09	130 ps	132 ps
nib_10	113 ps	113 ps
nib_11	116 ps	116 ps
nib_12	118 ps	118 ps
nib_13	110 ps	113 ps
nib_14	135 ps	135 ps
nib 15	137 ps	139 ps

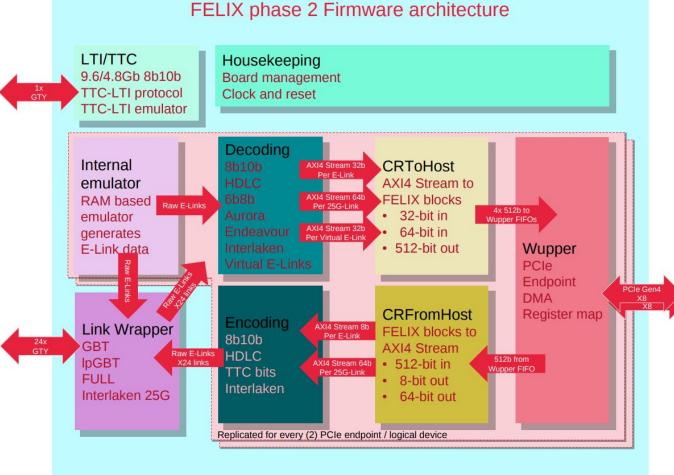
Complex write pattern, F0

byte_00	161 ps 151 ps
byte 01	153 ps 145 ps
byte_02	164 ps 144 ps
byte_03	159 ps 142 ps
byte_04	167 ps 133 ps
byte_05	163 ps 144 ps
byte_06	166 ps 141 ps 17
byte 07	169 ps 135 ps

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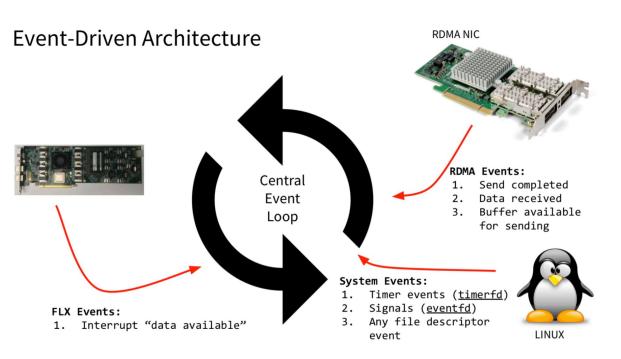
FELIX 182 Firmware

- Interface for Trigger/Control/Timing for both LTI/TTC
 - LTI distributes the LHC clock/trigger/control information to FELIX
 - FELIX redistributes clock to front-end electronics using GBT, IpGBT or LTI-FE format
 - Some sub-detectors need clock distribution with < 5 ps precision - achieved with additional phase detector (DDMTD) that ensures consistent startup phase determination
- Link Wrapper sends/receives data
- Encoding/Decoding blocks support lpGBT & 25 Gb/s & Interlaken
 - IpGBT e-links support 6b8b, 8b10b, HDLC, Aurora & Endeavour
- Wupper provides interface to PCIe DMA core (2 PCIe endpoints per card)
 - Supports Gen4 & Gen5
 - Internal emulator generates e-link data for testing fw blocks



FELIX Software

- Access to the FELIX hardware controlled via device drivers
- Basic configuration/monitoring (f-tools suite, e-link configuration, felix-monitoring)
- Felix-star readout application
 - Parallel readout of up to 10 DMA buffers per PCIe cards
 - Uses RDMA network technology for high-throughput, low-overhead data transfers
 - Will support TCP/IP for monitoring/slow control traffic
 - A simple API provides network protocol agnostic interface
 - Dataflow for Detector Control System has dedicated buffers/threads and uses TCP/IP rather than RDMA

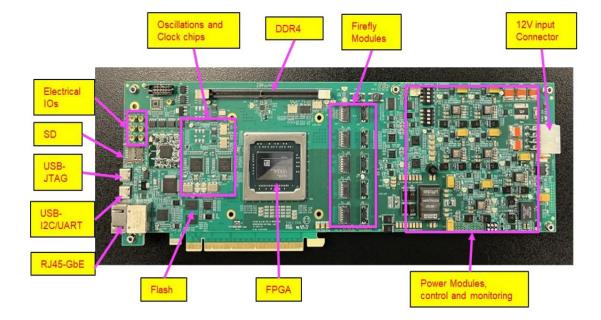


Prototyping status & Integration

- Successfully tested the first FLX-182 prototypes
- 10 FELIX 182 prototypes are in production and will be ready in Fall of 2023 for integration/testing with sub-detectors
- Operation with FELIX fw at PCIe Gen4 speeds was verified
- Integration with ATLAS Global Trigger has been successfully tested
- BIST features demonstrated
- FELIX also used in ProtoDUNE SP, NA62, sPHENIX, SPIDR4







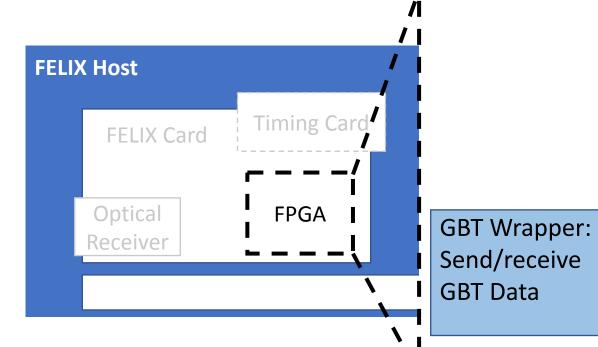




- FELIX for Phase I ATLAS upgrades was installed and commissioned successfully
- FELIX for Phase II ATLAS under development
- Support for FLX-182 firmware and software under development
- Early prototypes tested successfully, more coming in Fall of 2023

Backup

FLX-712 Fw

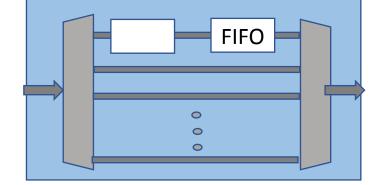


GBT Mode: 24 bi-directional radiation-hard, GBT links (4.8Gb/s – 3.2Gb/s with error correction)

FULL Mode: 12 links, custom light-weight protocol from front-end-path (9.6Gb/s) TTC & BUSY: Decode trigger data and recover LHC clock

Central Router: Map GBT data to E-link format

Demultiplex GBT link into data streams, decode data stream (8b/10b or HDLC), form 1 kbyte blocks read by DMA



Wupper PCIe/ DMA Engine: Push data to the memory