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FLX-182, the hardware platform for ATLAS readout during High Luminosity LHC

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FLX-182 is a PCIe card designed for the readout system of the ATLAS experiment for the High Luminosity phase of LHC starting in 2029. FLX-182 is responsible for decoding and transferring data from the front-ends into the host server memory, and receiving and distributing timing, trigger and control information. About six hundred FLX-182 will sustain 4.6 TB/s of total throughput at 1 MHz data rate. FLX-182 is equipped with a Xilinx Versal Prime VM1802 SoC, a PCIe Gen4x16 interface and can operate up to 24 optical links at 25 Gb/s. FLX-182 runs firmware capable of interfacing with all different subdetectors.

Summary (500 words)

The FELIX readout system has been added to the data acquisition system of the ATLAS experiment at the LHC in the data-taking period called Run3 (2021-2025) and serves at present a subset of the ATLAS sub-detectors.

An evolved version of FELIX, dubbed Phase-II, will be deployed in Run 4 (2029 –2032) and will serve all ATLAS subdetectors. FELIX Phase-II will sustain a data rate (1 MHz) ten times higher than that of Run 3 and a total throughput of 4.6 TB/s. The entire system will comprise about 300 servers, each equipped with custom PCIe FELIX cards and 400 GbE network interfaces. In addition to performing high-throughput and low-latency readout, FELIX will distribute to/from the detector front-ends timing, trigger and control (TTC) information, as well as monitoring and configuration. Multiple direct-memory-access buffers on the host will permit the separation of different streams in the FELIX software and firmware.

At the core of the FELIX system is the custom PCIe card. The Phase-II FELIX card is called FLX-182 and is equipped with a Xilinx Versal Prime VM1802 SoC, a PCIe Gen4x16 interface and 24 optical links that operate at a speed up to 25 Gb/s. Four additional 25 Gb/s links allow to communicate with the TTC system, or, alternatively, to implement a 100 GbE interface. A flash memory is used to store firmware images.
A few firmware variants have been developed to support the different communication protocols adopted by sub-detectors as well as specific features. Communication protocols include lpGBT and GBT, used by the lpGBT [1] and GBTX [2] radiation-hard ASICs for front-end electronics, as well as simpler 8b10 or Interlaken encoding for FPGA-to-FPGA communication. FLX-182 prototypes have been built and are undergoing integration tests. Quality-check software run on the SoC has been developed, while readout software is under development.

[1] http://lpgbt-fpga.web.cern.ch
[2] https://espace.cern.ch/GBT-Project

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