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CMS Level-1 trigger Data Scouting firmware prototyping for LHC Run-3 and CMS Phase-2

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A novel Data Acquisition (DAQ) system, known as Level-1 Data Scouting (L1DS), is being introduced as part of the Level-1 (L1) trigger of the CMS experiment. The L1DS system will receive the L1 intermediate primitives from the CMS Phase-2 L1 trigger on the DAQ-800 custom boards, designed for the Phase-2 central DAQ. Firmware is being developed for this purpose on the Xilinx VCU128 board, with features similar to one half of the DAQ-800, and validated in a demonstrator for LHC Run-3. This contribution describes the firmware development in view of the target design for the DAQ-800.

Summary (500 words)

A novel Data Acquisition (DAQ) system, known as Level-1 Data Scouting (L1DS), is being introduced as part of the Level-1 (L1) trigger of the CMS experiment. The L1DS is complementary to the central CMS DAQ and it captures the L1 intermediate primitives produced by the trigger processors at the full 40 MHz bunch crossing rate. The system will provide vast amounts of data for multiple purposes, such as trigger diagnostics, luminosity measurements and the study of otherwise inaccessible signatures, either too common to fit in the L1 accept budget, or with requirements orthogonal to the standard physics triggers. For the High-Luminosity LHC upgrades, the L1DS system will receive the L1 intermediate primitives from the upgraded L1 trigger, capable of sophisticated feature searches with resolution often similar to the offline reconstruction. The DAQ-800 custom boards, designed for the CMS Phase-2 central DAQ and with an ATCA form-factor, will be used to collect data from the L1 processors over high-speed optical links. The DAQ-800 board is capable of accepting up to 48 L1 input links for a total of 1.2 Tb/s. The maximum theoretical output bandwidth being 1 Tb/s, a moderate data reduction will be necessary to allow the board to operate at a steady output data rate of 800 Gb/s. The data pre-processing logic will be implemented on the two Xilinx Ultrascale+ VU35P FGPAs hosted on the board and chosen for their built-in High-Bandwidth Memory (HBM). The latter is required for the central DAQ unit to provide sufficient data buffering between the LHC-synchronous back-end and COTS switched network, relaying data to standard compute servers. The L1DS will use a custom firmware implementation of the TCP/IP protocol on the DAQ board FPGAs, to transfer L1 primitives to a set of data servers, where they will be stored in memory prior to being sent to a computing farm for the final processing. The L1DS firmware is being developed on the VCU128, a Xilinx development board with features similar to one half of the DAQ-800 boards. The development is currently being validated in the LHC Run-3 demonstrator of the L1DS, which captures the primitives from the Global Muon Trigger (GMT) and Calorimeter Trigger, the trigger decision bits from the Global Trigger output and the input stubs to the Barrel Muon Track Finder (BMTF). Additionally, machine learning inference applications can be deployed directly on the FPGA to enhance the analysis capabilities of the L1DS. This contribution describes the scouting firmware development carried on the VCU128 board in view of the Phase-2 target design for the DAQ-800 custom board.

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