Contribution ID: **123** Type: **Oral**

SystemC framework for architecture modelling of electronic systems in future particle detectors

Tuesday 3 October 2023 11:20 (20 minutes)

The prototyping cost in advanced technology nodes and the complexity of future detectors require the adoption of a system design approach common in industry: design space exploration through high-level architectural studies to achieve clear and optimized specifications.
This contribution proposes a configurable SystemC framework to simulate the readout chain from the front-end chips to the detector back-end. The model is transaction accurate, includes an event generator and interfaces with real physics events, and provides metrics such as readout efficiency, latency, and average queue occupancy.
This contribution details the structure of the framework and describes a case study based on Velopix2.

Summary (500 words)

The CERN EP department has launched a strategic R&D programme on technologies for future experiments. In this context, the IC technology work package, namely WP5, is working on the development of a simulation framework for architectural modelling of future particle detectors.
This work focuses on the modelling of pixel-based detector from front-end to back-end at a high level of abstraction to perform architectural studies. The objective is to study the readout network efficiency as well as to provide the metrics to compare different solutions to satisfy functional and non-functional requirements, such as data throughput, data quality, downlink material cost, and other parameters both detector-wise and at ASIC level. At the same time, it can provide a reference model for HDL code design and verification. For this reason, an important feature is support for co-simulation of the high-level architectural model and the RTL model.
The framework proposed in this contribution is built in SystemC, a system-level specification and design language based on C++ classes that has been widely adopted in industry for high-levels of abstraction modelling, such as system-level simulations. The SystemC language is open-source, supports TLM2.0 standard, allows RTL co-simulation and can be integrated with UVM-based verification environments, and is developed by a wide consortium of companies in several industrial domains, most prominently computer aided design (CAD) companies.
The framework provides two main component modules: a layer and a network. The layer module contains the processing logic, whereas the network module instantiates the connectivity among different layer modules. This structure enables code re-use while writing models for different systems. Information transmission is modelled via packet transfer, where a packet represents the data that the system is processing. An example would be hit data transferred in a pixel chip. Packet transfers are based on TLM2.0 sockets providing different abstraction levels depending on the needs of the project. The stimuli can be internally generated with full control on event occupancy, cluster size and shape, and any other data characteristic, therefore allowing parametrized studies. On the other hand, the framework also provides methods to interface with externally generated events to assess performance with data deriving from physics-level detector simulations.
The first study case for the proposed framework was the Velopix2 LHCb detector. In this context, the front-end chip design team is developing a chip architecture able to cope with pixel rates up to 350 kHz/pixel. The initially proposed architecture has been modelled and simulated with physics data proving that the readout

architecture was unable to provide sufficient readout efficiency. The framework enabled collection of metrics to be used in a per-layer bottleneck analysis based on average queue occupancy and packet transfer rate. Such analysis revealed the limitations of the initially proposed architecture and how to revise it.
In conclusion, the proposed framework provides a tool for early architectural analysis, helping both front-end chips designers and system developers to have a comprehensive view of the performance of the detector under development as well as a consistent reference model for the RTL development and verification.

Primary authors: PULLI, Adithya (CERN); CERESA, Davide (CERN); BRAMBILLA, Francesco Enrico (EPFL - Ecole Polytechnique Federale Lausanne (CH)); DHALIWAL, Jashandeep (CERN); KLOUKINAS, Kostas (CERN); ESPOSITO, Stefano (CERN); LLOPART CUDIE, Xavi (CERN)

Presenter: CERESA, Davide (CERN)

Session Classification: Programmable Logic, Design and Verification Tools and Methods

Track Classification: Programmable Logic, Design and Verification Tools and Methods