Contribution ID: **37** Type: **Oral**

Verification Environment for ALTIROC ASIC of the ATLAS High Granularity Timing Detector

Tuesday 3 October 2023 11:40 (20 minutes)

ALTIROC3 is the second version of the ASIC for the ATLAS High Granularity Timing Detector to read out full size LGAD sensors (15x15 pixels of 1.3mm x 1.3mm). The ASIC, designed in 130nm technology, comprises around 250k flip-flops, more than 1000 8-bit configuration registers, and several clock domains and implements different analog IP-blocks critical for digital data acquisition and processing. This contribution presents the verification approach and tools employed, including a new System Verilog verification environment based on Universal Verification methodology (UVM) for functional, power and SEE verification, complemented with formal verification for Clock Domain Crossing (CDC) and Reset analysis.

Summary (500 words)

ALTIROC ASIC of the ATLAS High Granularity Timing Detector (HGTC) is required for the High Luminosity LHC where there will be a large increase in pile-up. The ASIC will provide luminosity measurement at each Bunch Crossing (BC) and precision timing information with 20 ps resolution for Time-Of-Arrival (TOA) and 40 ps resolution for Time-Over-Threshold (TOT) only upon reception of a trigger.

ALTIROC3 ASIC followed a Digital-on-Top approach in order to enable digital tools capabilities in constraining, designing and better verifying the ASIC reducing the Turn-Around-Time (TAT) of the design flow.

Taking advantage of the automatization and reproducibility of the design and verification flows, a new System Verilog verification environment based on Universal verification Methodology (UVM) has been developed to cover all intended functionalities of the design at full chip level to give the designers enough confidence before submission.

The objective of the new verification environment has been to verify the full chip using digital tools. For the first time, analog IP blocks have been characterized with cycle accurate Verilog models that represent a breakthrough for a more comprehensive mixed-signal full chip functional verification.

For instance, the modeling of the analog front-end together with the two TDCs allowed stimulating the hit sampling digital logic in unexpected ways. The verification framework provided assistance to verify the chosen architecture.

The functional verification of critical interfaces between analog world and digital world consisted in verifying not only the behavior of the analog IP block, but also the how they have been integrated in the Digital-on-Top implementation.

The new UVM verification environment comprises reusable UVM Verification Components (UVC), register abstraction layer (RAL) block for the configuration and design specific verification components to assist the design phase and to stimulate the design efficiently exploiting constrained randomization and functional coverage collection.

The high number of clock domains present in the ASIC, together with the complex clock and reset architecture, required to complement the classical functional verification approach with formal methods, whose performances are necessary to exhaustively prove the correctness of the design.

Moreover, the verification environment developed for ALTIROC3 has also been helpful to assist power verification, namely IR drop and dynamic power consumption, and extensively used to verify SEE at RTL level and on the final netlist.

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Session Classification: Programmable Logic, Design and Verification Tools and Methods

Track Classification: Programmable Logic, Design and Verification Tools and Methods