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Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System

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The ALICE collaboration is developing the new Inner Tracker System 3 (ITS3), a novel detector that exploits the stitching technique to construct single-die monolithic pixel sensors of up-to 266 mm x 93 mm. ITS3 requires all hits from a particle flux of 4.4 MHz/cm2 to be transmitted on-chip to one of the sensor edges. This on-chip readout is limited by a power budget of 20 mW/cm2, a readout inefficiency of <2.5×10−3 and ≤10 % dead area. The model of ITS3 on-chip readout architecture will be presented, used to optimize the data flow implementation limited by physical and power budget constraints.

Summary (500 words)

The ALICE collaboration is developing the Inner Tracker System 3 (ITS3), a new detector that aims to replace the three innermost layers of the tracking system during LHC's Long Shutdown 3. The detector consists of three cylindrical layers, with each half-cylinder made of a single-die monolithic pixel sensor bent towards the beam pipe. They are developed using a commercial 65 nm CMOS Imaging technology with dimensions up-to 266 mm x 93 mm. This can be achieved by profiting from the stitching technique, which allows the manufacturing of modular chips larger than the design reticle.

The expected Pb-Pb interaction rate is 100 kHz, which generates a particle flux in the innermost layer of 4.4 MHz/cm2. With a pixel pitch of ˜20 µm, up to 4 pixels per incident particle are hit, yielding an occupancy of 8 × 10−4. The shipment of these hits follows a continuous trigger-less solution, where all hits detected during a pre-defined integration period of 2 µs, 5 µs, or 10 µs are read together in frame packets. If the number of pixel hits during the integration period is too high, the readout frame is assembled incomplete. The fraction of incomplete frames define the performance of the readout architecture. This readout architecture must achieve a fraction of incomplete frames below 2.5 × 10−3, a power density below 20 mW/cm2, and a dead area lower than 10%.

To optimize the readout architecture and buffer sizes, a behavioral model was designed in System Verilog. This module emulates the components and requirements of the ITS3 readout. Each ITS3 sensor is composed of independent Stitched Units. These Stitched Units are made abutting 12 Repeated Sensor Units (RSU), and 2 end-caps (Figure 1). The RSUs contain the sensitive area of the chip. Each RSU contains 12 power units with independent readout architectures. These readout architectures read in parallel different regions of the sensitive area into on-chip memories to cope with particle fluctuations (Figure 2). The hits stored in these memories are sent in frame packets to the left end-cap, which hosts the only off-chip data connection. The model was tested using random data and physics data extracted from LHC behavior. This data takes into consideration the centrality of the collisions, the pile-up of different collisions in one integration period, the QED electrons generated from electromagnetic interactions, and different cluster sizes.

This submission will explain in detail the methodology, results, and learnings obtained from using the model. The optimized Stitched Unit requires 144 links of 160 Mbit/s, 432 on-chip memories with 15-bit width, and 128-word depth. Apart from these definitions, this study provides key learnings for the readout architecture implementation such as the correlation between losses and collisions pile-up, or the best ordering for reading the memories inside the power units.

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