The CMS HGCAL trigger data receiver

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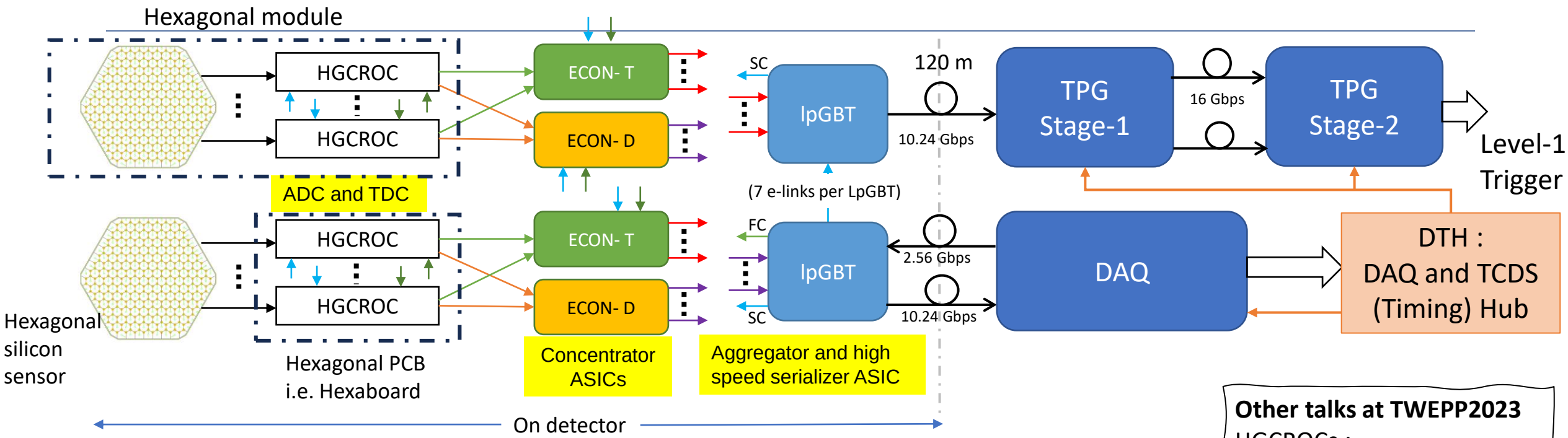
On behalf of the CMS Collaboration

TWEPP 2023

HGCAL
Back-End Group

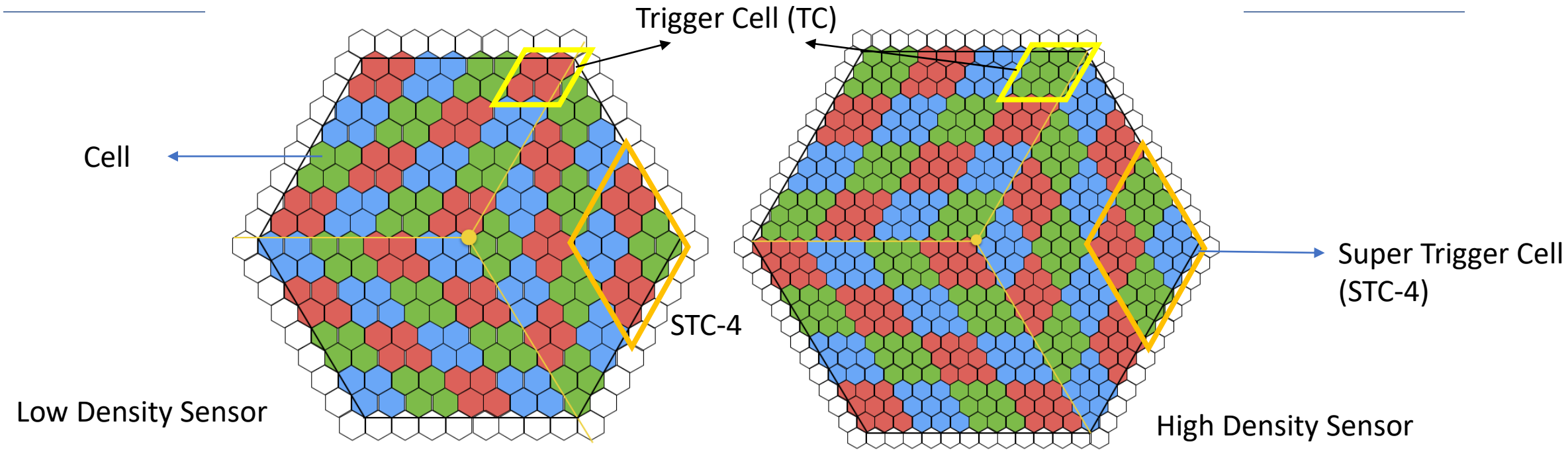
HGCAL Readout



- Large number of links: ~10k DAQ and Trigger LpGBTs (Low-power Gigabit Transceiver)
- Asymmetric design
  - DAQ path provides configuration, control and event readout
  - TPG (Trigger Primitive Generator) path is readout only (streaming @ 40 MHz)
  - Stage-2 is time multiplexed (18)
- All BE subsystems are envisaged to be implemented on common ATCA baseboard (Serenity) and common infrastructure firmware - EMP firmware framework

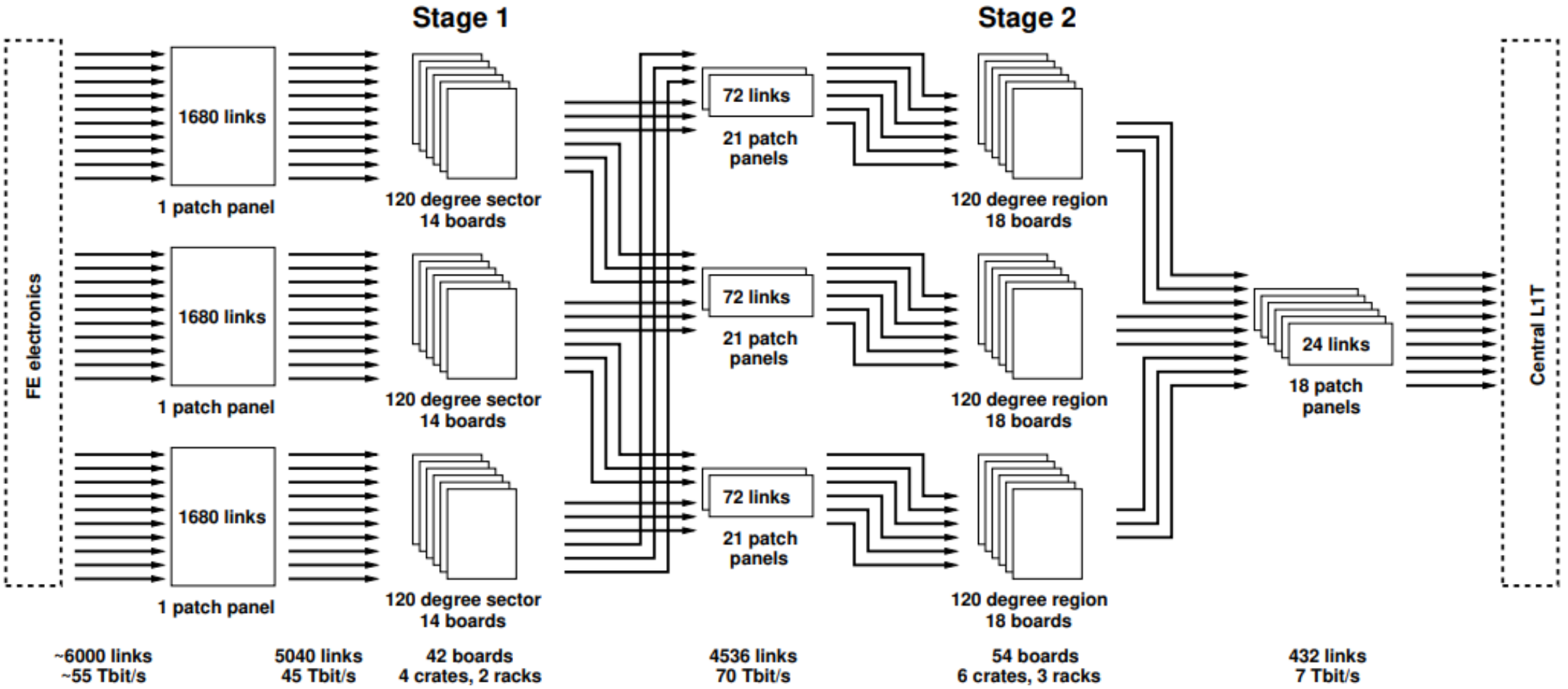
Other talks at TWEPP2023
HGCROCs :
https://indi.to/rsMvb
ECONs:
https://indi.to/j7qmQ
Serenity:
https://indi.to/WP7mx
Si Sensor tests:
https://indi.to/qmM36
Vertical Integration (poster):
https://indi.to/jxK6D

Some definitions

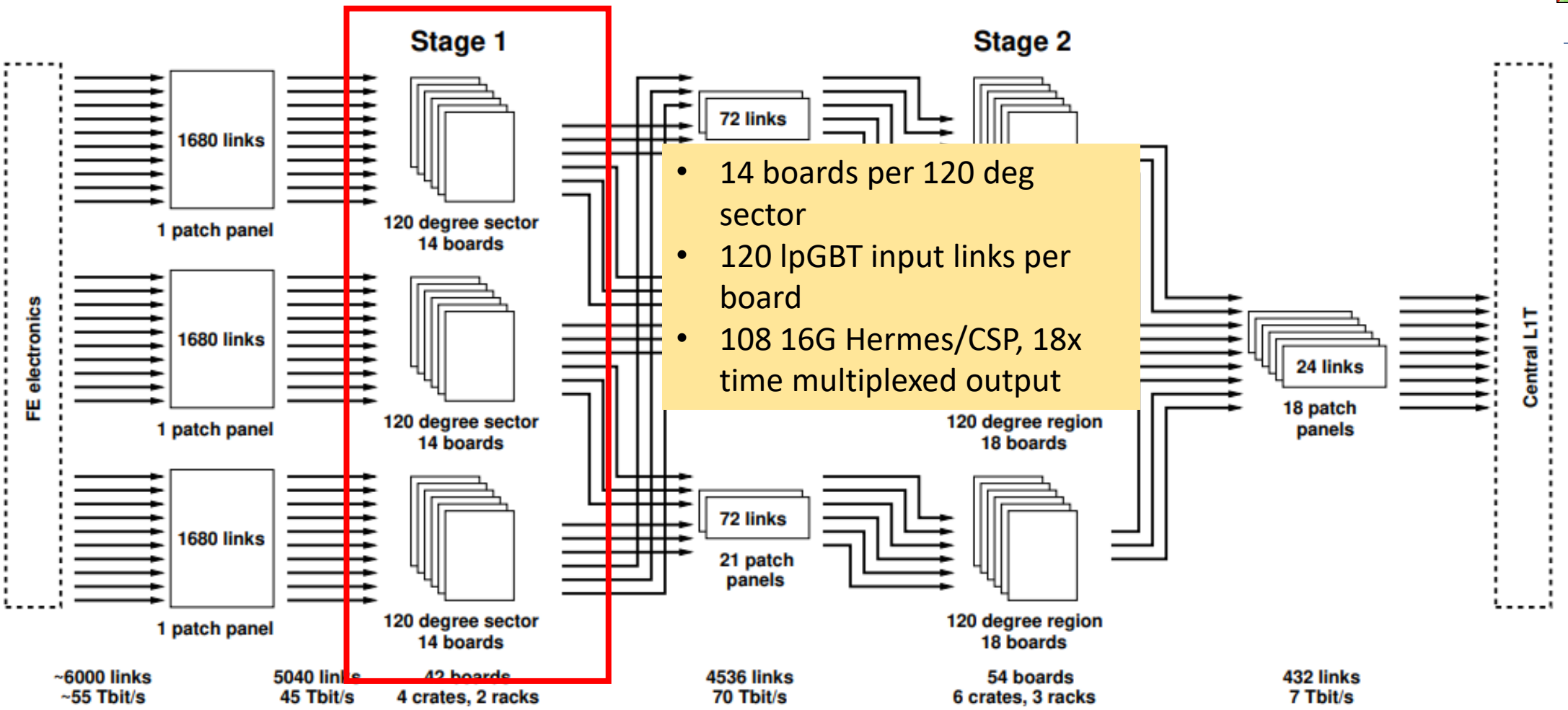


- Figure above shows two HGCAL silicon sensors with different hexagonal cell sizes
  - 1.18 cm^2, sensor cells for LD (left), and for the small, 0.52 cm^2 for HD (right)
- HGCROC (readout chip) samples each cell from the sensor (charge and timing), and these are readout using DAQ path
- HGCROC also computes (addition of charge) a coarser unit i.e. collection of 2x2 or 3x3 cells to form a Trigger Cell (TC) – these propagate through trigger path
- The concentrator ASIC calculates sum of energies for whole module (Module Sum) and Super Trigger Cells i.e. cluster of TCs when setup accordingly

TPG architecture

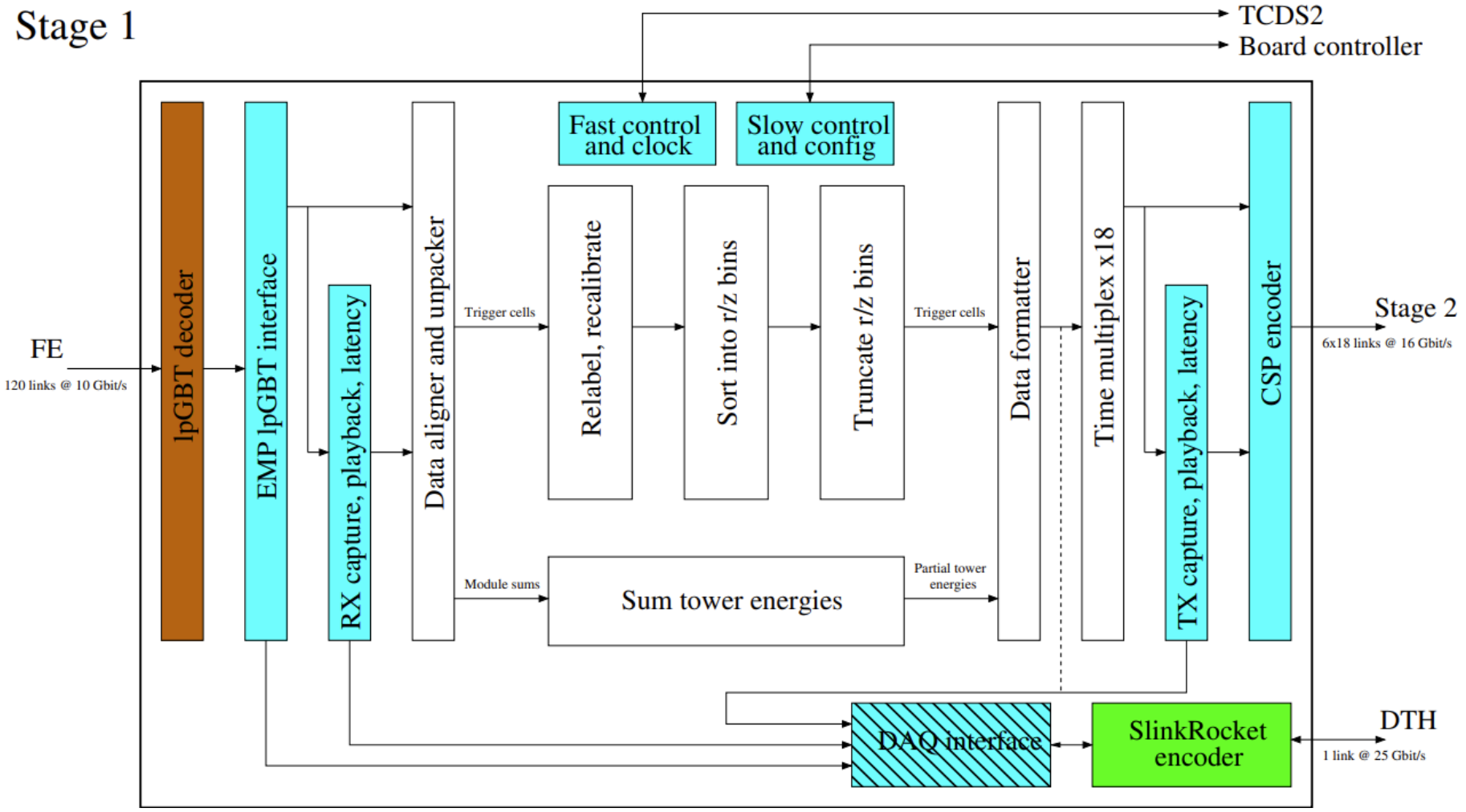


TPG architecture



- 14 boards per 120 deg sector
- 120 lpGBT input links per board
- 108 16G Hermes/CSP, 18x time multiplexed output

The CMS HGCAL trigger data receiver: Stage -1



- Block diagram shows firmware organization for *one stage-1 board*
- Collaboration of
  - Imperial College
  - LLR
  - Univ. Split
  - Univ. Maryland

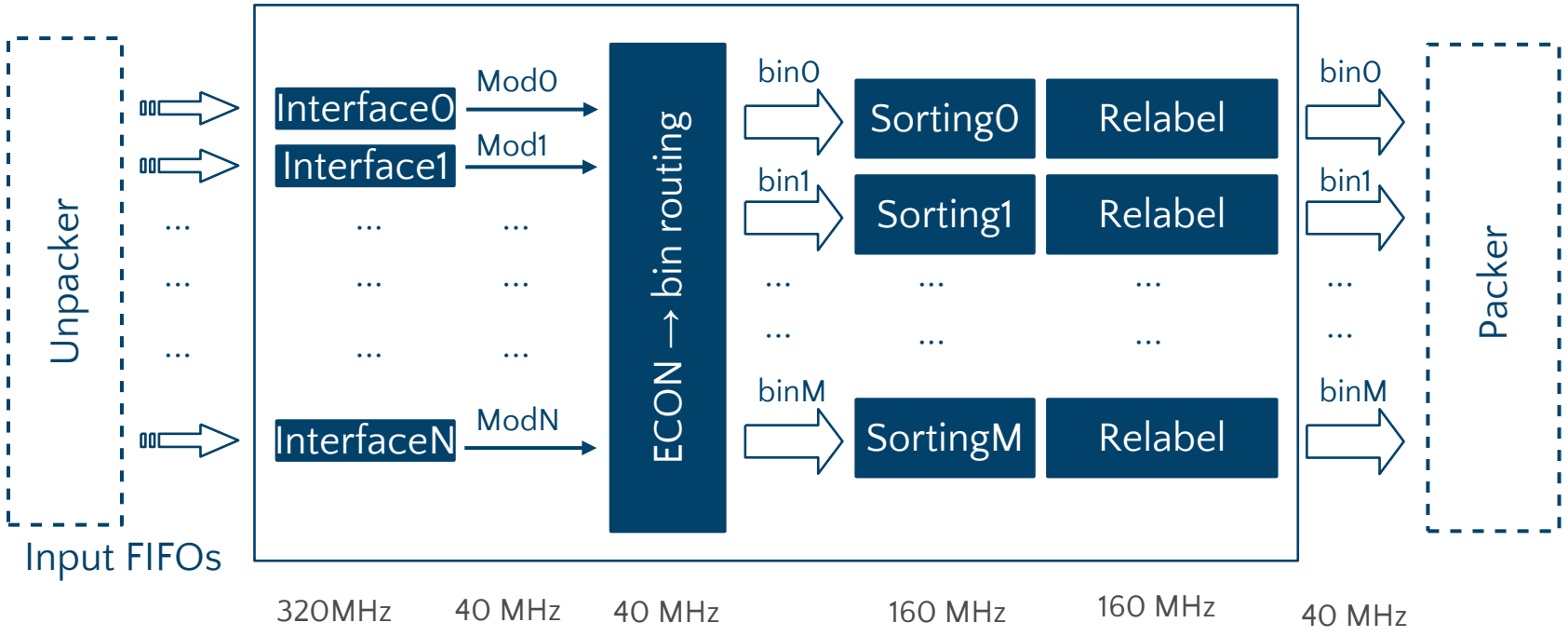
Colored boxes indicate shared firmware infrastructure (EMP/CMS/CERN)

ECON-T unpacker (data receiver)

- Challenges
  - Decode the ECON-T packet and present decoded data in simple and unified format to downstream blocks
  - Decoding threshold-sum (TS) packet is particularly challenging due to its variable latency and variable length format
  - Should be able to do this using very small FPGA resources since each Stage-1 FPGA deals with about 260 modules
- Firmware implemented for three ECON-T algorithms
  - Threshold Sum (TS)
  - Best Choice (BC)
  - Super Trigger Cell (STC)

  } Fixed size formats
- Current baseline uses combination of BC and STC in the front and back, respectively, of the HGCAL

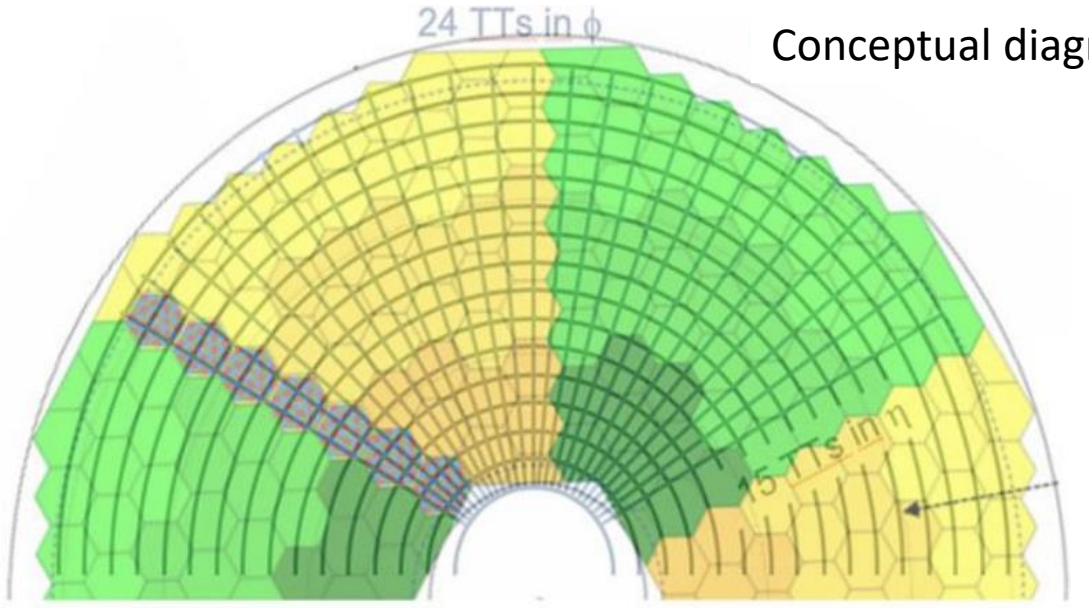
TC processor



- Interface with the unpacker: flattening trigger cell streams from input FIFOs
- Routing trigger cells in each modules into r/z bins
- Sorting and truncation of the trigger cells in each bin
- Relabeling of the trigger cells

Tower Sum: Input and Outputs

- INPUTS – data from 120-degree sector
  - 260 modules with 8-bit values in 5E/3M floating point format
    - Each input represents sum of TC energies from one module
  - 260 2-bit inputs
    - Needed for calibration
- OUTPUTS – sums of input energies
  - Outputs two arrays of Trigger Tower sums
    - CE-E (428) and CE-H (515)
    - Actual number of active towers are board dependent
  - Each output represents sum of input energies belonging to the same TT
  - Total 943 8-bit values in 4E/4M format for one of the biggest design
- The STCs contain all the module data so module sums are formed from them, and no extra readout is needed



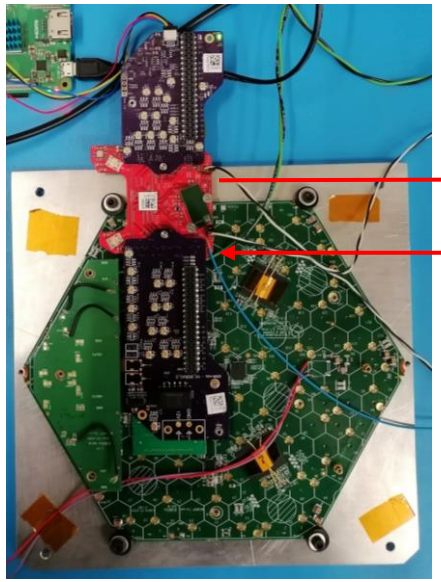
Conceptual diagram

360 towers / 120 deg

Bench-top testing

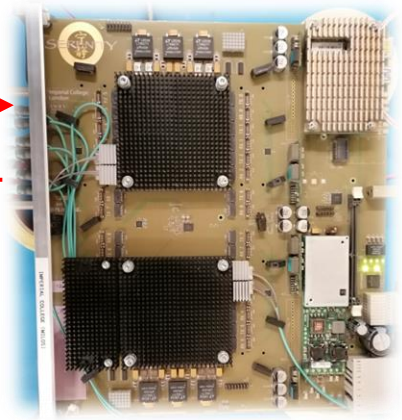
- Most of the firmware blocks have been tested individually using buffer playback mechanism of Serenity to inject data and record outputs
- About a year ago efforts started to integrate Serenity (BE design) with real front-end hardware
  - Benchtop test system of single Train was setup with HGCAL low density hexaboard, concentrator ASIC emulators and LpGBTs (the Engine)
  - The firmware was built around EMP firmware framework and greatly benefitted from common LpGBT infrastructure
  - Few other supporting blocks were developed (e.g. Fast Command generator) to thoroughly test the trigger path
  - ECON-T emulator was eventually replaced by ECONT-P1 ASIC

- **Front-end PCBs and ASICs**
  - Engine PCB
    - VTRX+
    - lpGBT
  - Wagon PCB
  - ECON Mezzanine PCB
    - ECON-T-P1
  - Hexaboard PCB
    - HGCROC
    - Rafael



Trigger (ECONT) and DAQ (ECOND) data

Timing, Slow Control and Fast Control



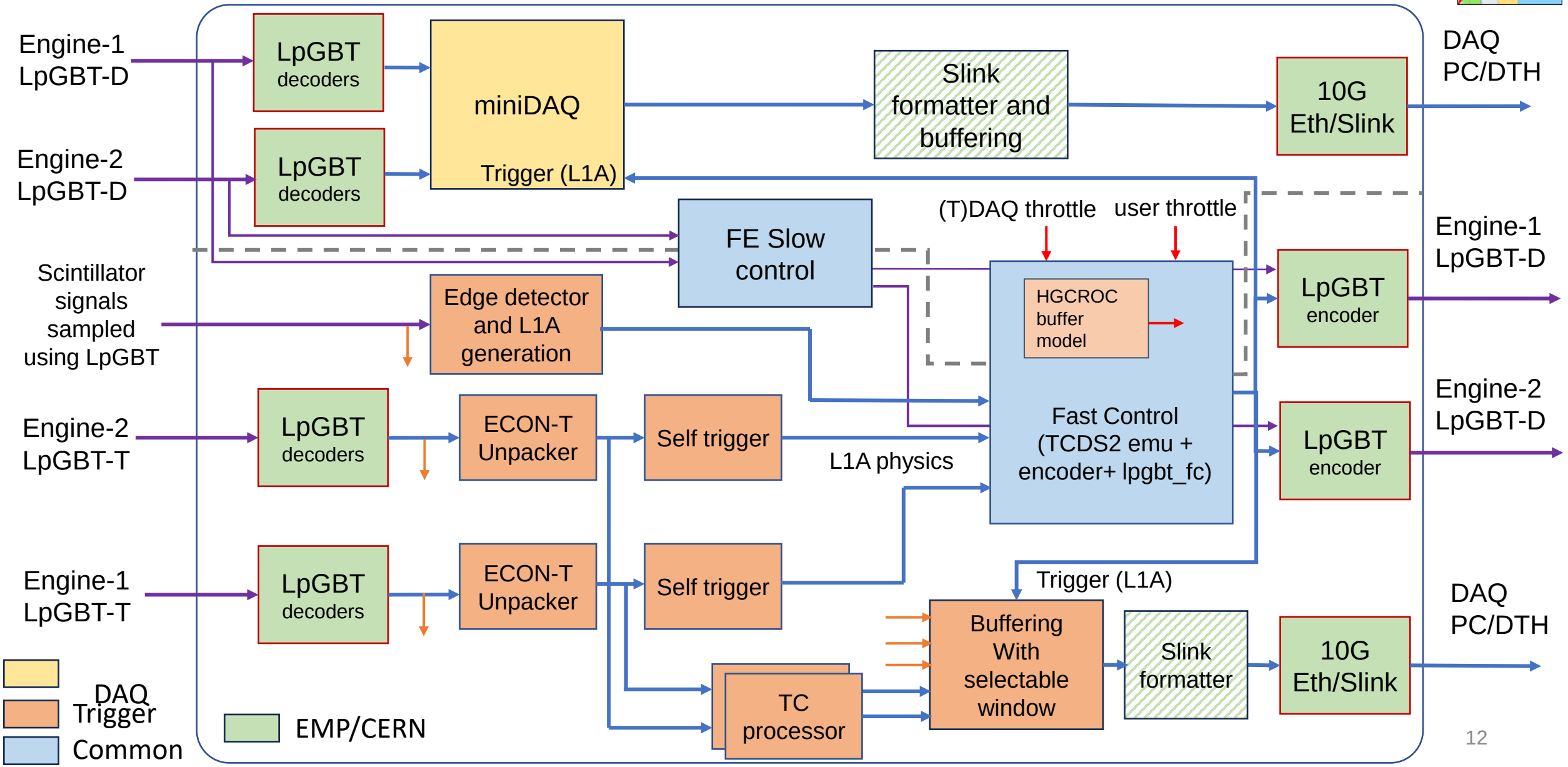
- **Back-end**
  - Serenity v1.1 ATCA board
  - KU15P FPGA daughter card
  - Firefly optics

Integrated architecture for test beam

- Efforts moved towards setting up integrated test-bench for the trigger and DAQ path ultimately leading to hardware setup for the beam tests
  - A special bridge PCB (Unicorn) was designed to enable us using ECON emulators in FE for the first beam test (Aug)
  - Combined mezzanine with ECON-D-P1 and ECON-T-P1 was available for the Sept beam test
- Integrated firmware was designed which consisted of many different processing blocks as well as ancillary blocks
  - ECON-T unpackers and TC processor
  - Self trigger generator for ECON-T unpackers
  - Latency and event buffers for trigger stream
  - miniDAQ (subset of full DAQ)
  - Readout mechanism for trigger buffers and miniDAQ (for 10G readout, later modified for DTH)
  - TCDS2-emulator to generate various fast command sequences including calibration sequences and triggers (Level-1 Accept signal)
  - External trigger processor
- Only Super Trigger Cell (4E3M) algorithm was used for the first beam test as ECON-T emulator did not support Best Choice (BC); BC was tested in Sept (second) beamtest

Integrated architecture for test beam: Block Diagram

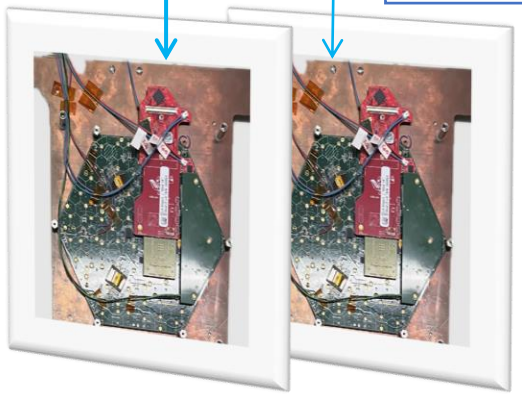
Serenity firmware



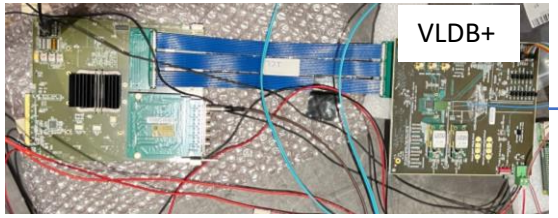
The whole chain – a vertical slice of *final* whole chain

MPO-24 cassette

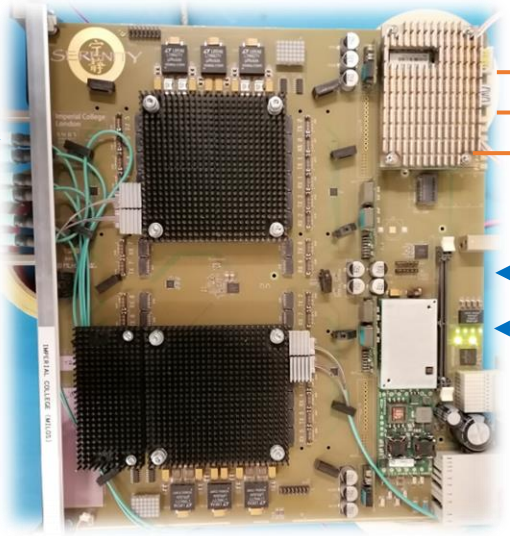
80m fiber



LD Modules with
- HGCROC 3As
- RAFEAL
- ECON-T-P1 + ECON-D-P1 combined mezzanine (Sept) / ECON emulators with bridge PCB (Aug)
- LD Engine (2 Trig LPGBT + 1 DAQ LpGBT)



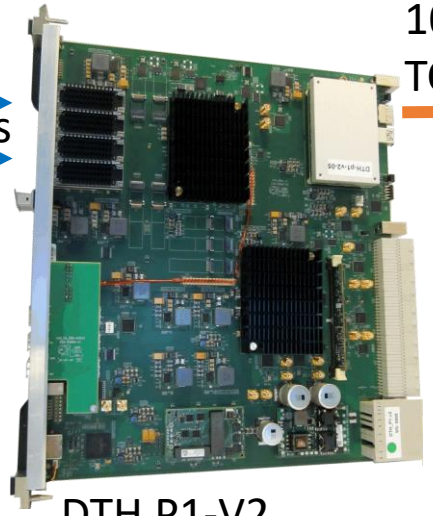
Scintillator signal (discriminated) sampling



Serenity v1.1

10G UDP/IP Links

25G Slinks



DTH P1-V2
(*only in Sept, some runs)

100G TCP/IP

DAQ PC

EOS and DQM

Slow Control, Fast control etc.

DAQ Software

DTH control

PSUs

Serenity

DTH

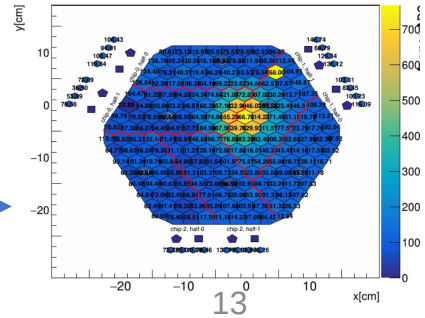
DAQ PC

Grafana monitoring

RUN CONTROL

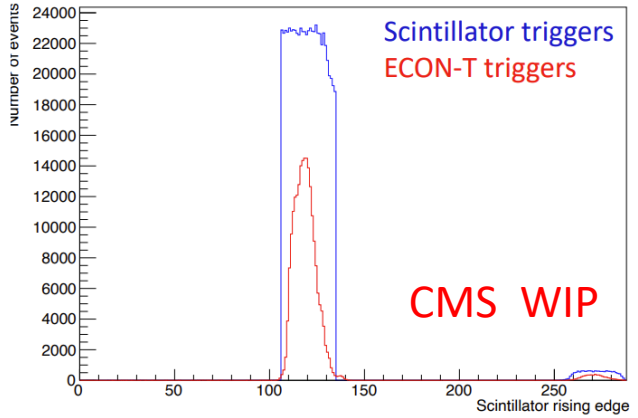
CMSSW DQM

Temperature, Humidity near sensor modules (cold box)



Operational challenges

- Configuring the FE ASICs
  - The front-end has four types of ASICs (e.g. HGCROC, ECONs, LpGBTs) which have many tunable parameters.
    - Subtilities in navigating different slow control interfaces behind LpGBT and signal integrity was crucial
    - Selecting just the right parameters for ASICs was an iterative process.
  - Each ASIC sends its processed data over a 1.28 GHz serial link to next ASIC.
    - Correctly aligning them and selecting the procedure (using different phase tracking modes) to keep the alignment intact also proved to be an important lesson
    - The link alignment also impacts which ECON-T event is ‘tagged’ as BC0. Correctly tagging the event while maintaining overall timing of the system (between DAQ and trigger) was tricky
- Timing in the DAQ data with trigger – matching L1’As
  - The internal calibration pulse (CALPULSE-INT) along with self triggering mechanism was key to timing in the system – fixed self trigger delay and HGCROC buffer depth
  - The scintillator delays were adjusted to match that of self trigger – completing whole chain
  - Finally, HGCROC sampling delays were adjusted to match both module timings
  - Uncertainly in timing resulting from different word-boundary settings at BE for the ECONT->LPGBT, during power cycling is yet to be understood completely

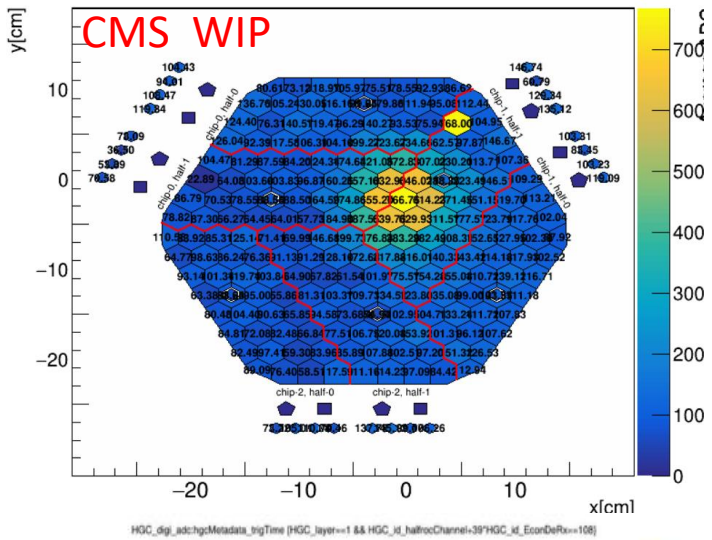


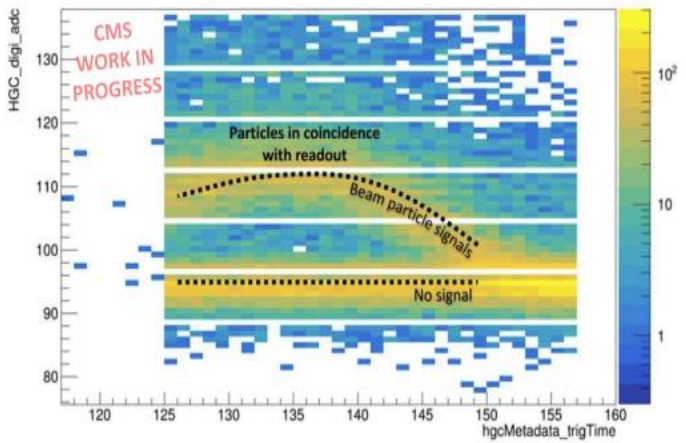
- Matching event tag (Event number, BX counter, Orbit Counter) across the system was eventually achieved after understanding some subtle behavior differences of FC decoder across the ASICs

Data !

DPG data set

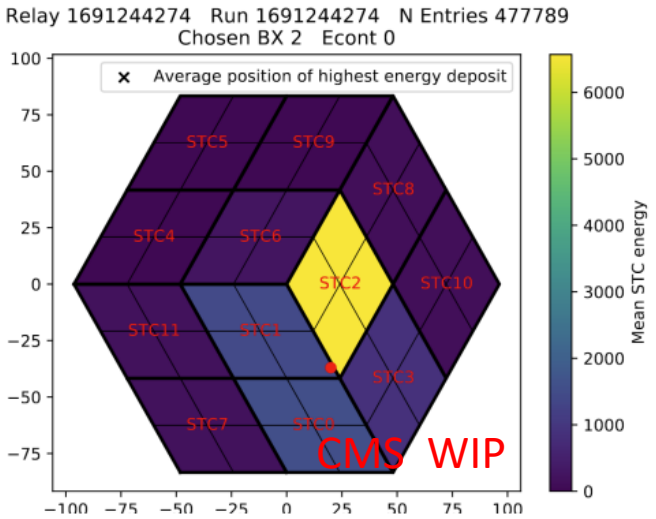
ADC data





This is a direct measurement of the HGCROC pre-amp shaper response

ECON-T data



STC Energy (encoded)

- Several billion events collected
- At rates upto 100 kHz

To do list: Completed

- Many different tasks were outlined for the recently concluded test beam to stress the system and explore some corner cases

✓ Data recording with Self-trigger (to study anomalous signals)

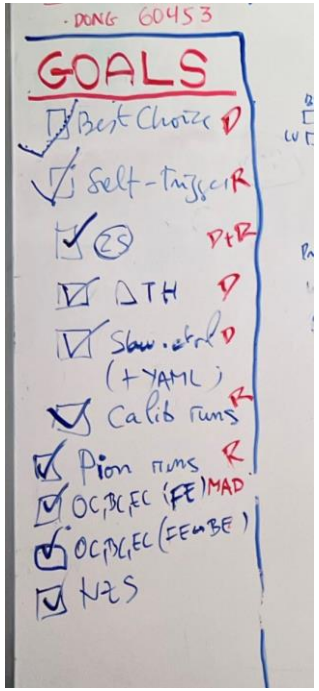
✓ Inclusion of Best Choice ECON-T algorithm

✓ ECOND: test Zero Suppression (ZS) and Non-Zero Suppression (NZS) (NZS requires special fast command)

✓ Calibration runs

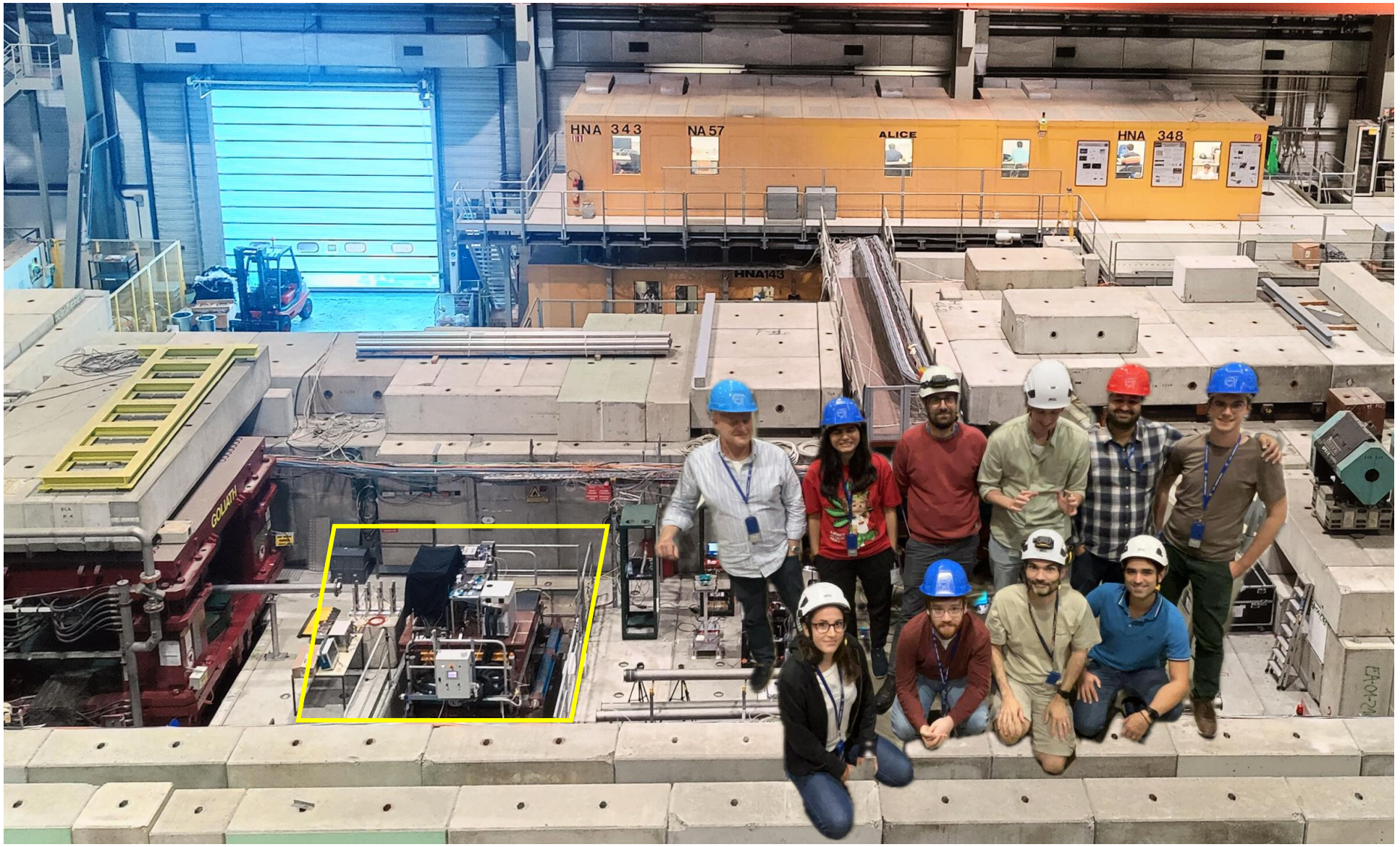
✓ Using DTH for data recording to disk

✓ Investigating FC stream and matching event tags (EC, BC, OC) across the system



Conclusions

- Over last couple of years, trigger receiver system has started coming together and recent beam test was major test of this development
- Subset of TPG Stage-1 system was integrated with DAQ path and commissioned successfully for test beam
  - Many lessons learnt regarding ASIC configuration and timing
  - Online and offline verification of ECONT receiver block look encouraging
  - Offline verification of TC processor is ongoing
- Two ECON-T algorithms STC and BC have been tested in the beam test system
- In the recent test beam, we were also able to use DTH board (from central DAQ team) to acquire data from Serenity
  - Our tests have identified a subtle bug - cDAQ team is already fixing it
- Some ancillary blocks developed for test beam system may stay long term
  - TCDS2 emulator and FC chain has been very useful to generate different (and realistic) FC sequences (can become part of EMP firmware framework)
  - Scintillator trigger system will be useful for cassette testing
- Much to learn from data collected !

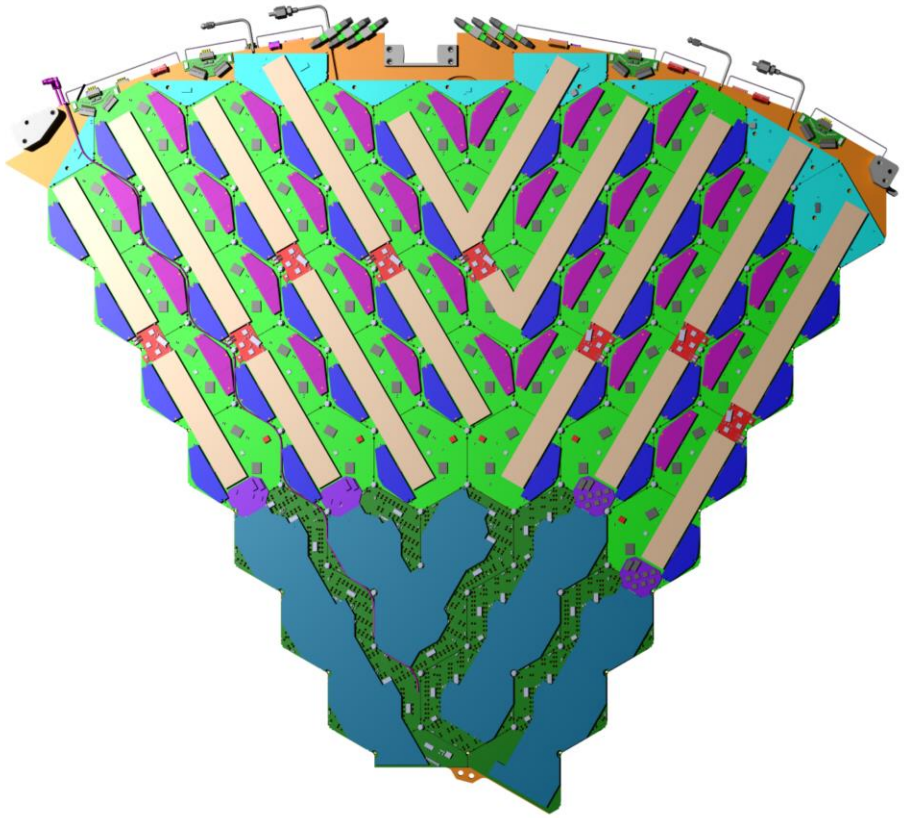


Not in picture: ECON team, DPG team

THANK YOU !

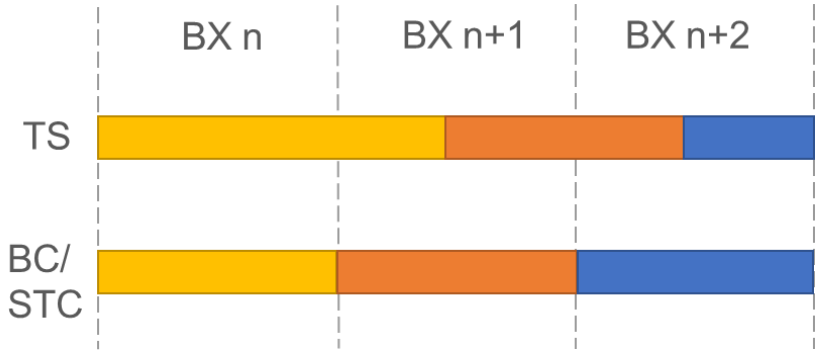
Outlook

- Having tested complete vertical slice of the HGCAL (silicon), we envisage to expand horizontally
  - Support up to 12 trains
  - Add support for HD trains
  - Work towards full DAQ and Slink aggregator
- Work has been started (@KIT) towards integrating Serenity BE with scintillator tile boards
- This will enable us to use the Serenity based back-end system for cassette testing at FNAL and CERN
- We are also looking forward to receiving next iteration of Serenity boards



Stage-1: ECON-T unpackers

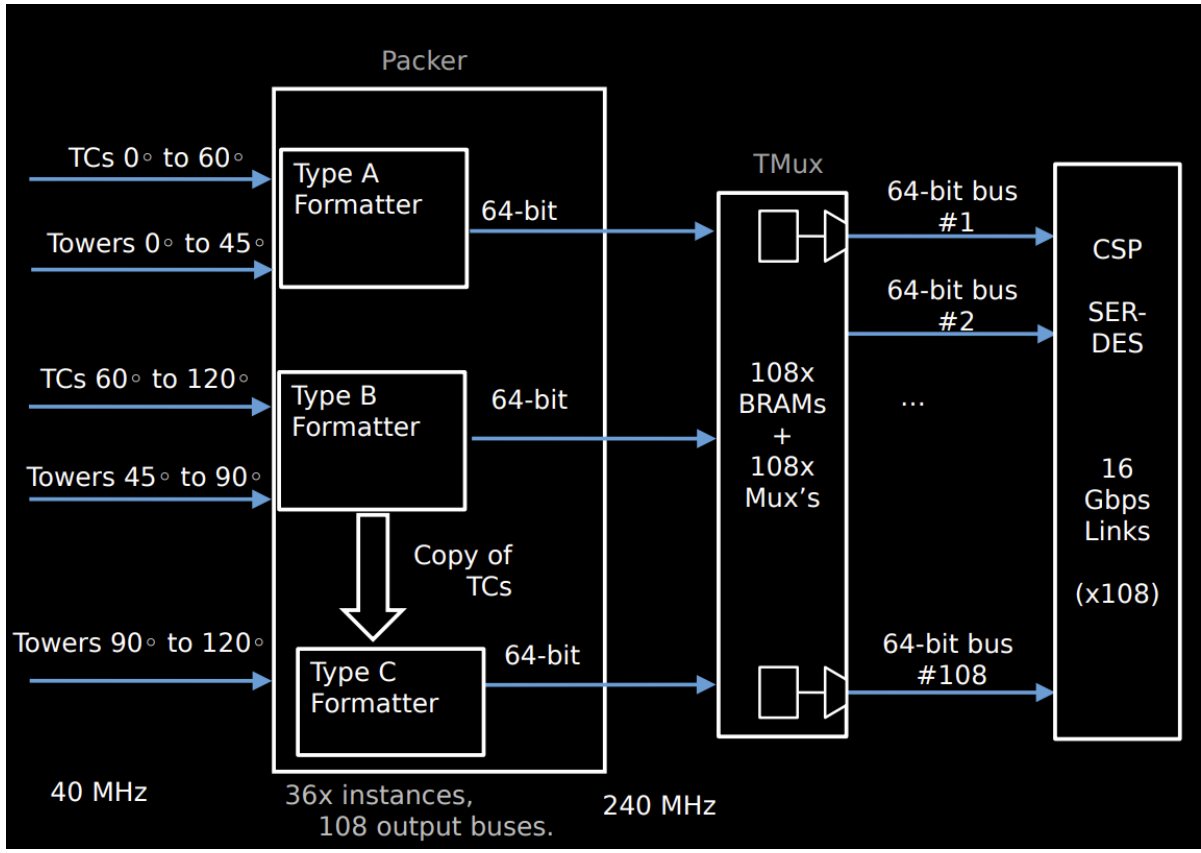
- The fixed length formats (BC, STC) are simpler to decode than variable TS format
  - E.g., Header is always at same location – no special sync mechanism
  - Packet formats are dependent on number of active e-links – frozen at design time
  - Thus, same firmware block does not need to handle all cases – case specific optimizations can be applied
  - It may be possible to keep all trigger cell (TC) values at Stage-1
- The unpackers for BC have been implemented
  - Low Occupancy: 100 LUTs
  - High Occupancy: 1100 LUTs, 6 BX latency due to decoding of 48-bit map
    - Only required for shower max layers (typically 4 e-links); about 40% (104) unpackers would be high OCC
  - Estimated to consume <10% of VU13P LUTs
  - Resources are significantly smaller than TS (~3300 LUTs, >50% for 260 unpackers per FPGA)
- STC unpackers being implemented
  - Resources are estimated to be similar to BC case



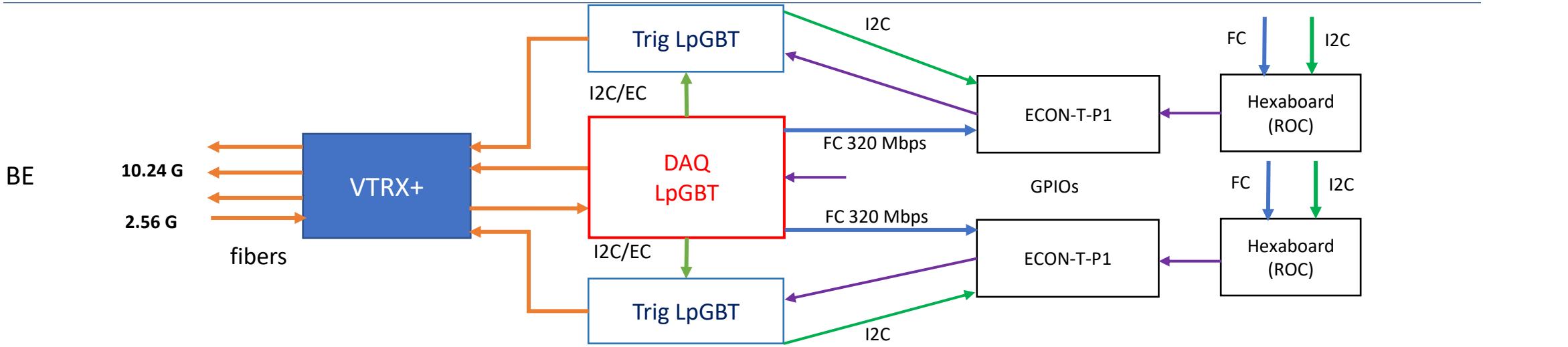
Packer-TMUX

Packet type A	Packet type B	Packet type C
Trigger Cells 0° to 60°. Tower energies 0° to 45°.	Trigger Cells 60° to 120°(same size of 0° to 60° sector). Tower energies 45° to 90°.	Duplicated Trigger Cells, 60° to 120° sector. Tower energies 90° to 120° + filling.

- The packer receives the Trigger Cells and the Tower energies
  - Trigger Cells: organized as the 0° to 60° sector and 60° to 120° sector - they have exactly same size
  - Tower Energies: organized in three sectors (0° to 45°, 45° to 90° , 90° to 120° plus filling)
  - The tower energies are also padded to be all the same size
  - Note there is not an exact 60 degree symmetry in the whole HGCAL, only in the CE-E part
- Output packets are time multiplexed by 18
- More optimization of trigger cell arrangement in link to Stage-2 has been underway may lead to redesign of this block



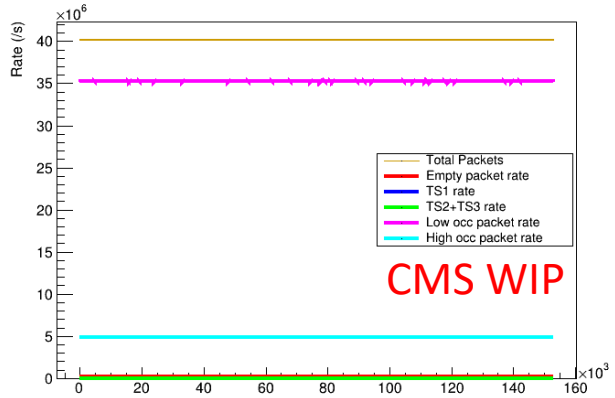
Interface: Slow Control



- Complete slow control chain from Serenity BE to available FE ASICs developed and tested
  - DAQ LpGBT register read/write using IC
  - Trigger LpGBT register read/write using IC over EC
  - ECON-T and HGCROC register read/write using I2C from trig-LPGBT
  - Slow control through GBT-SCA also tested with TrainV2
  - Firmware uses EMP supplied slow-control transactors with HGCAL specific edits (contributed to EMP framework)
- Stress tested e.g., millions random register read/writes to HGCROC (~4 hours)
- More generic software interface, SWAMP was also implemented on Serenity

ECON-T and HGCROC

- Detailed interface tests with ECON-T emulator (TrainV2) and ECON-T P1 (TrainV3)
  - Tested TS with most of the corner use cases with firmware decoding
    - Lots of online checking and error/status counters e.g. histograms of number of TCs in each packet, lock counter etc.
  - Tested if BE firmware unpacks different algorithms correctly
    - Most of the tests repeated for Best Choice; will be done with STC as well
  - Stability tested over days
- Interfaced HGCROC (trigger-links) to ECONT
  - Achieved correct FC sequence to establish word alignment
  - End to end TC verification from HGCROC to BE unpacker
- **Complete trigger path tested from HGCROC to BE unpacker!**




```
*** Packets Summary for unpacker 1, log file unpacker_mon_20221006_192305.log  ***
    Total packets processed by the unpacker1 is 12288481053789.0

    Total TS1 truncated packets 0.0
    Total TS2-TS3 truncated packets 0.0
    Total Empty packets 44628111610.0
    Total High Occ. packets 1477978049132.0
    Total Low Occ. packets 10765875629631.0
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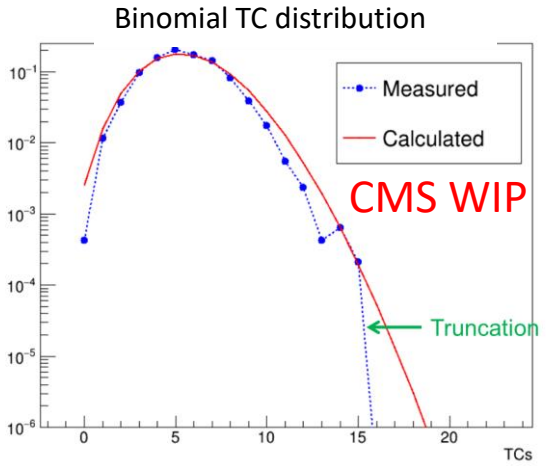

Verification of trigger path

- The unpacker accuracy has been examined with offline data analysis by comparing STC energies