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The CMS HGCAL trigger data receiver

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As part of the CMS Phase-2 upgrade, a prototype of the receiver of raw trigger data from the HGCAL endcap has been implemented using the Serenity ATCA platform. The receiver firmware was developed to test the unpacking of data from the front-end endcap trigger concentrator ASIC and measure its performance and stability. The firmware mainly consisted of unpacker blocks to decode ASIC packets, error detection mechanisms and online histogramming capability. The system was successfully used to achieve complete trigger path readout, involving several ASICs, and to test the stability of the system with online and offline monitoring.

Summary (500 words)

The CMS HGCAL front-end (FE) system includes several custom radiation-hard ASICs. These consist of a multichannel ADC and TDC (HGCROC) followed by concentrator ASICs (ECON) which aggregate data from multiple HGCROCs. Aggregated data is serialised using a high-speed serializer (LpGBT) and transmitted to the back-end (BE) system using optical transceivers (VTRx+). The HGCAL Trigger Primitive Generator (TPG) will construct calorimeter clusters for the Level 1 trigger decision using "trigger cells"(TC) from the FE chain. BE Stage-1 of the TPG is responsible for decoding the compressed TCs from the trigger concentrator ASIC (ECON-T), filtering the TCs, and sending them to the time-multiplexed Stage-2 of the system. The TPG Stage-1 will be implemented using the Serenity ATCA platform, with each FPGA expected to handle about 300 ECON-Ts. The overall HGCAL electronics system is summarised in Figure 1.

The ECON-T supports different compression algorithms. The variable latency algorithm offers high efficiency but it is complex and resource intensive to decode at the BE. The fixed latency algorithms are much easier to handle and have been shown to offer comparable performance in simulation studies. The unpacker firmware was developed for the variable latency and one of the fixed latency algorithms. The BE firmware mainly consisted of unpacker blocks to decode ECON-T packets, error detection mechanisms and online data analysis by histogramming different parameters. Status and error counters were periodically read out using an onboard control bus and metrics were displayed using a Grafana web interface.

The prototype Stage-1 system was tested with two versions of HGCAL FE vertical stacks. The earlier version used an emulator for the ECON-T while the latest version used the prototype ECON-T. The BE firmware and the FE ASICs were tested in steps, integrating one ASIC of the chain at a time. Initial tests included configuring the ECON-T with known input data patterns (static and PRBS) and testing the decoding at the BE with different compression algorithms and packet types. Figure 2 shows the result of one such test where the ECON-T was programmed to use PRBS-generated TCs and the variable latency algorithm to package them. A histogram of the number of TCs in each decoded event in the firmware showed the expected packet type selection and truncation behaviour. Ultimately, the challenging task of integrating the complete trigger chain was achieved and we could accurately reproduce (receive) pre-programmed TCs from HGCROC in the BE.

The prototype BE system allowed successful testing and validation of some major BE firmware components and the ECON-T ASIC. It has established a readout of the complete trigger chain. We were also able to test the stability of the system with online and offline monitoring. The BE system is being expanded further to include the DAQ path (HGCROC and ECON-D ASIC) and high-speed readout. We are preparing to test a complete vertical slice in a beam test in summer 2023.

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