



TWEPP 2023 Topical Workshop on Electronics for Particle Physics

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IP2I, Lyon, France

1) iRPC project for HL-LHC

2) FEB design

3) FEB certification, calibration and integration

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CNIS

1)iRPC project for HL-LHC

1.1) iRPC project for HL-LHC phase



- 36 petal-like chambers.
- Redundancy with CSC chambers providing high granularity space resolution.
- Excellent absolute timing resolution for L1 trigger: O(500 ps).
- Dedicated trigger for Heavy Stable Charged Particles.



1.2) iRPC project constraints

	Present system	iRPC
η coverage	0-1.9	1.8 - 2.4
Max expected rate (Safety factor SF = 3 included)	600 Hz/cm ²	2 kHz/cm ²
Gap size	2 mm	1.4 mm
Average charge / MIP	~ 120 pC	~ 40 pC
Electronics threshold	150 fC	30-50 fC
TDC T resolution		20 ps



A dedicated iRPC electronics designed to fulfill higher background conditions.





1.3) What is an RPC chamber



Muon crossing the chamber generates small avalanches in 2 gas gaps
 A signal is induced in copper strips located outside of the gas gaps.
 Signal transported to the FEB where it is amplified, dscriminated and time tagged.



1.4) iRPC readout



2) FEB design





M. Gouzevitch: FEB for CMS iRPC project



2.1) History of the FEB

First proto

2017 proof of principle for CMS-MUON-TDR-016

2 PetiROC2A + FPGA Cyclone II + ETHERNET directly on strip PCB (50 cm)



Feb V0 2018 First FEB (Conf. note)

1 PetiROC2A + MEZZANINE with FPGA Cyclone II + ETHERNET





Feb V1 2019 FEB without mezzanine

2 PetiROC2B + FPGA Cyclone V + ETHERNET



Feb V2_1,2 2021 Non-rad hard for iRPC Demo

6 PETIROC2C + 3 FPGA Cyclone V + Optical GBT



Feb V2_3 2021 Mass production prototype

FEBv2_1 + firmware update feature by optical GBT





2.2) FEBv2 details

- \succ 2 FEBs / Chamber → 144 (+16 spares) FEBs in total
- ➤ 3 Erni connectors with 32 channels each.
- ➤ 6 ASIC PetiROC2C (PR2C):
 - Specially designed by OMEGA group for CMS RPC project based on Petiroc2A
- ➢ 3 FPGAs (96 + 6 TDC channels)
 - FEBv2: CYCLONE V (non rad-hard)
- CERN ASICS: GBTx + GBT-SCA + VTRx
 for the communication ald close control
 - for the communication ald slow control
- Separated 2V and 4V power zone for Analog and Digital components. Latchup protection (Overcurrent detection).



05/10/2023





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M. Gouzevitch: FEB for CMS iRPC project



2.4) PetiROC ASIC

PETIROC2A designed for PET

- High frequency preamp
- **-** Thr > 60 fC
- Time resolution < 100 ps
- Limitations: low rate expected



https://dx.doi.org/10.1109/NSSMIC.2018.882445

PETIROC2A for RPC :

- Retriggering and interchannels cross-talk
- Thr > 100 fC
- Time resolution < 200 ps

PETIROC2B modif for iRPC :

- Reduce preamp. frequency
- Thr ~ 100 fC
- 10-20 ns / ASIC dead time introduced to remove retriggering
- \rightarrow 2-3% efficiency loss / chamber

PETIROC2C re-designed for iRPC :

- Removed useless components from PR2A.
- Thr < 50 fC
- 40 ns auto-reset / channel te remove retriggering.
- 864 (+ 96 spares) required,
 900 available,
 1000 under production.



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2.5) Radiation hardness

- <u>TID</u> (γ's) -- Facility ENEA Casaccia Calliope ⁶⁰Co July 2022 Requested: 17 Gy Certified:
 - FPGA Cyclone V (50 Gy):
 - Petiroc (160 Gy);
 - Power supply zone (100 Gy)
 - Safety Factor: 3 9
- 2) <u>TNID</u> (neutrons) Facility FNG Frascati, with support from RADNEXT March 2022 Requested: 6e11 neq1MeV/cm²: Certified: 25e11 neq1MeV/cm²:

SF: 4

3) <u>Neutron flux</u> -

Requested: 10e3 neq1MeV/cm²/s Certified: 450e3 neq1MeV/cm²/s SF: 45









2.5) Radiation hardness







- No persistant radiation damage is observed on any components of the FEB for the doses under consideration :
 - \rightarrow performences of the FEB doesn't change with accumulated dose.
- No Single Events Upsets (SEU) observed in Petiroc2C
- Few Single Event Latchups (SEL) observed in power supply well catched by the overcurrent protection.
- SEU's observed in Cyclone V.

 \rightarrow We estimate that during HL-LHC phase 1 Cyclone V needs a soft reset (1 second) every 10 hours of CMS data-taking.

 \rightarrow Soft reset can be performed in a transparent way for CMS data taking and trigger.

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3) Certification, calibration and integration

Relevant physics parameters :1) Sensitivity to RPC signal : pedestal alginements and calibration2) TDC Time resolution and time alignement.



CMS

3.1) FEB certification steps in IP2I, Lyon

Based on the **FC7 card (Tracker certification card)** system and controlled by **Python software** tools.

- > Perform a Quality Check Process to validate :
- Each electronic block of the FEB independently (SCA, GBTx, Power Supplies, tests points)
- The data integrity of the system
- The operation of the FEB firmware designed in the FPGA(s)
- The operations of the TDC(s) and ASIC's
- Simulation and validation of real operation with injection board



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M. Gouzevitch: FEB for CMS iRPC project

3.2) FEB pedestal alignement method



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3.3) FEB calibration

DAC T vs Charge

Measurement setup considerations Injection board FEB-V2 DACT PetiROC Injection capacitor (detector simulation) 1 mV 100 mV Injected charge 100 pF Generator Attenuator (Low voltage Noise) -40 dB 68 200 な マ 47 ERNI Good quality generator mandatory (low noise voltage and linearity) Connectors -Use of high ratio attenuator to reduce noise -Use of highest injection capacitor



Calibration factor = 4.6 ± 0.5 fC/DAC T

THR: Specification

50 fC 与 11 DAC T Used in test beams 32 fC 与 7 DAC T

3.4) TDC time resolution



Pure TDC time resolution was measured using 2 channels test and a reference:



3.5) Chamber absolute time resolution



- 2 chambers iRPC chambers in test beam in Gamma Irradiation Facility (GIF++) at SPS CERN.
- Absolute time resolution of the system : 780 ps $\rightarrow\,$ per chamber 780/ $\sqrt{2}$ ~ 550 ps

3.5) Space resolution



- A cosmic telescope is made of 2+2 RPC chambers with 1x1cm² pads.
- iRPC chamber in sandwitch.
- Comparing extrapolated track and actual position of the RPC hit.

3.5) Space resolution





3.6) FEB power consumption

Total consumption: 2V*6.3A+4V*2.3A = 22 W



FPGA

Hottest elements:

- linear regulators Ohmic effect
- Optical communication
- FPGA logic

Cooling system

- 1) Thermal pads + copper plate
- 2) Cooling pipe
- 3) Cool water: 15 C

Max temperature < 50 C

Play also the role of grounding plane



CONCLUSIONS

- iRPC FEB desinged/certified, integrated into the chamber and ready for mass production.
- The rad tolerance of the FEB are sufficient for project requirements
- Time and threshold calibration finalised and caracteristics meets the HL-LHC requirements :
 - Threshold : 30 fC
 - Space resolution :

1.6 cm along strip, 0.4 cm perp. to strip

- Time resolution : 500 ps



BACKUP





Validation en radiation gamma



Caliope a ENEA Casaccia a côté de Rome





FEBv2 logical scheme



M. Gouzevitch: CMS iRPC FEB development and validation











Expected fluence and dose (RE34/1 FEBs)

- at R=303 cm for RE3/1 is ~4.3 (5.8) x1011 n/cm2, and
- at R=304 cm for RE4/1 it is about 6.2 (8.2) x10¹¹ n/cm²,
- at R=303 cm for RE3/1 is ~10 (13.6) Gy
- at R=304 cm for RE4/1 it is about 18 (24) Gy
- where R=303 (304)cm are the expected FEB positions
- Expected fluence and dose (Balcony)
 - The total irradiation fluence 800 x 10⁹ cm⁻²
 - Maximum integrated dose is about 10 Gy





Behzad Boghrati, Radiation Hardness of Electronics for Phase-2 Upgrade of RPC Muon System, RPC Workshop, 31 Aug. – 1 Sep

2020



2.8) Extrapolation to HL-LHC

Estimation using flux (same method used for LB ESR)

ODE:

Estimation using fluence

	CHARM	HL-LHC (continuous data taking at max intensity for 1 day)		(HEH+ThN)/SEU from CHARM	(HEH+ThN)/year at HL-LHC (10 years of data taking)	SEU/year		
Flux (HEH+ThN) (/cm²/s)	4.2e5	5.6e3	210e6 - We could assu		3.2e10 150/year			
SEU	1/8.2 mn	<mark>1 / 10.3 h</mark> 2.3 / day		 Among these stops only a fraction would require an FPGA power cycle (see slide 14). 1500 FPGA power cycles in full FEB life. During CHARM tests we performed around 3000 FPGA power cycles without problems. 				