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Design, production and irradiation results of the new advanced front end electronics of CMS iRPC

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New advanced front end electronics are designed for the improved RPCs of CMS experiment for data taking during HL-LHC era. This electronics is developed to read out the RPC detectors from both ends of a signal strip, using a new ASIC, iRPCROC, which triggers the Cyclone V FPGA to record the timing information, allowing the correct identification of the position along it. The on-chamber results of the test beams and commissioning at CMS with focus on performance of the electronics will be presented.

Summary (500 words)

New advanced front-end electronics are designed for the new improved RPCs of CMS experiments for data taking during the HL-LHC era. During the High Luminosity CERN LHC (HL-LHC) operation phase, the instantaneous luminosity will be increased to 5 – 7.5e24/cm²/s, a factor 5–7.5 above the LHC design value.
The front-end electronics (FEBv2) is designed to read out the RPC signals from 2 ends of a strip and determine the hit position along the strip with high precision and the absolute hit timing. The analog RPC signal first enters the iRPCROC, a new ASIC from the PETIROC family. There it is pre-amplified, and the rising edge is discriminated at GHz frequency. This version of the ASIC includes features drastically reducing the cross-talk between channels as well as the retriggering effects. Finally, the resulting digital signal is time-stamped by a delay-line Time-Digital-Converter (TDC) implemented into the Cyclone V INTEL FPGA.
In the first step, we describe the schematic of the FEB. We will discuss the main features of the design, which reduce the noise, cross-talk, retriggering, and grounding scheme.
The second step will present the calibration, synchronization, and measurement of the time resolution. It is as low as 30 ps, well below the time resolution effects from the RPC chamber. We describe how we calibrated and estimated the charge sensitivity of the FEB and how we determined the optimal working point. The FEB can be operated with a threshold of 30 fC, with negligible noise. This threshold can be lowered if needed down to 20 fC.
In the third step, we will describe the peculiarities of the FEB operation in the hard radiation background characteristic of the HL-LHC phase. We developed a radiation-tolerant firmware which we will describe. The FEB underwent multiple certification sessions for the total integration dose and for the Single Event Upsets and Single Event Latch-Up in gamma, neutron, and mixed field (thermal neutrons ThN, high energy neutrons, and hadrons - HEH) facilities in ENEA, Italy, and at CERN.
No cumulative effects in the FEB operation were observed after irradiation with the mixed field in the CHARM facility. The total integrated dose was 60 Gy and fluences 1.6e11 HeH/cm², 3.3e11 ThN/cm². In the neutron irradiation facility FNG in ENEA, Frascati, we pushed the high energy neutron flux up to 25e11 neq1MeV/cm² concentrated on 1 of the Petiroc2B. No degradation was observed either.
In the CHARM facility, it was demonstrated that in the HL-LHC conditions, with an expected flux of 5000 HEH/s/cm², including safety factor 3, an SEU would occur 1-2 times per day, and an SEL once one year. The SEL protection system was proven to work well. Furthermore, the SEU recovery time does not exceed 20 s.

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