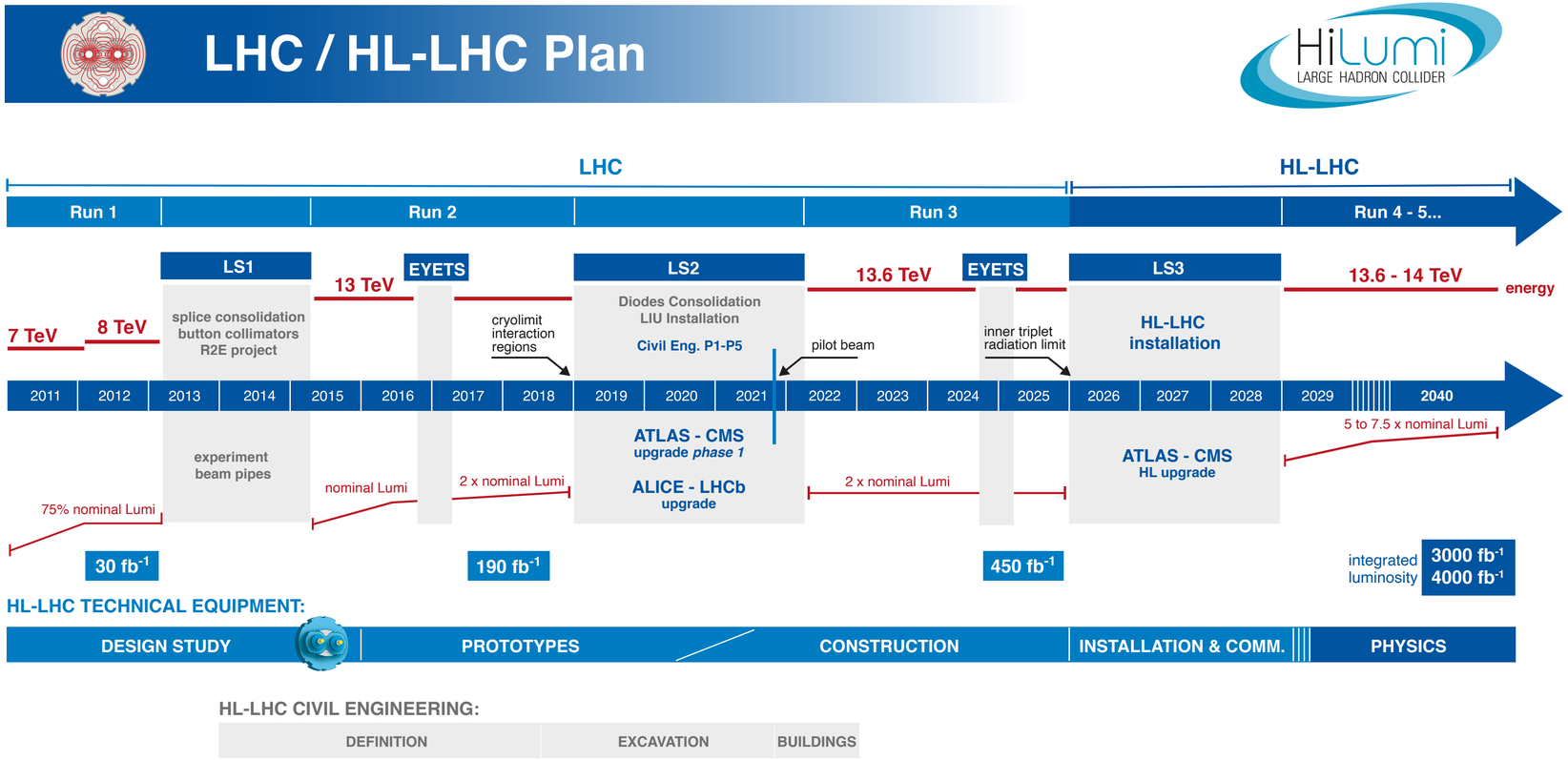
The Trigger & Data Acquisition interface module of the Tile Calorimeter for the ATLAS Phase-II Upgrade

Tigran Mkrtchyan (KIP, Heidelberg)

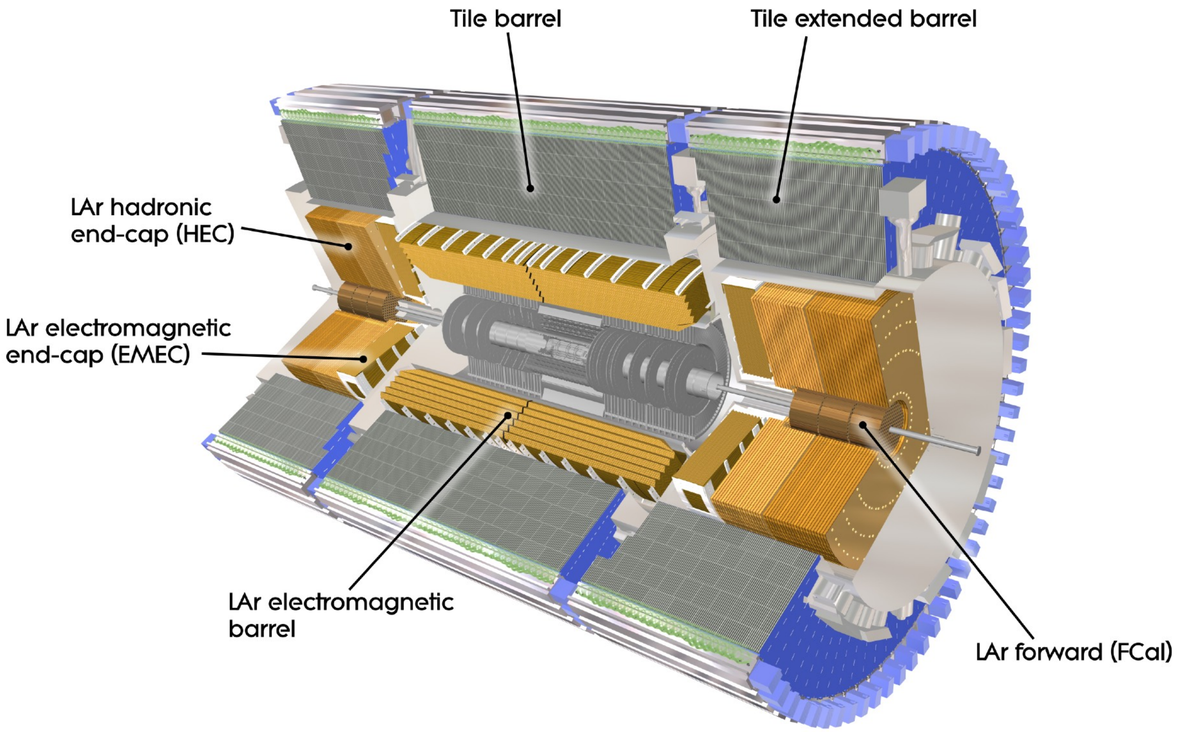
05.10.2023, TWEPP-23

The HL-LHC



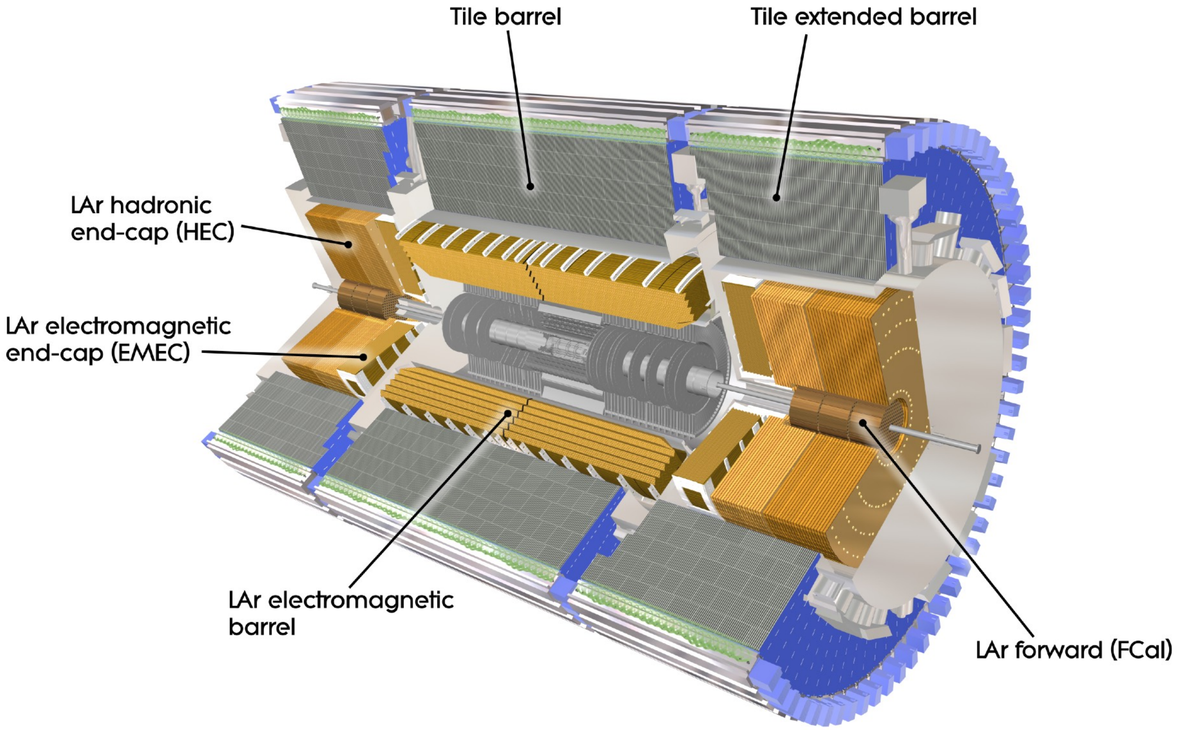
- The instantaneous luminosity will increase by a factor of ~ 5
- 200 proton-proton collisions per bunch crossing
- Increased particle flux through TileCal: from 2 to 24 Gy for 4000 fb^{-1}

The ATLAS Tile Calorimeter



The ATLAS Tile Calorimeter

- Central hadronic calorimeter $|\eta| < 1.7$
- Sampling calorimeter with steel absorbers
- Plastic scintillators as active medium



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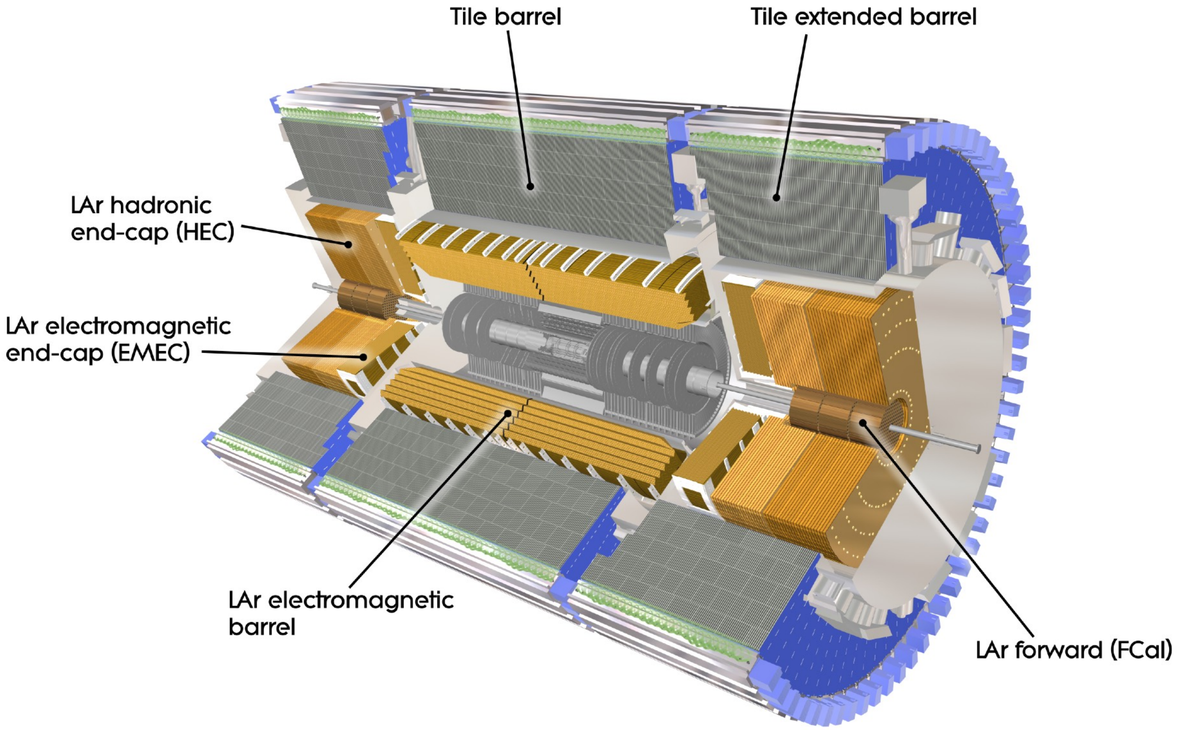
- ~ **5000** cells
- ~**10000** Photomultipliers (PMT)
- Each cell read out by 2 PMTs using wavelength shifting (WLS) fibers



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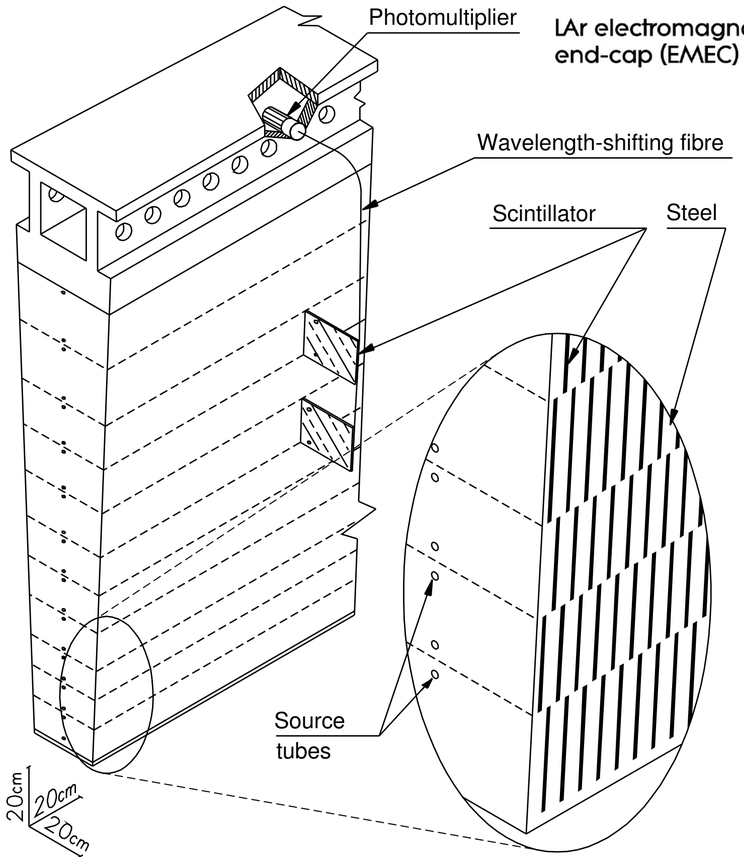

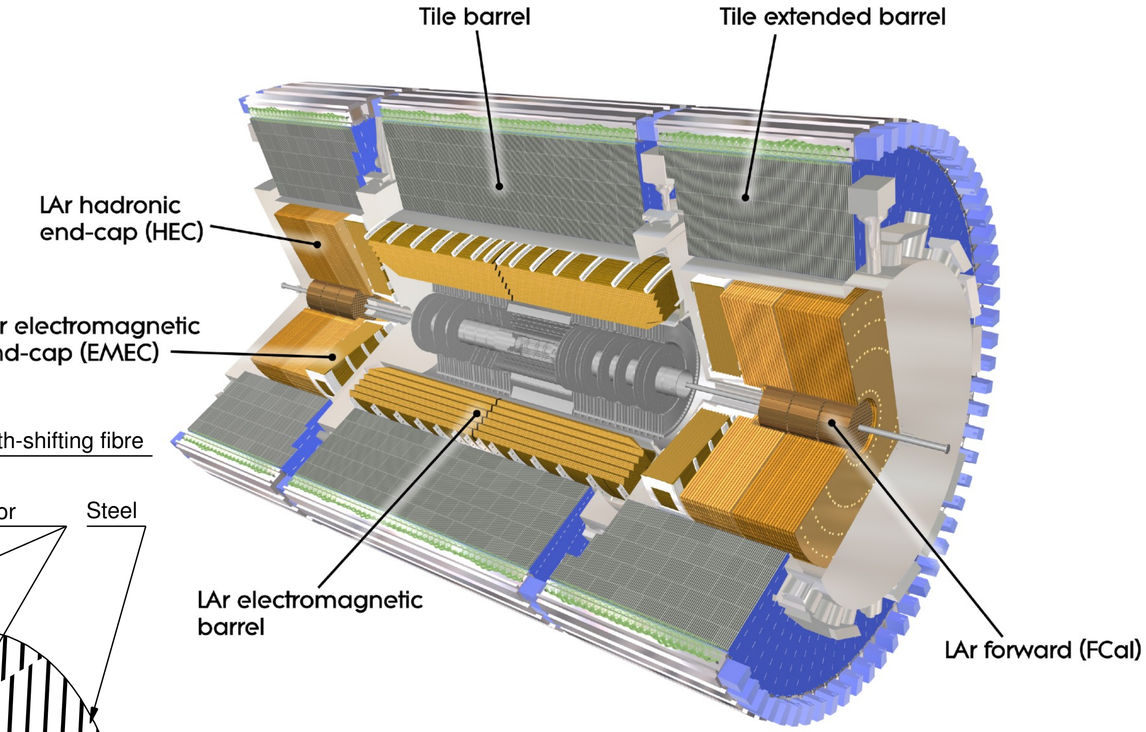

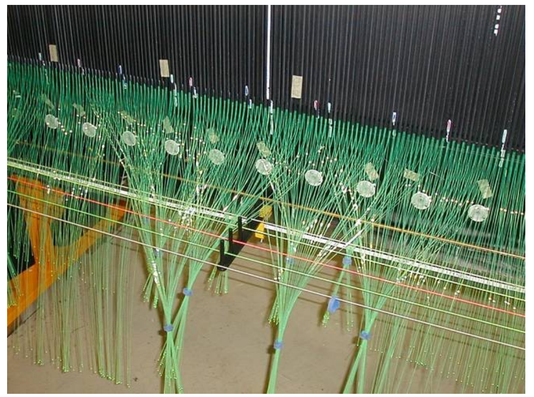

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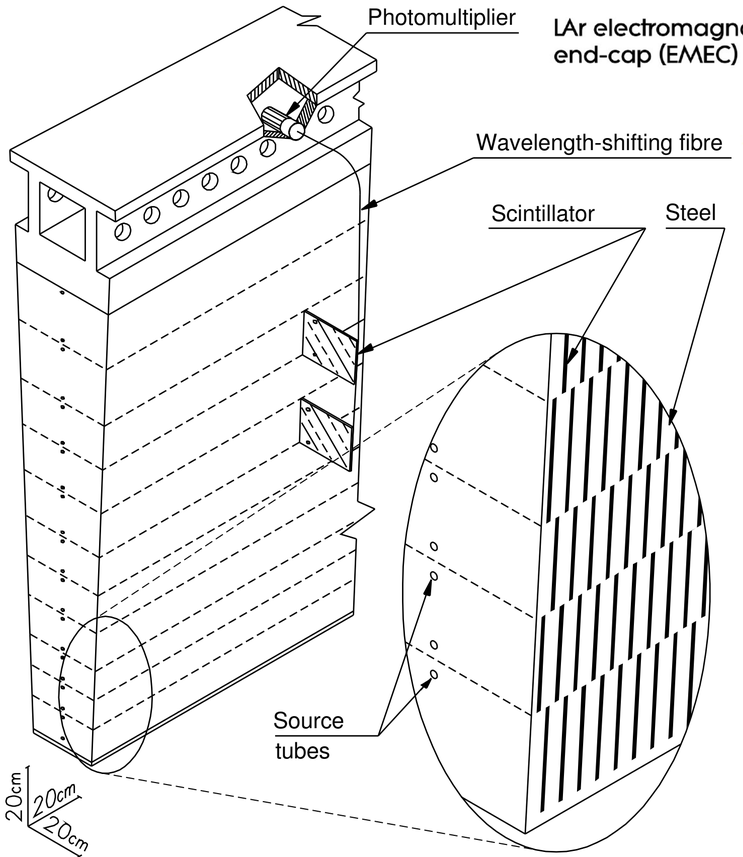
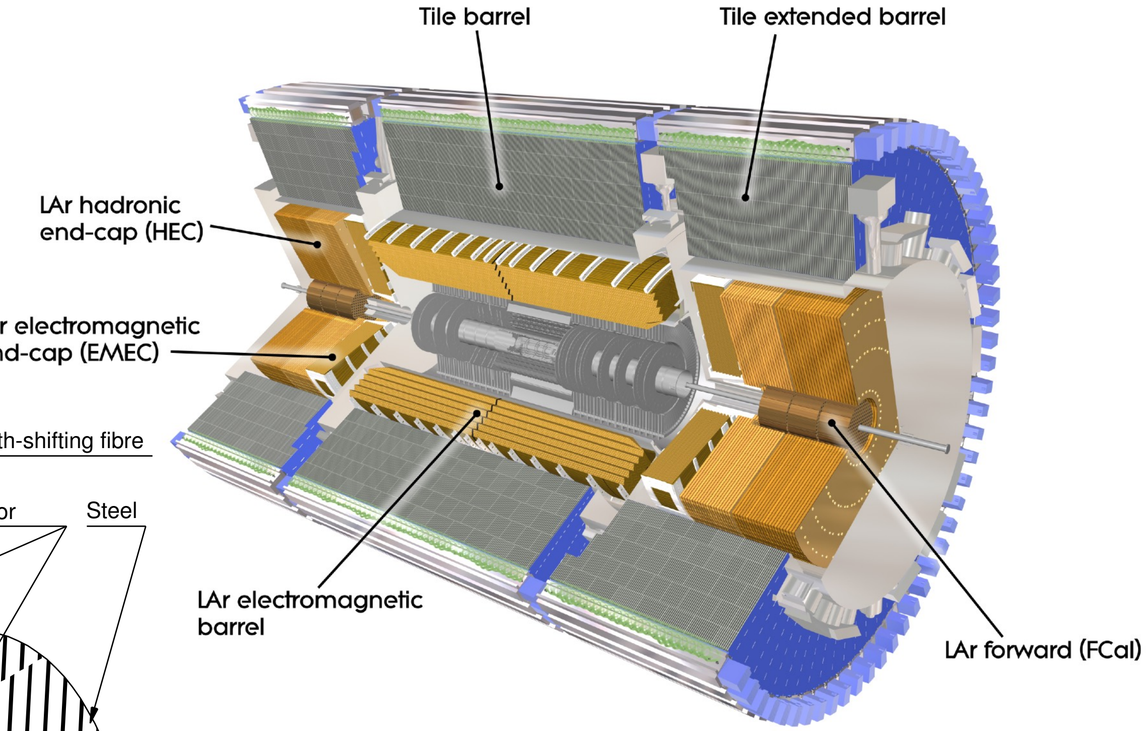
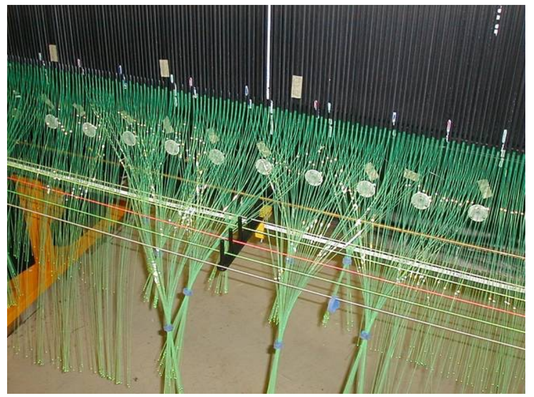
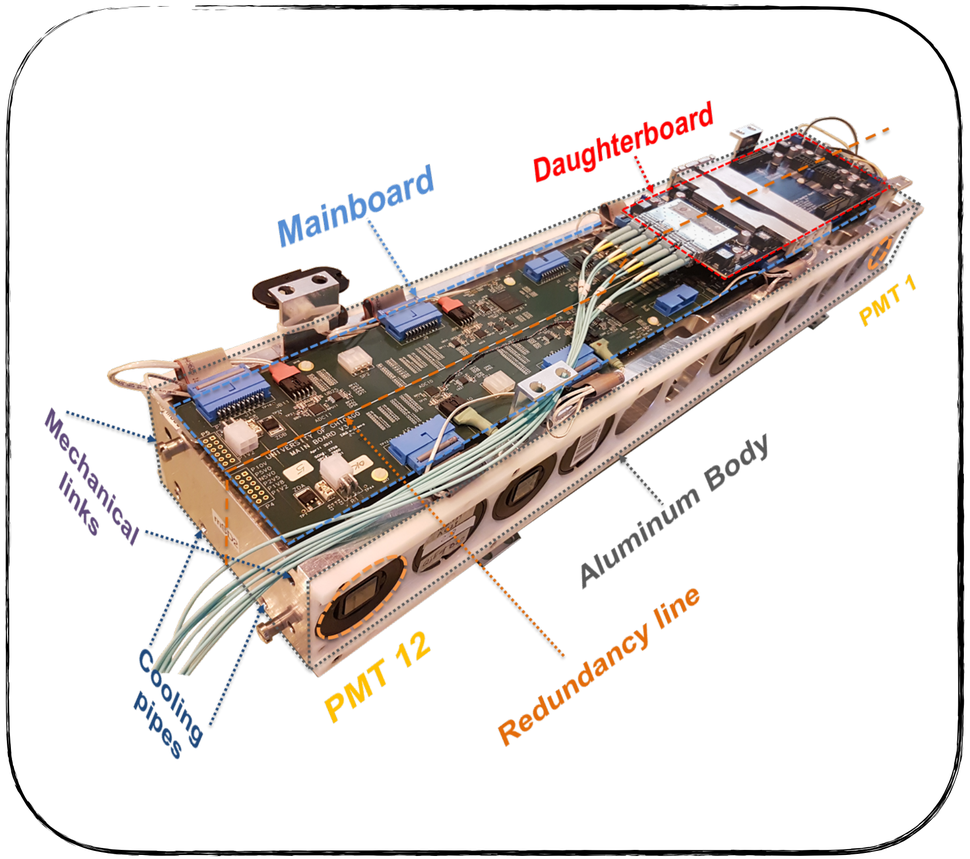
- ~ **5000** cells
- ~**10000** Photomultipliers (PMT)
- Each cell read out by 2 PMTs using wavelength shifting (WLS) fibers
- Critical for all physics signatures:
  - Jets, Missing p_T
  - Muons & Electrons/photons
  - Taus







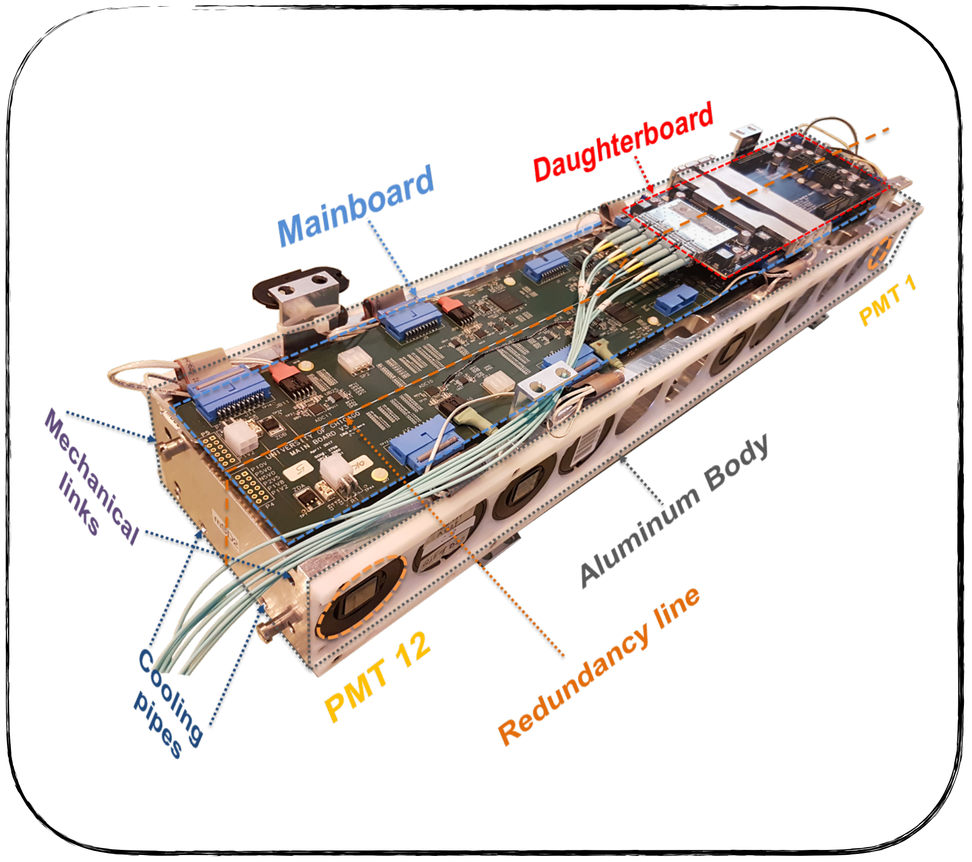
Phase-II Upgrade of TileCal



The new Mini-Drawer

Phase-II Upgrade of TileCal

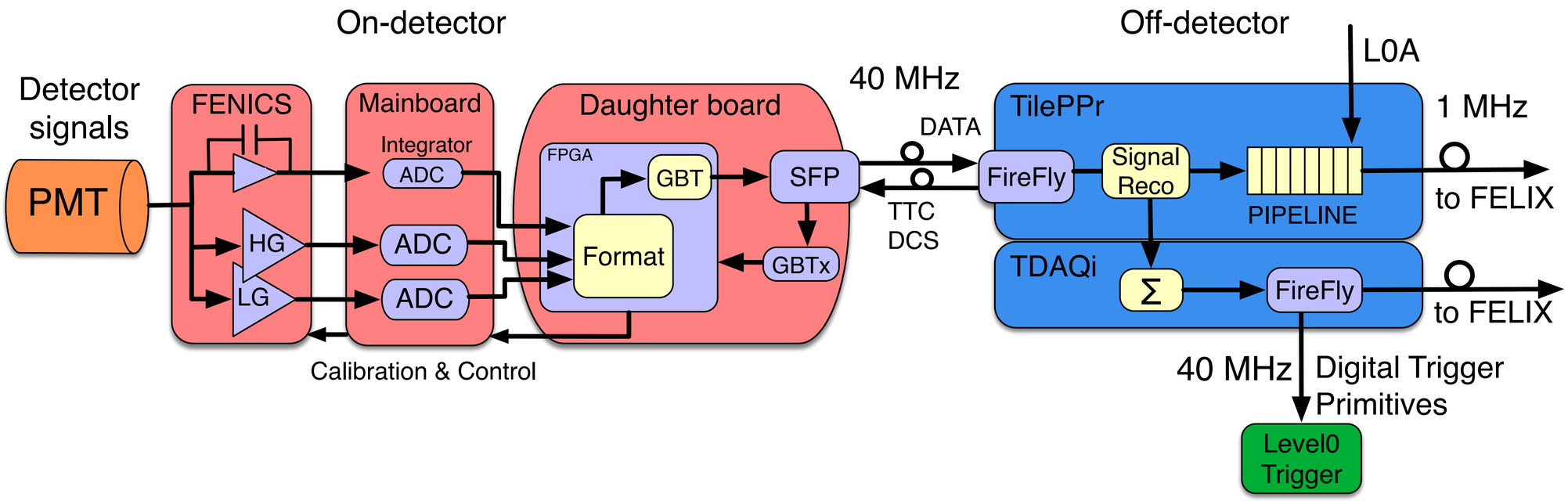
- **Replacement** of the entire Front- and Back-End Electronics
- New **modular** mechanics (Mini-Drawers)
- **Increased** Radiation Hardness & Redundancy
- **Redesign** of the High-Voltage and Low-Voltage Systems
- **Faster** readout electronics
- **Replacement** of most exposed PMTs



The new Mini-Drawer

Phase-II Upgrade of TileCal

- Detector components (absorbers, scintillators, most PMTs) will not be replaced
- Add reliability by means of redundancy
  - Minimise single point of failures
- Replacement of Photomultipliers most exposed to radiation
  - Better response stability and degradation
- Employ electronics components with higher radiation tolerance



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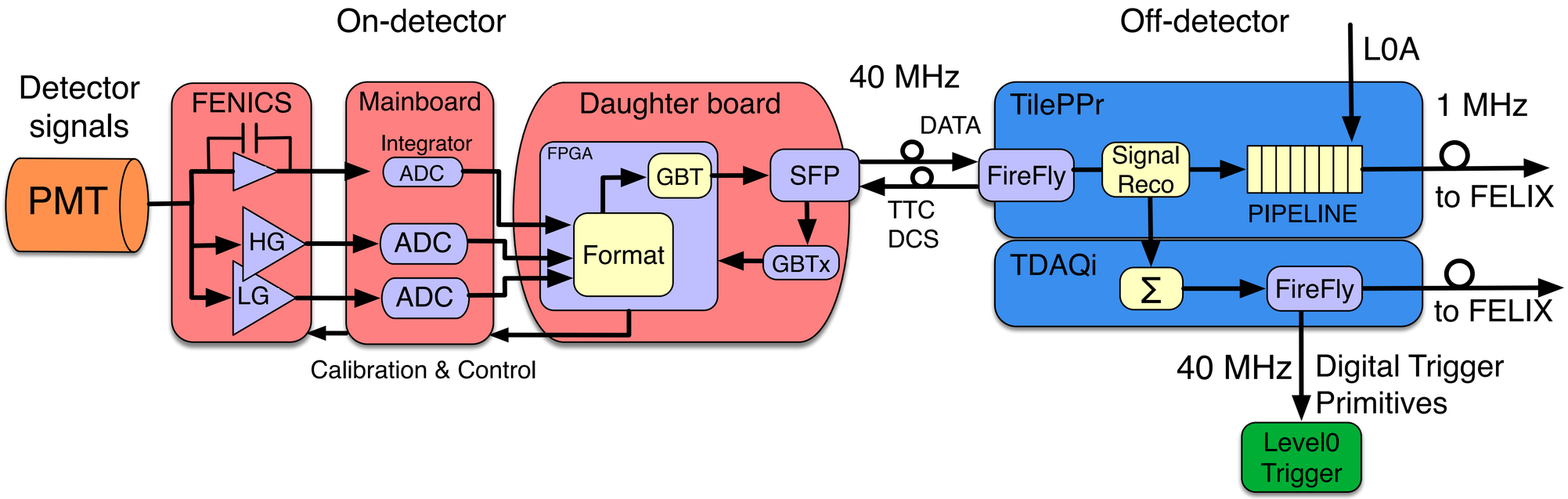
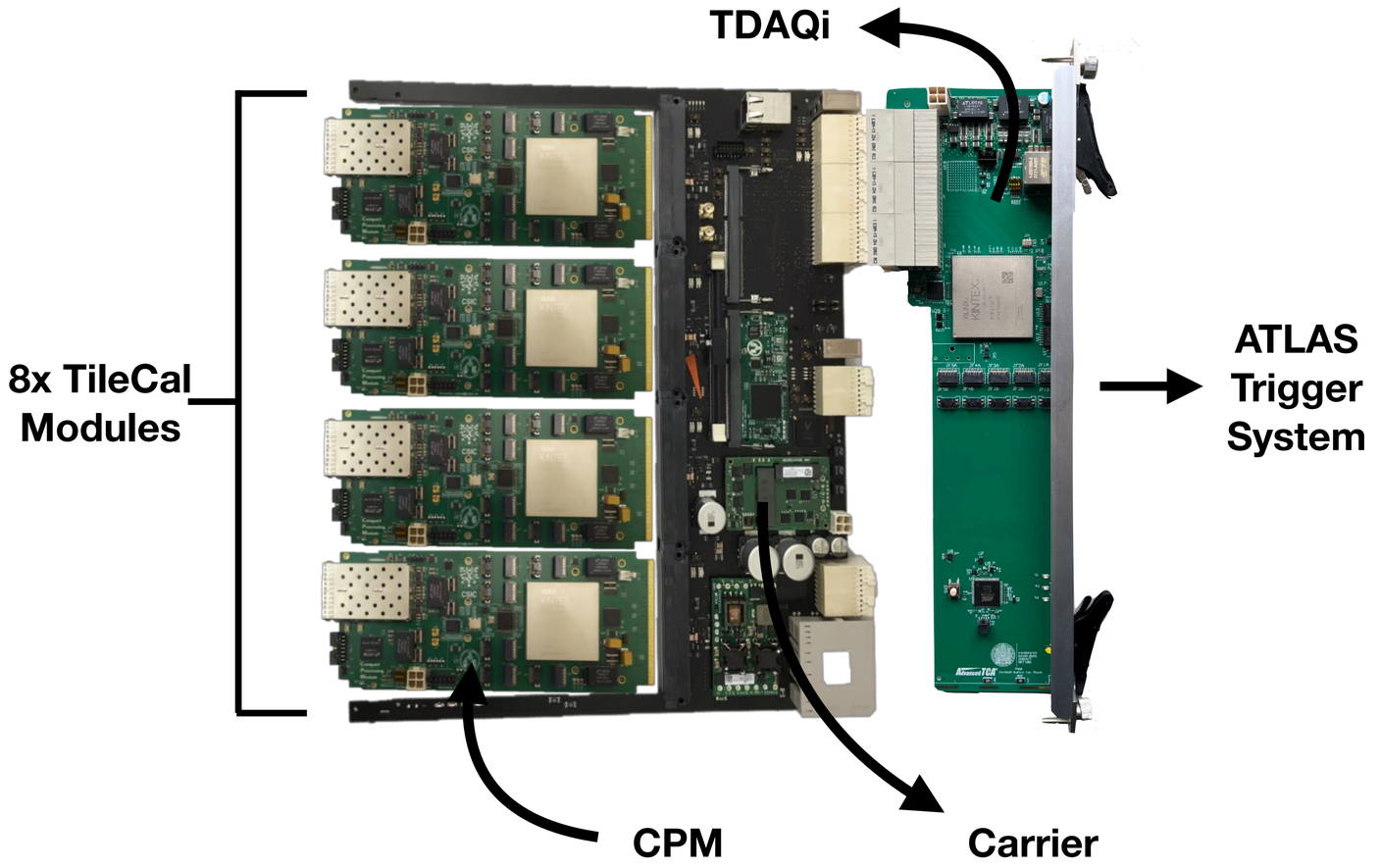
- New readout architecture
  - **Digital Trigger** at 40 MHz
  - Higher trigger rates ~ **1MHz**
  - Larger data buffering - all done off-detector
  - **High-speed** optical transmission



Off-detector Electronics

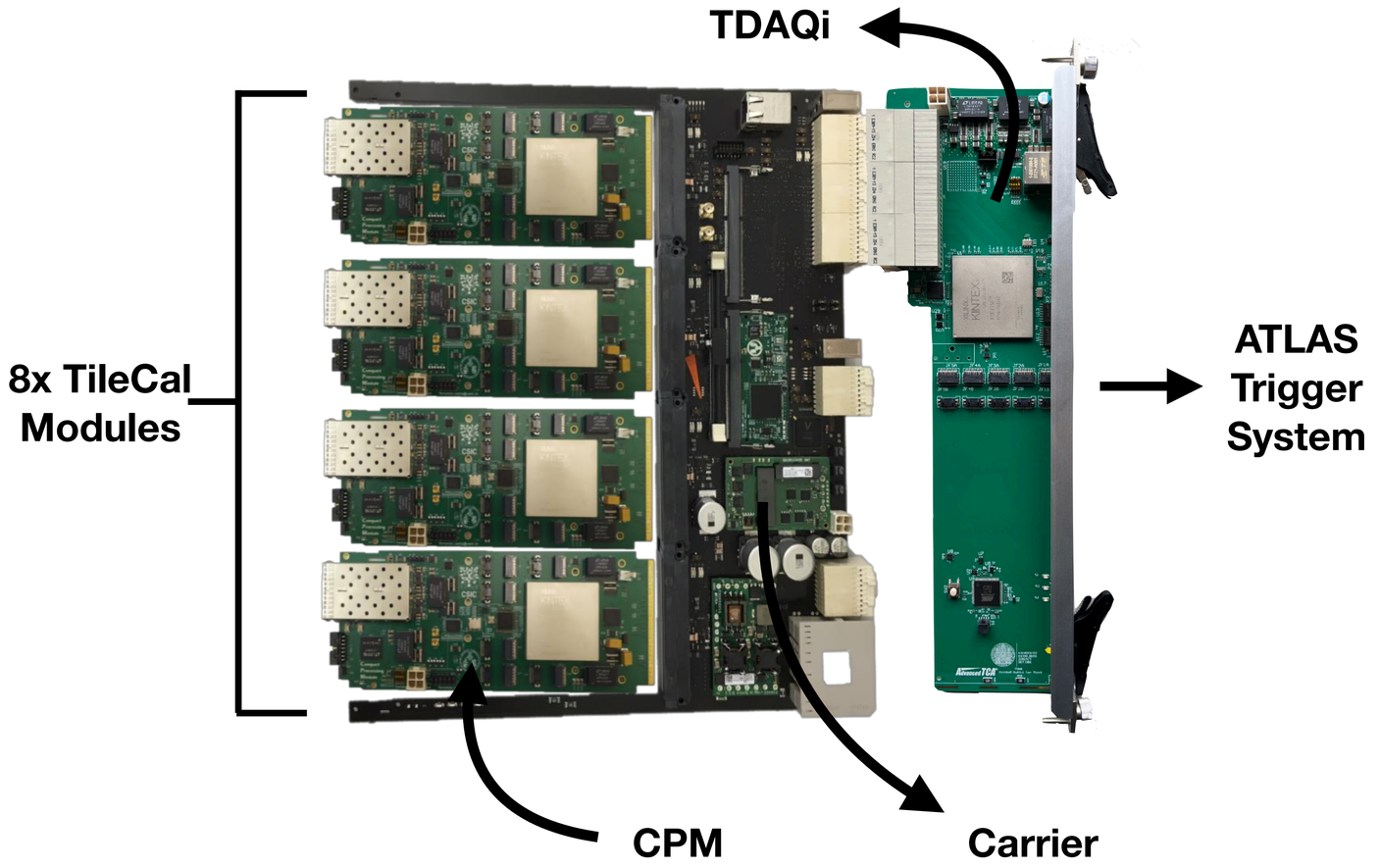
- **AdvancedTCA**-based blades
- **Hub** between the on-detector and ATLAS Trigger & DAQ
- One Tile PreProcessor board includes:
  - 4x Compact Processing Modules (CPM)
  - 1x Carrier Board
  - 1x Trigger & DAQ interface (TDAQi)
- 8 TileCal modules are read out by one TilePPr



Off-detector Electronics

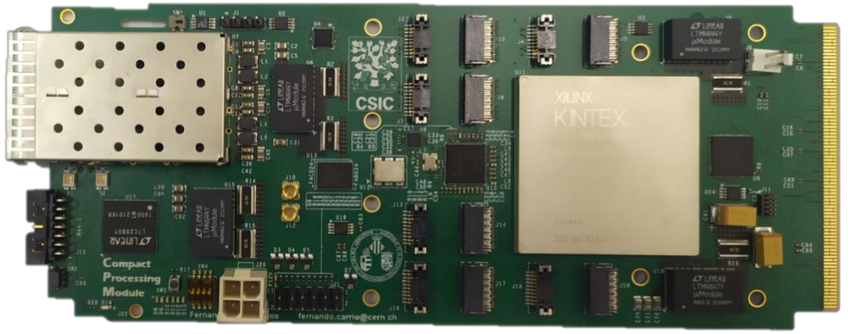
- **AdvancedTCA**-based blades
- **Hub** between the on-detector and ATLAS Trigger & DAQ
- One Tile PreProcessor board includes:
  - 4x Compact Processing Modules (CPM)
  - 1x Carrier Board
  - 1x Trigger & DAQ interface (TDAQi)
- 8 TileCal modules are read out by one TilePPr

- The total system is made up of 32 PPr boards
  - **128x** CPMs
  - **32x** Carrier boards
  - **32x** TDAQis

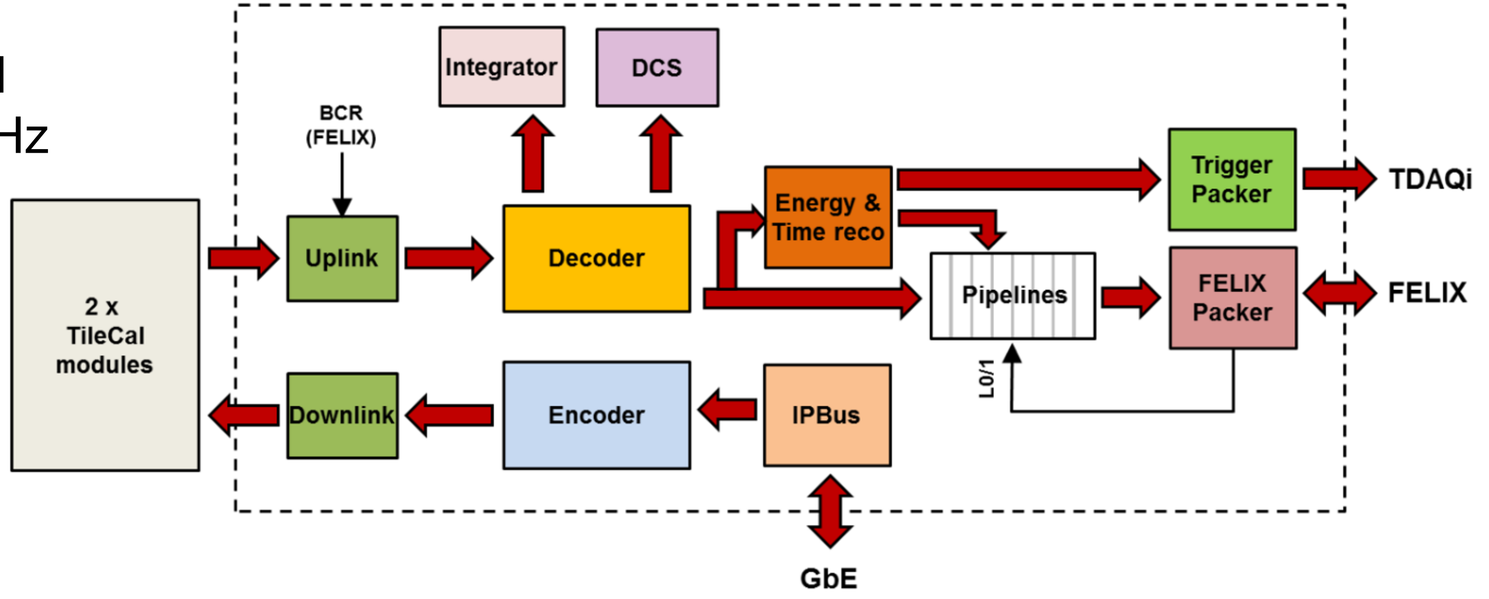


The Compact Processing Module

- Configuration & Control of the On-detector electronics
- LHC Clock recovery & distribution
- Reception of optical signals from the on-detector
- Data processing (cell energy calculation) and calibration for every bunch crossing @ 40 MHz
- Data pipelining & awaiting Trigger decision
- Passes reconstructed cell energies to the TDAQi for trigger prepocessing @ 40 MHz



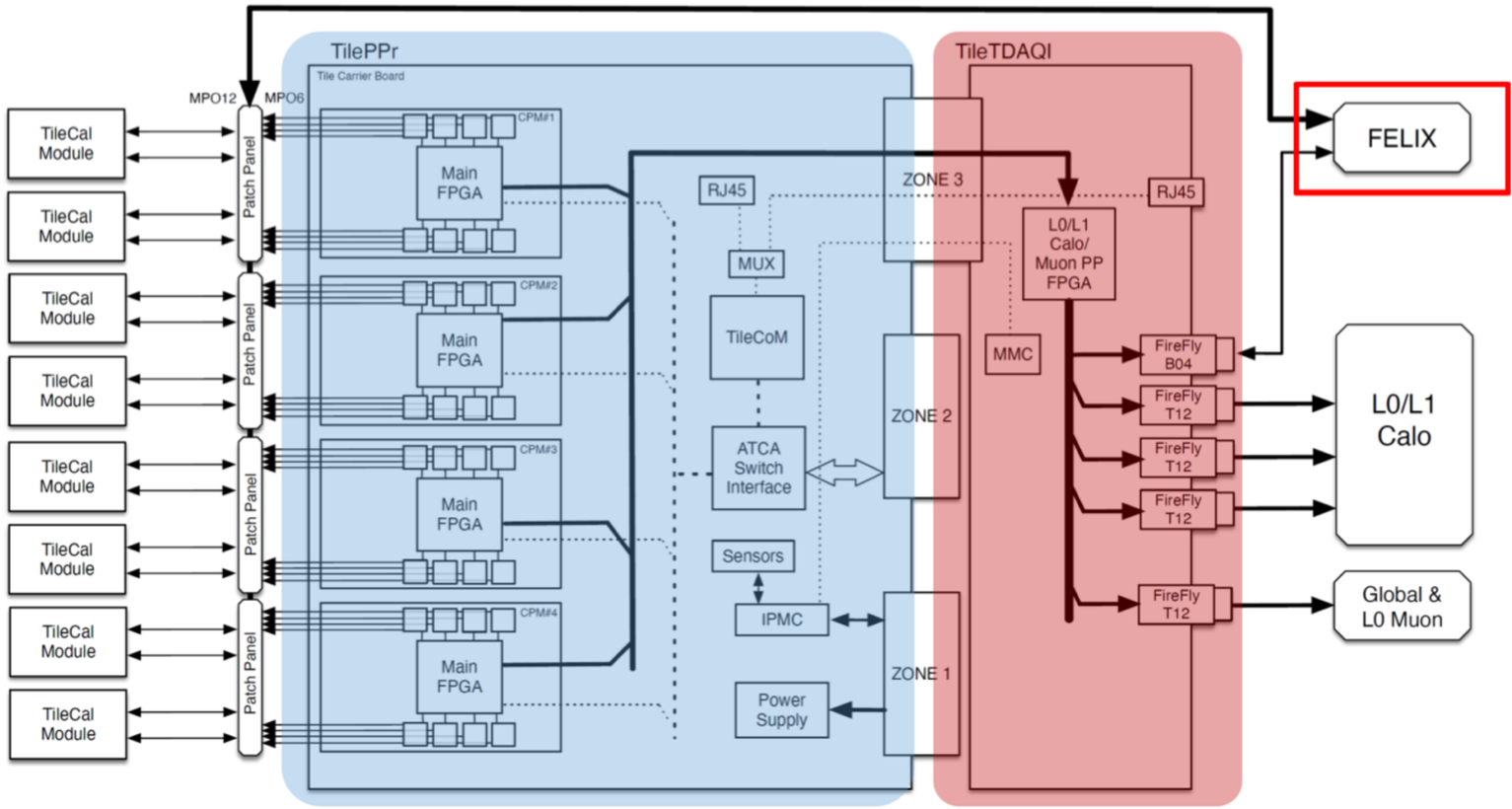
CPM v2



Overview of the CPM Firmware

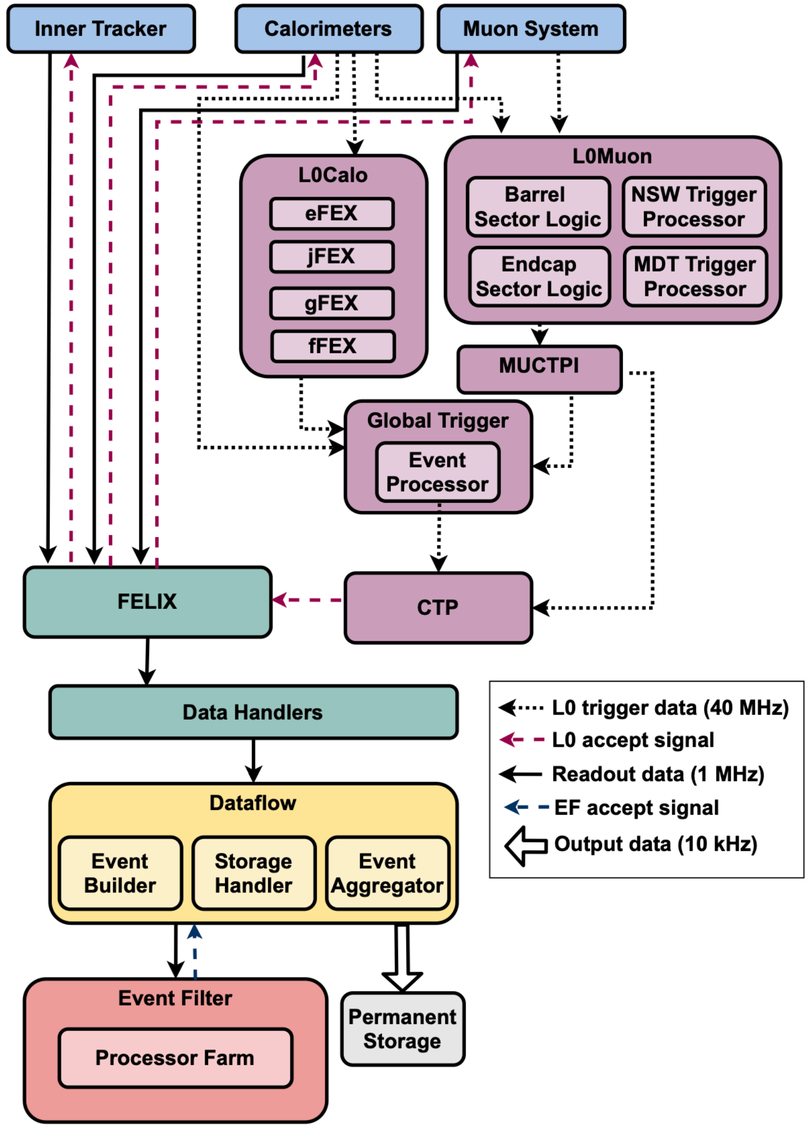
Trigger & Data Acquisition Interface

- The interface between TileCal & the Trigger system
- The last step in the TileCal Off-detector electronics
- Reception of energies from 4 CPMs corresponding to 8 TileCal Modules
- Building of trigger primitive objects
- Transmission of trigger primitives to the ATLAS Trigger System

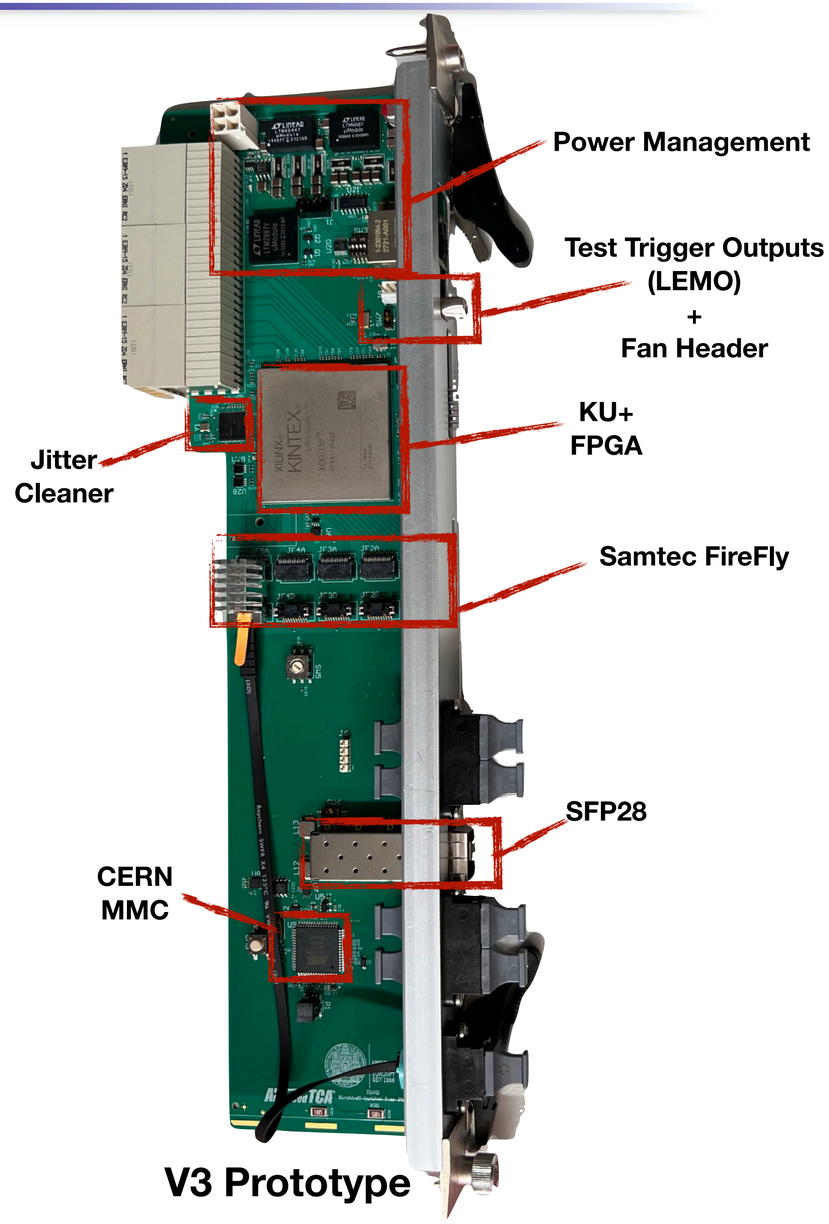


The ATLAS Trigger & Data Acquisition System

- Fully digital Trigger system
- Only optical inputs from the subdetectors
- The Trigger system receives from TileCal:
  - Summed coarse **Trigger-Towers**:
    - L0Calo - Calorimeter Trigger
  - **Cell Energy Flags**:
    - L0Muon - Muon Trigger System
  - **Cell energies**
    - Global Trigger
- Estimated allowed latency of ~**10 µs**
- **1 MHz** Triggering



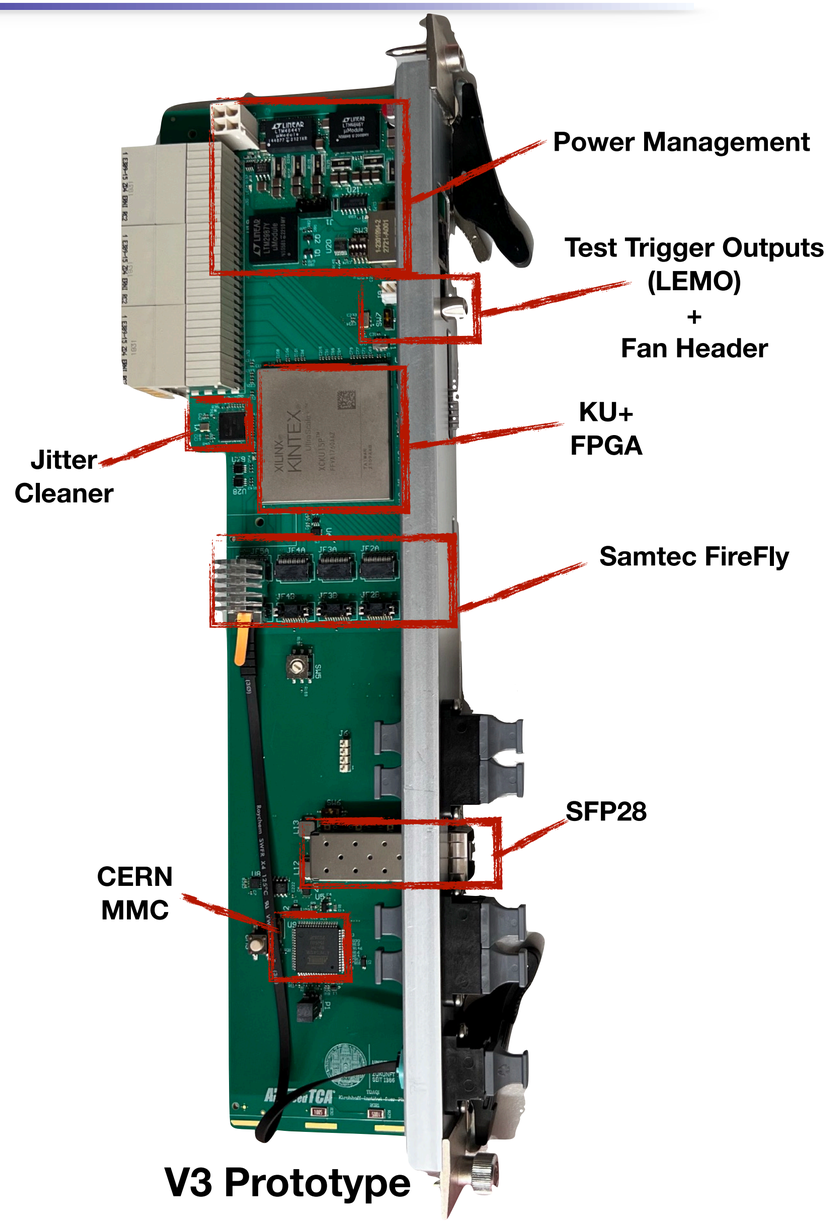
The TDAQi Hardware



V3 Prototype

The TDAQi Hardware

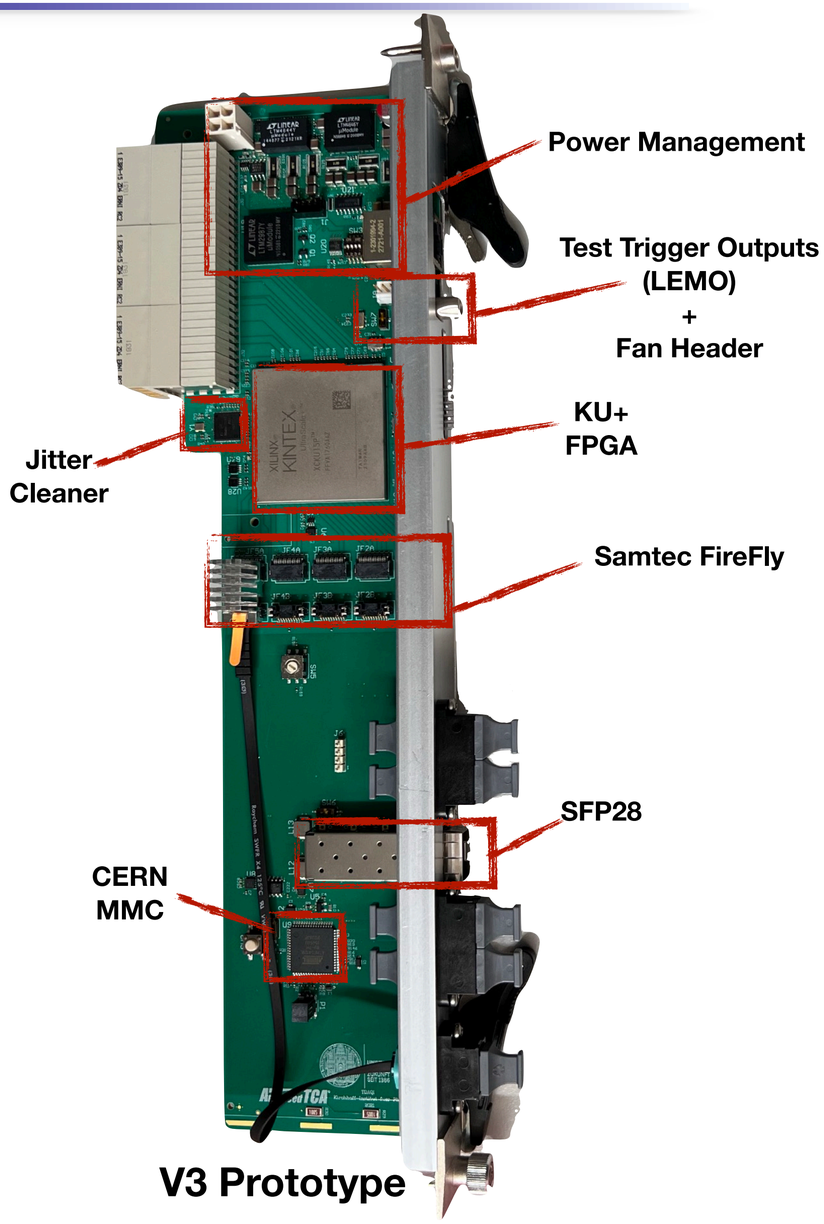
- AdvancedTCA compliant **R**ear-**T**ransition **M**odule



V3 Prototype

The TDAQi Hardware

- AdvancedTCA compliant **R**ear-**T**ransition **M**odule
- Kintex Ultrascale+ FPGA (XCKU15P-2FFVA1760E)
  - Over 1.1 Mil Logic Cells, 34.6 Mb BlockRAM + 36.0 Mb UltraRAM
  - 32 GTY Transceivers
  - 44 GTH Transceivers



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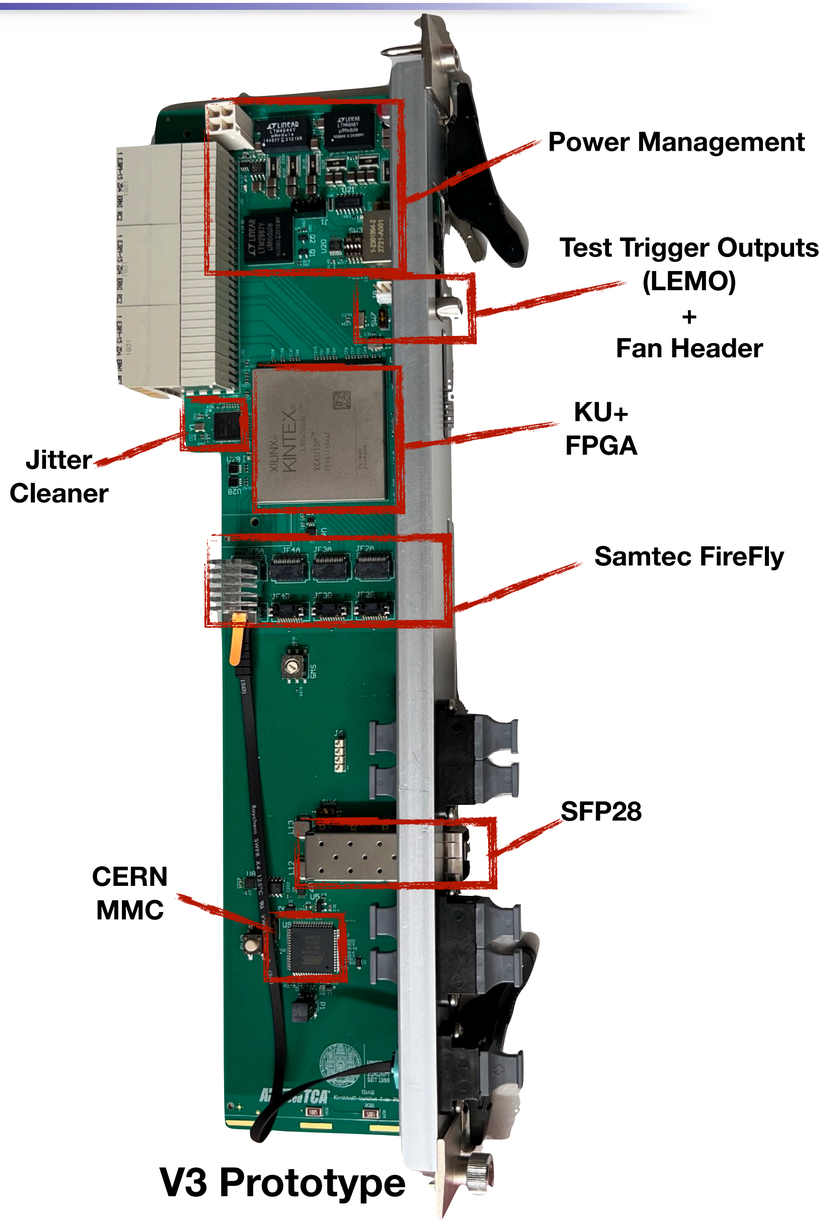
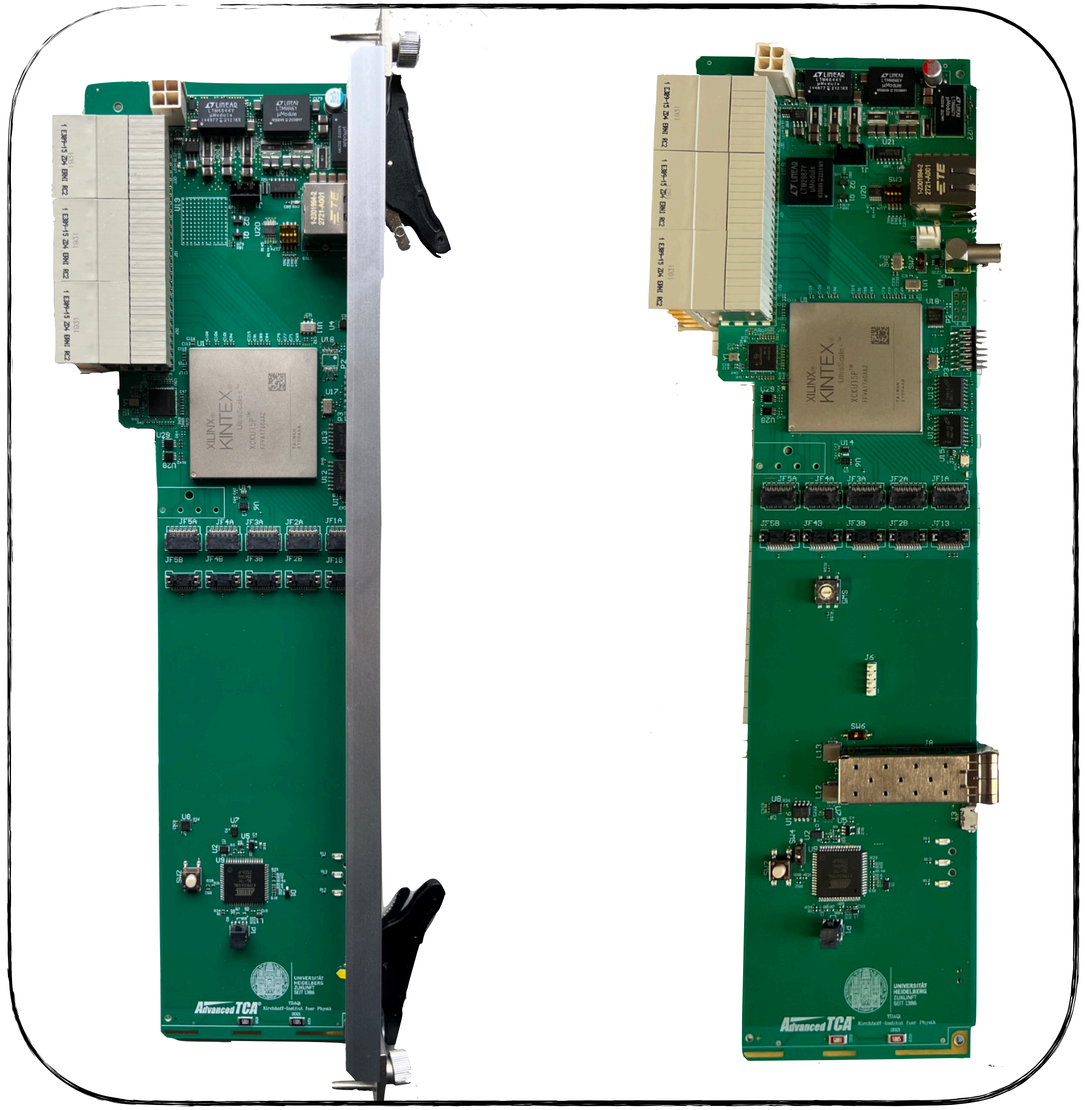
  - Over 1.1 Mil Logic Cells, 34.6 Mb BlockRAM + 36.0 Mb UltraRAM
  - 32 GTY Transceivers
  - 44 GTH Transceivers
- Optical transceivers:
  - 4x Samtec Firefly 12-way transmitters (Up to 16 Gbps)
  - 1x Samtec Firefly 4-way bi-directional transceiver (Up to 14 Gbps)
  - 1x SFP28 (Up to 25 Gbps)



V3 Prototype

The TDAQi Hardware (2)

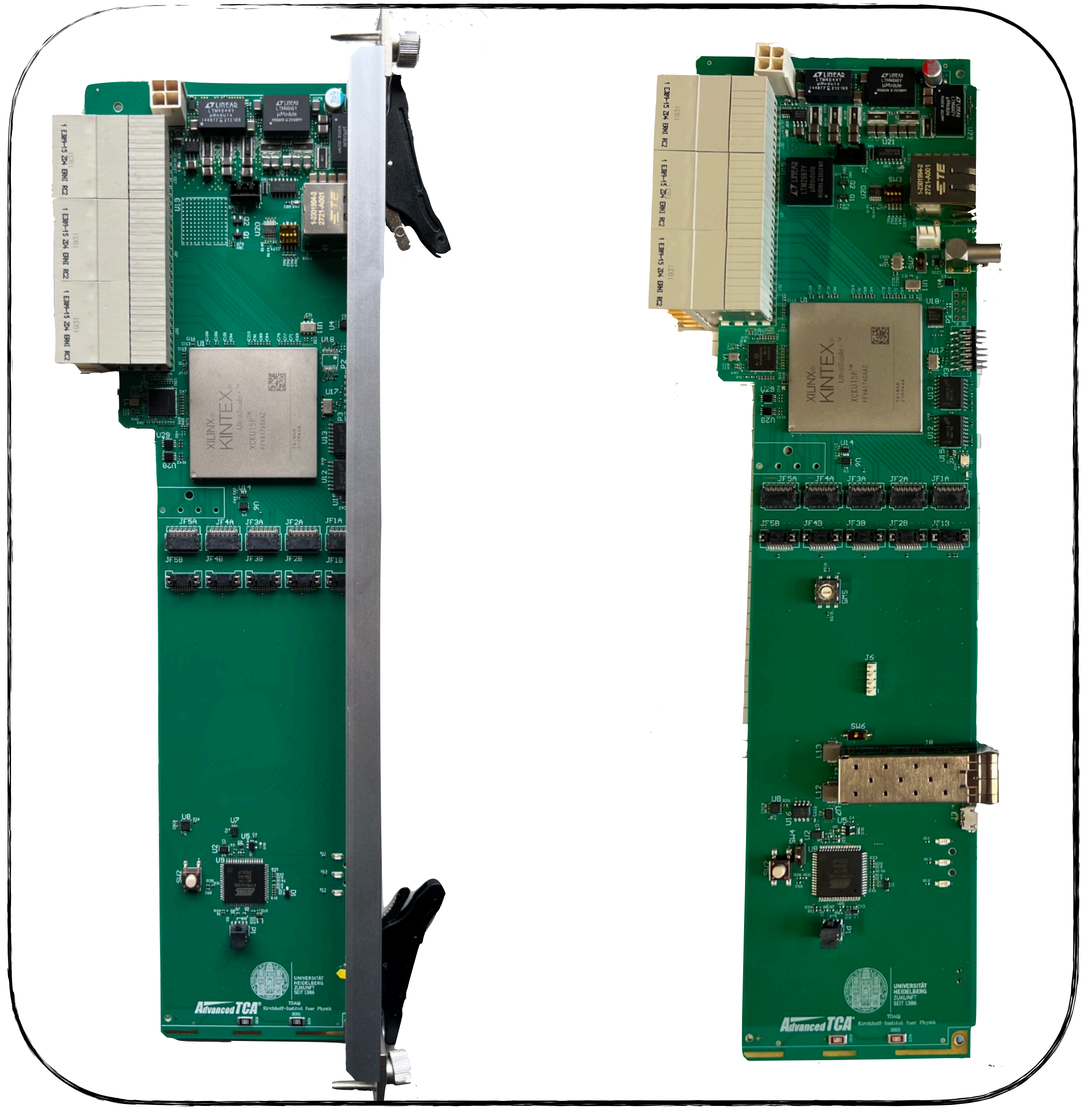


V2 Prototype

V3 Prototype

The TDAQi Hardware (2)

- Multiple revisions of the prototype produced:
  - **2x** TDAQi V1 - proof of principle
  - **4x** TDAQi V2 - full connectivity
  - **2x** TDAQi V3 - final prototype



V2 Prototype **V3 Prototype**

The TDAQi Hardware (2)

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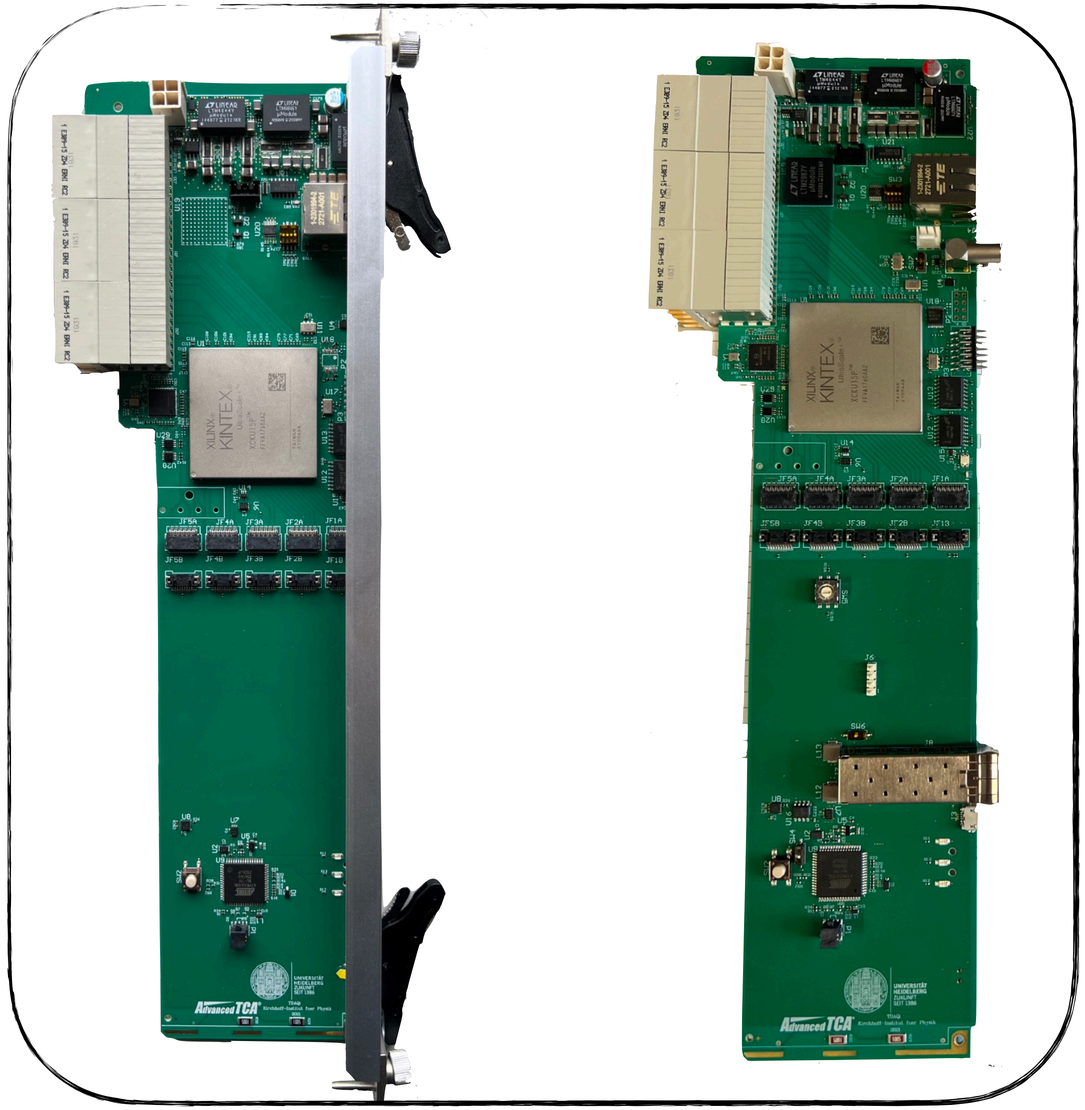
  - **4x** TDAQi V2 - full connectivity
  - **2x** TDAQi V3 - final prototype
- V2 PCBs produced at **2** companies
  - Synamic8GN & IT-968G high-speed dielectric materials
  - Both are high Tg, ultra low-loss, halogen free
  - No difference observed in testing



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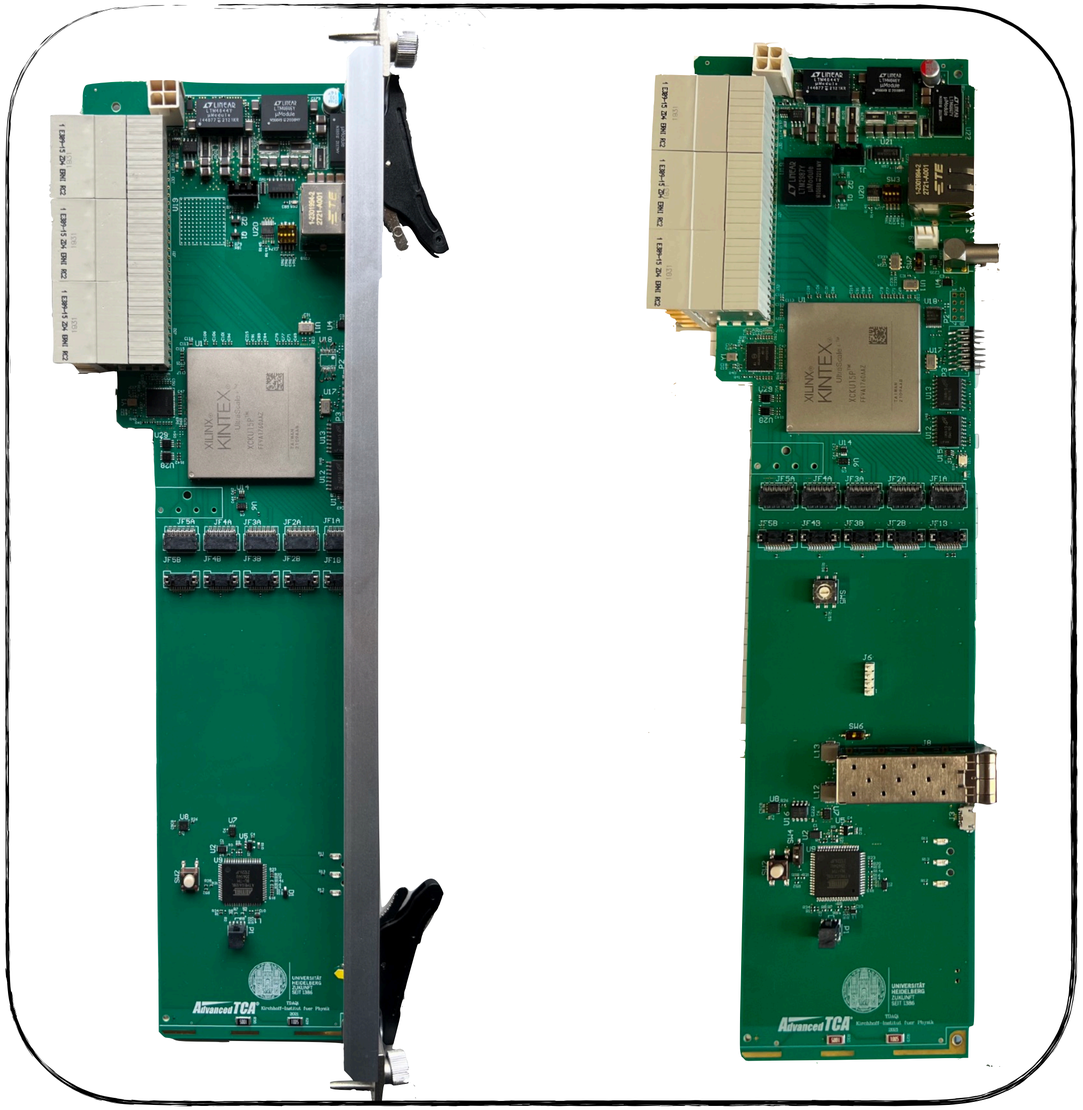
- V3 uses Synamic8GN - **14** layers - dense high-speed routing



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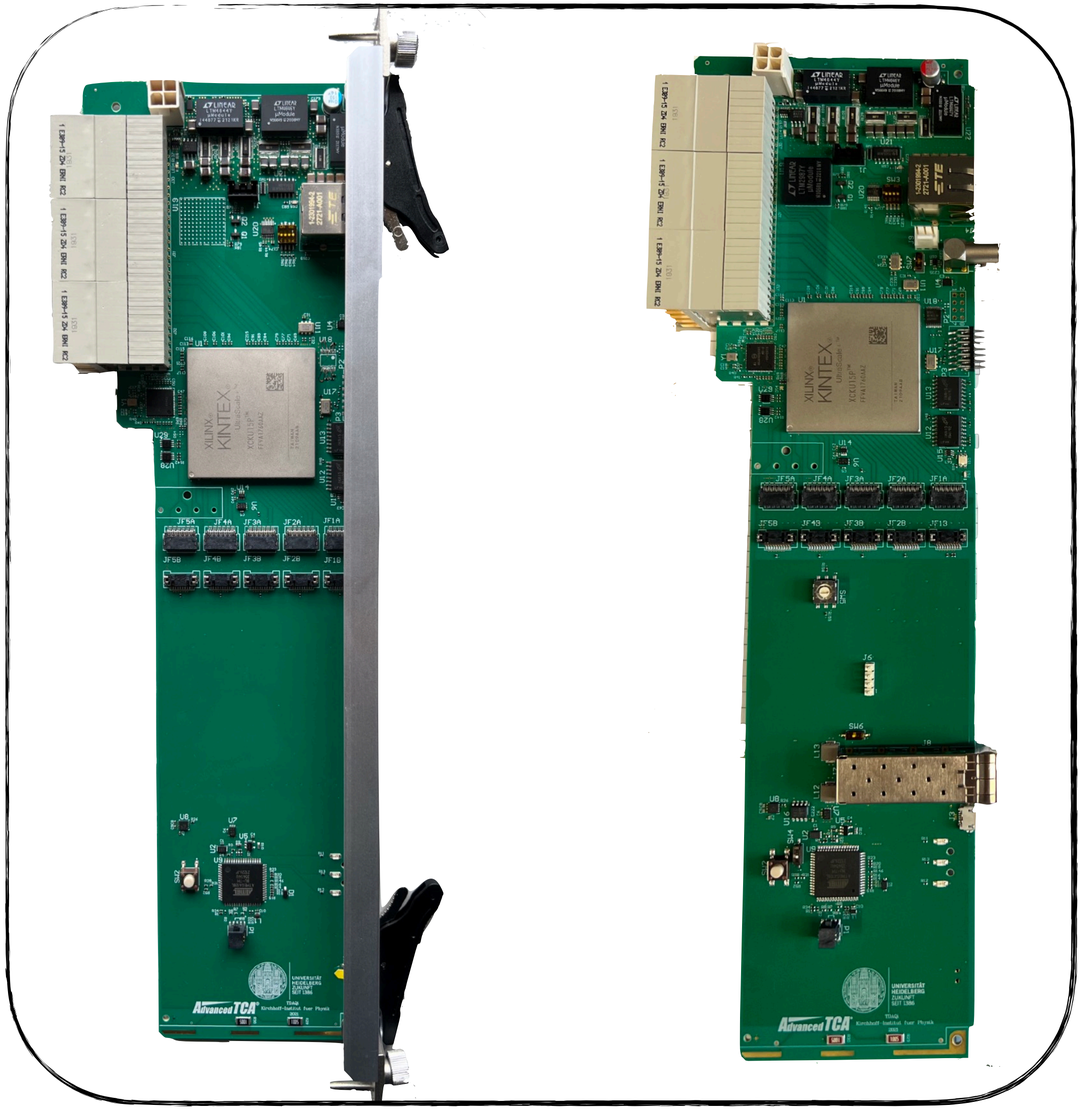

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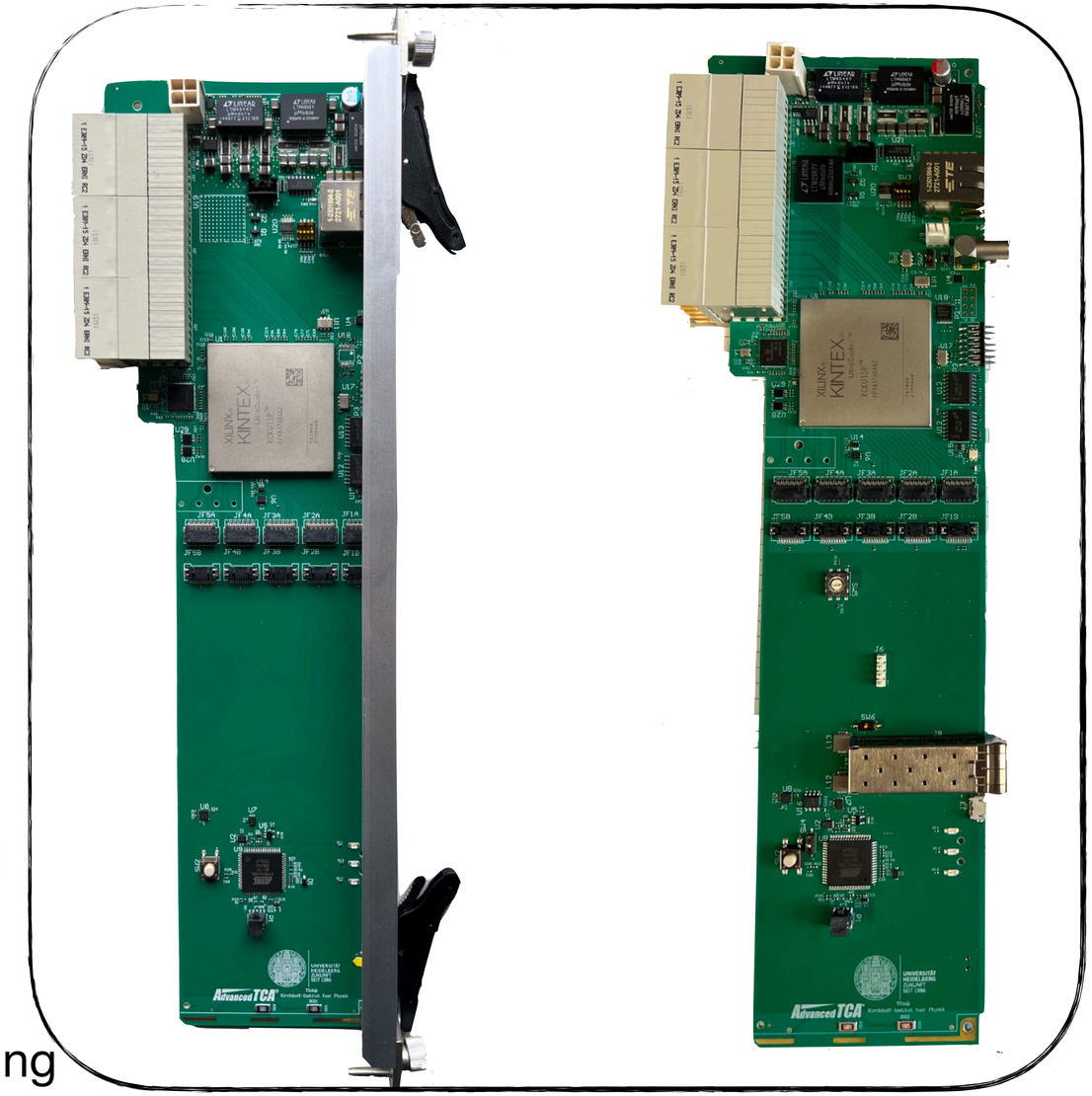
- V2 PCBs produced at **2** companies
  - Synamic8GN & IT-968G high-speed dielectric materials
  - Both are high Tg, ultra low-loss, halogen free
  - No difference observed in testing
- V3 uses Synamic8GN - **14** layers - dense high-speed routing
- Initial procurement and assembly issues - now resolved
- All modules functional; minor patching performed for regulating IR drop, active cooling, hot-swap switch

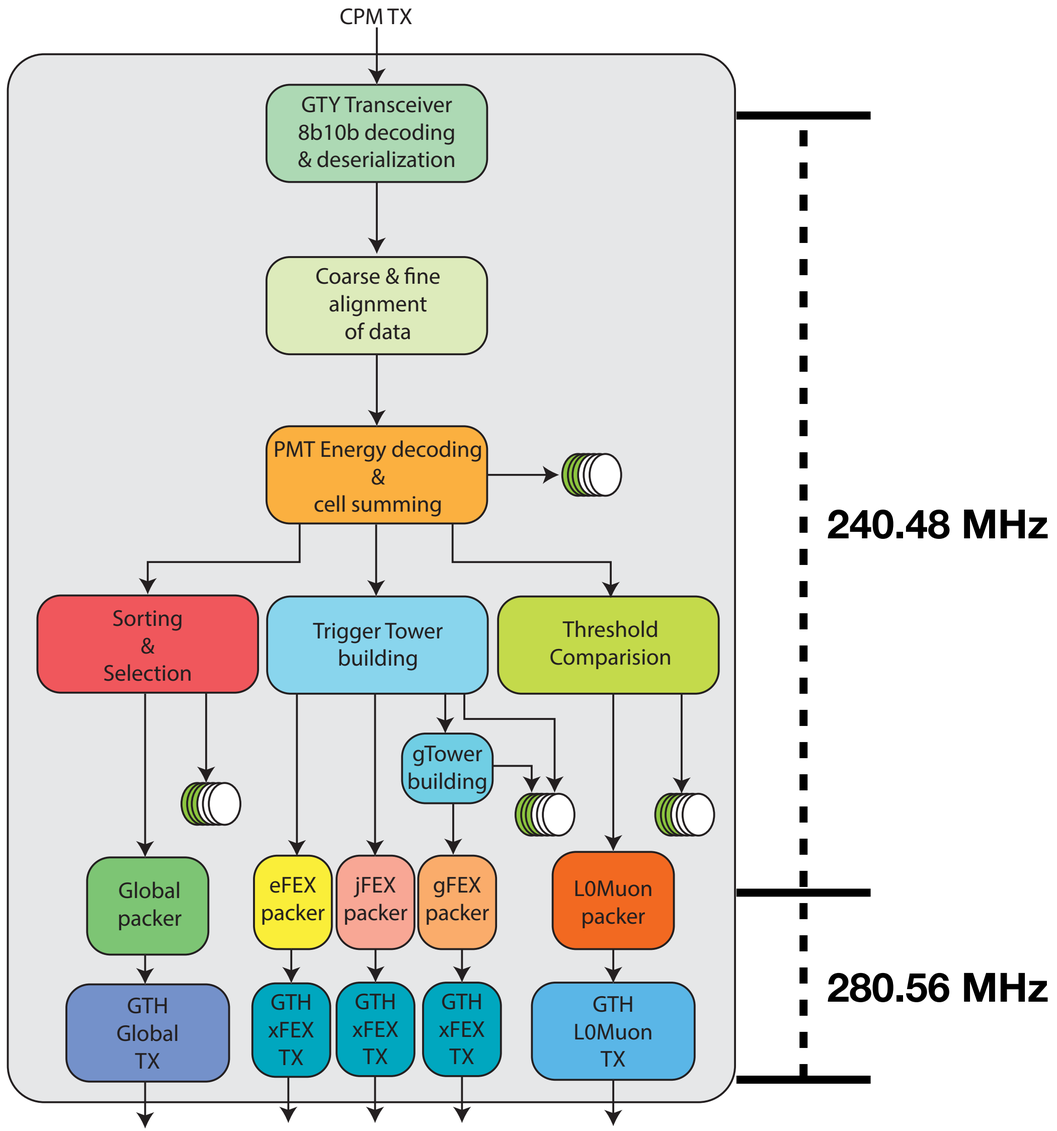


V2 Prototype **V3 Prototype**

Realtime Data Path

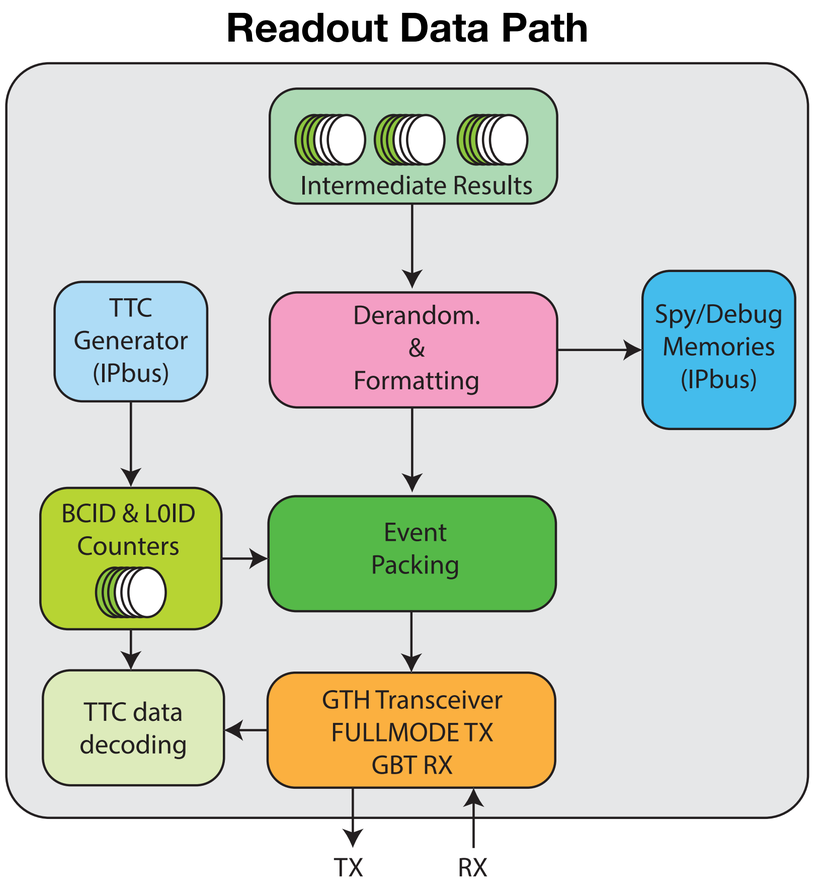
- Synchronous with the LHC clock (40.08 MHz)
- Data processing on the Trigger path
- Multiple stages of processing algorithms
  - Driven by a 240.48 MHz clock
- Each Trigger subsystem has a unique data object requirement
- Final stage of data packing performed with a 280 MHz clock:
  - Careful Clock-Domain-Crossing from 240.48 to the 280.56 MHz domain
  - Maintain fix and deterministic latency

Trigger (Realtime) Data Path of the TDAQi



Readout & TTC Path

- Intermediate results of the realtime path are buffered up to 10 us
- Upon a trigger decision, the results are transferred to the ATLAS DAQ (FELIX)
- Max. rate of 1 MHz
- Derandomization, Formatting & Packing logic driven with the synchronous 240.48 MHz clock
- Trigger, Timing & Control information retrieved from FELIX via the RX link
  - Current Protocol: GBT @ 4.8 Gbps
  - To switch to LTI-FE 8b/10b @ 9.6 Gbps

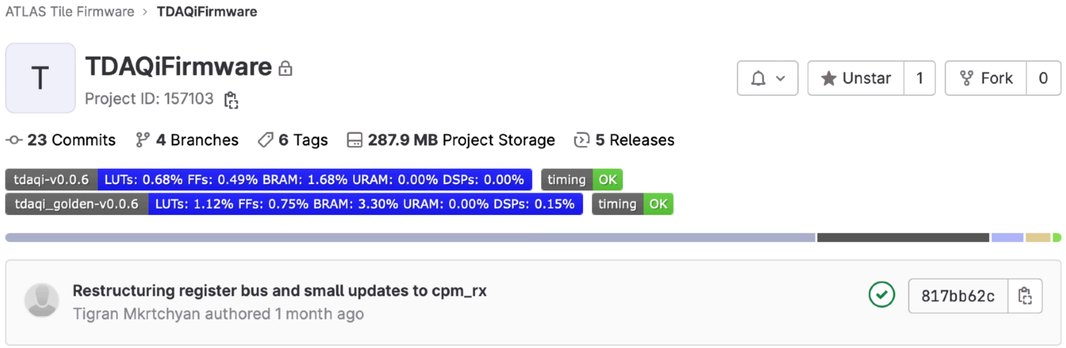


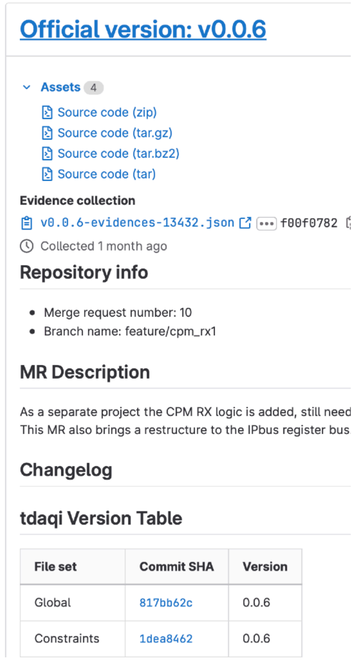
System Monitoring

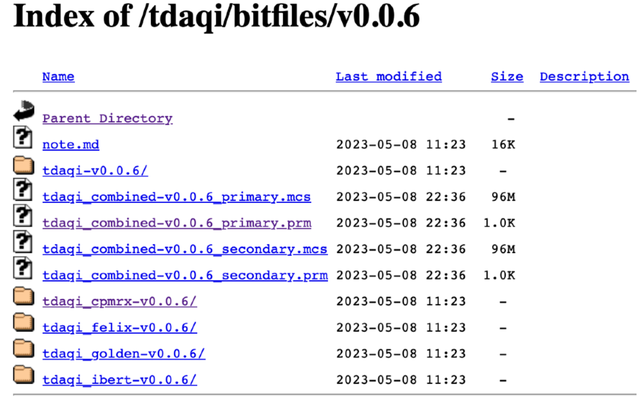
- RTM power consumption rated up to **max. 50 Watts per slot**
- V3 prototypes consume **43 Watts** on full load
- Temperatures stable inside ATCA shelf running on mid fan (8) settings
  - FPGA: 30° C (average); 50° C (max)
  - FireFly: 37° C (average); 45° C (max)
- MGT and internal voltages stable
- Framework to read all Tile off-detector electronics and visualise with Grafana at CERN

Firmware Management

- The TDAQi FW is available within the Tile FW group on Gitlab: https://gitlab.cern.ch/atlas-tile-firmware
- Automatic FW build release packing when pushed to master
  - Based on HOG
- All artefacts and version/timing info available on release page
- Files hosted on EOS with web access for convenience
- Single Flash memory file containing **5** different FW designs
  - Golden image with 4 additional user images
  - Seamless switching between FW via software commands





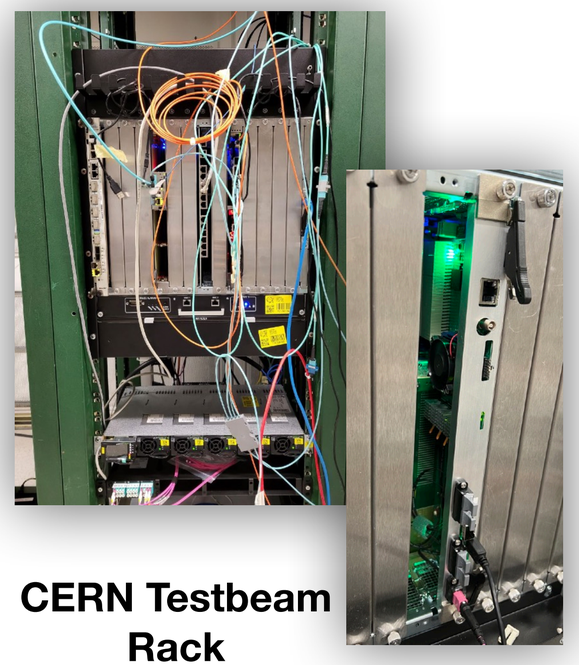


Files on EOS web
https://tilefw.web.cern.ch/tdaqi/

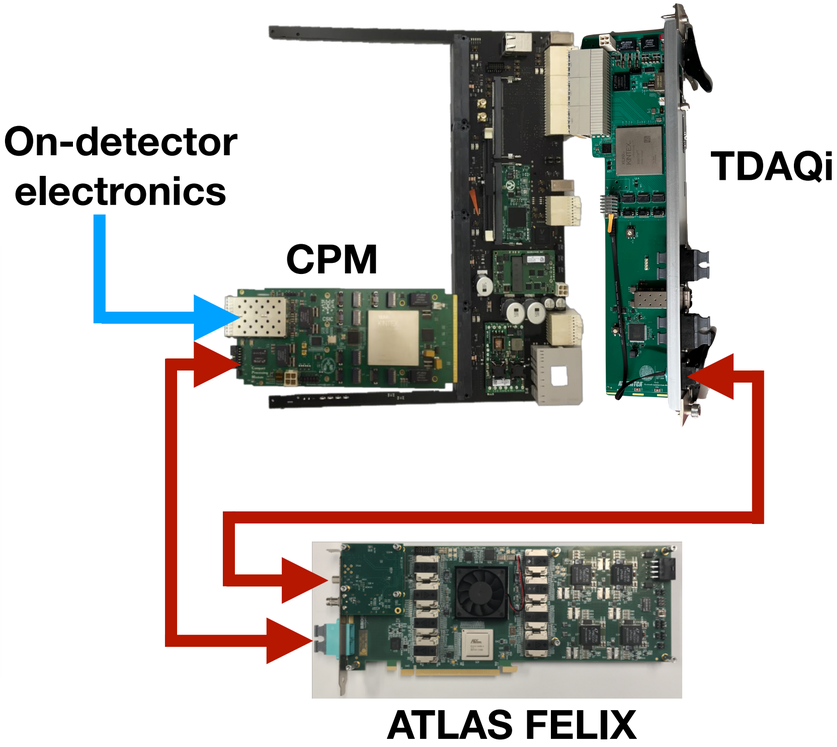
System Integration

- Multiple test-benches with the off-detector electronics
  - **CERN**: Lab and Testbeam (SPS North Area)
  - **KIP** Heidelberg
  - **IFIC** Valencia

CERN Lab Testbench



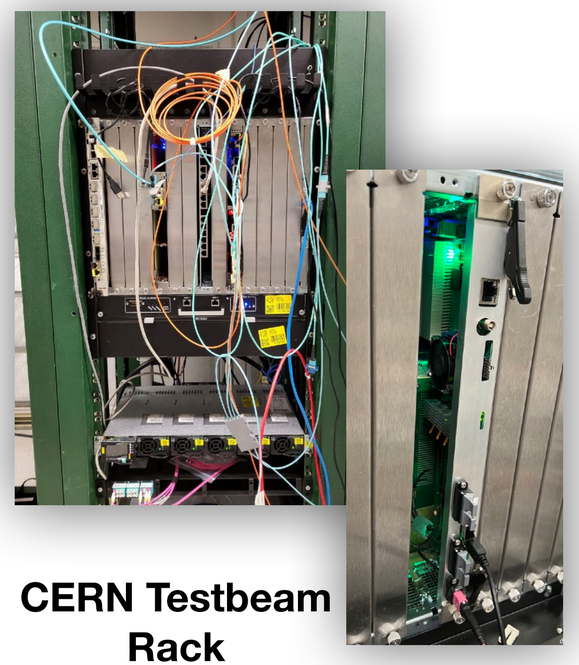
CERN Testbeam Rack



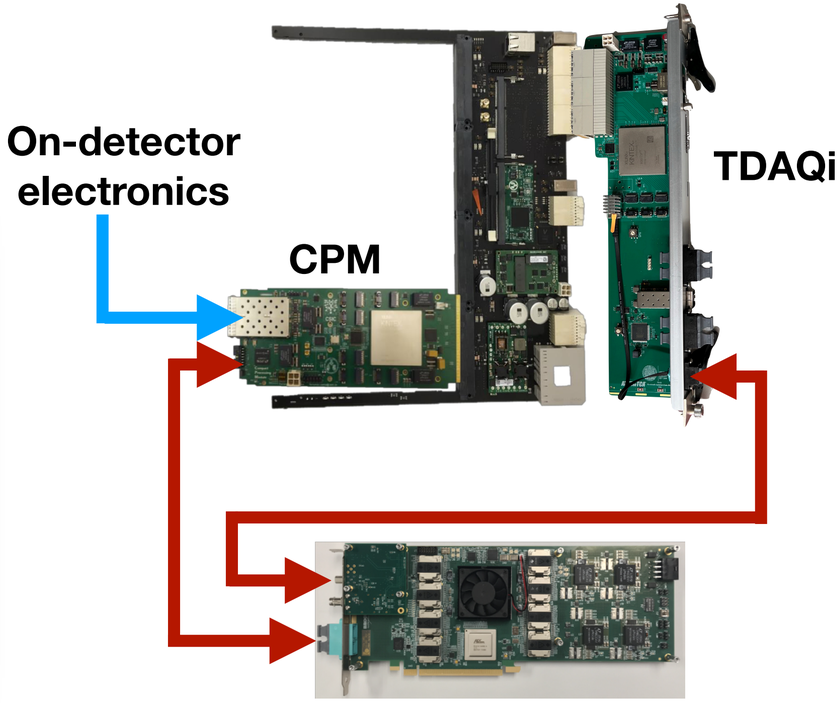
System Integration

- Multiple test-benches with the off-detector electronics
  - **CERN**: Lab and Testbeam (SPS North Area)
  - **KIP** Heidelberg
  - **IFIC** Valencia
- Vertical slice at the Testbeam
- Use of real beam data to validate the full trigger chain
- ATLAS Infrastructure (clock distribution & control software)

CERN Lab Testbench



CERN Testbeam Rack

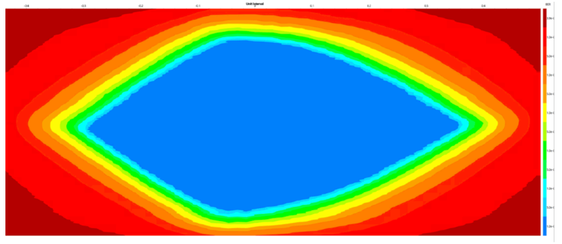


Signal Integrity

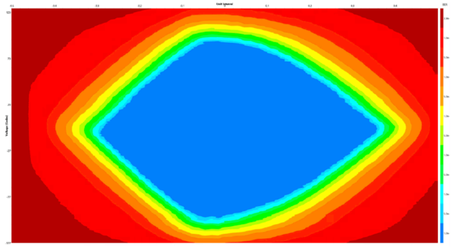
- BER tests performed for all transceivers
- FireFly transmission tested with special receiver board
  - Equipped with 14G RX FireFly
  - Soak tests with BER < 10^{-15}
- CPM -> TDAQi links
  - Eye scans captured on TDAQi
  - 95% of links have good eye openings
  - AMC & RTM connectors optimised in the next revision

Example channels:

FireFly 1

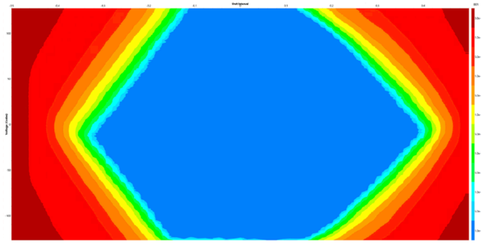


FireFly 2

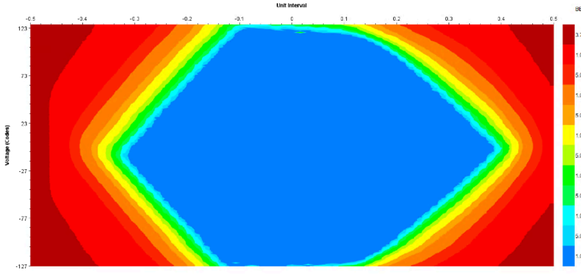


Optical @ 11.2 Gbps

FireFly 3

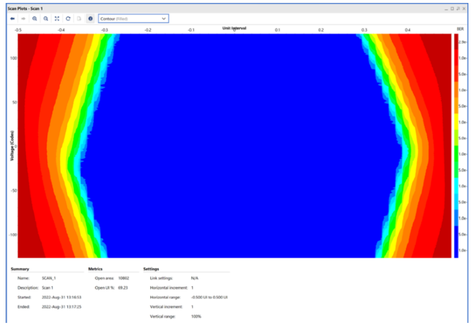


FireFly 4

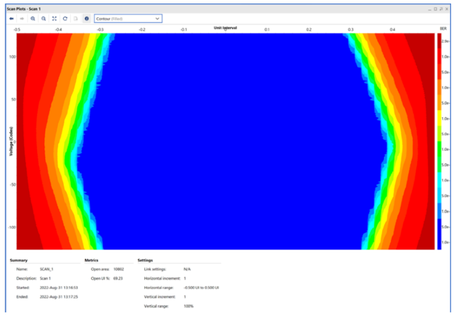


Electrical @ 9.6 Gbps

AMC 1

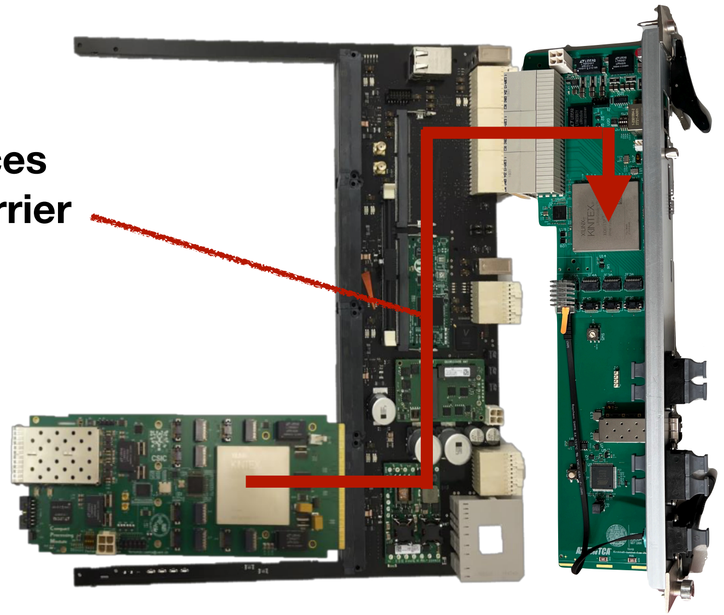


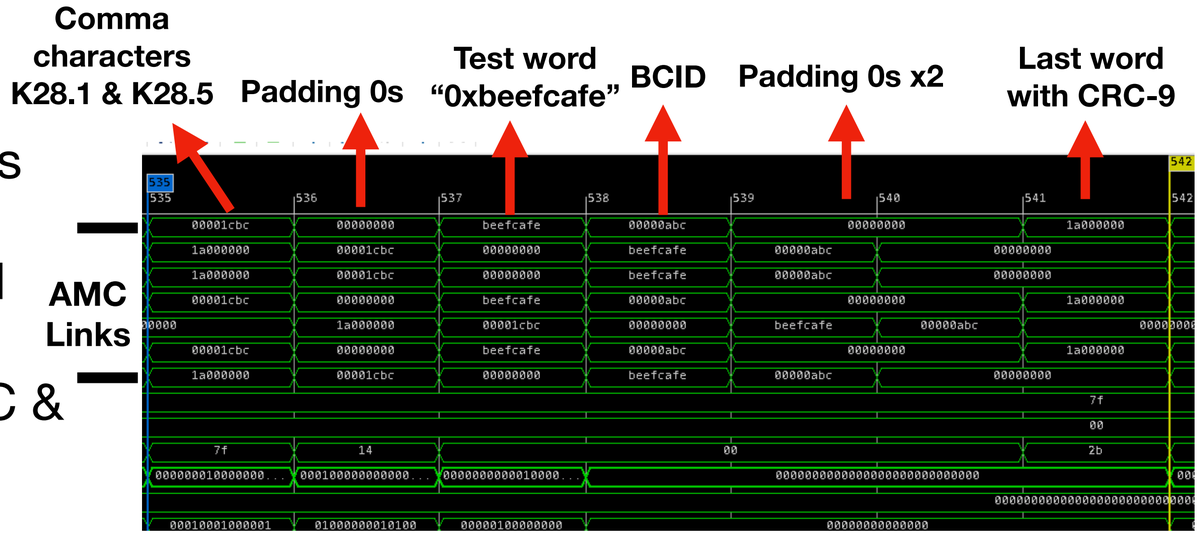
AMC 2



System Integration (CPM -> TDAQi)

- Receiving Test Frame with basic information
- 6x 32-bit words @ 240.48 MHz = **9.6 Gbps**
- 7 transmitter links with identical information
- Asynchronous 240.48 MHz reference clocks on both sides
- Counters with ramp patterns
- No 8b/10b decoding errors seen in single channel tests
- CRC/decoding error monitoring counters implemented
- Long signal traces on the carrier, passing through AMC & Zone 3 connectors





TDAQi Connectivity

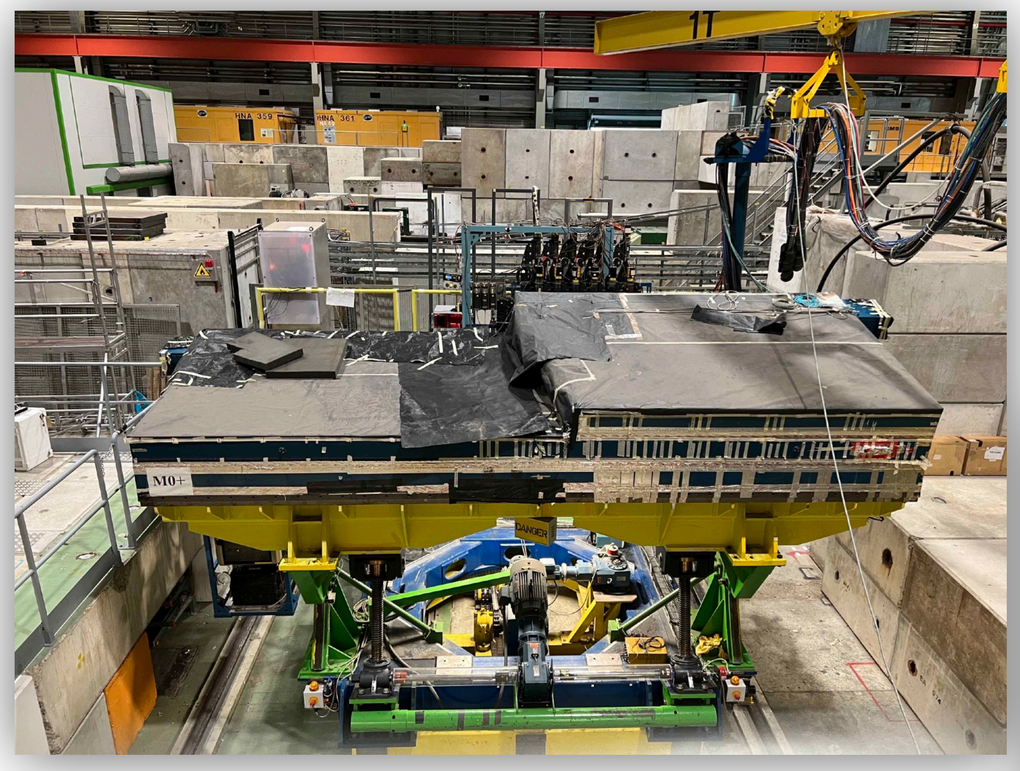
- **70** Operational links
  - **41** Transmitter links
  - **29** Receiver links
- 2 link speeds:
  - 9.6 Gbps
  - 11.2 Gbps
- 8b/10b encoding for all TX links
- Spare links available:
  - 12 TX to AMCs
  - 1x SFP28 (up to 25 Gbps)

Module	Type	Links	Speed (Gbps)	Encoding
CPMs	TX/RX	4 x 7 RX / 3 TX*	9.6	8b/10b
eFEX	TX	12	11.2	8b/10b
jFEX	TX	12	11.2	8b/10b
gFEX	TX	1 + 1	11.2	8b/10b
L0Muon	TX	6	9.6	8b/10b
Global	TX	8	11.2	8b/10b
FELIX	TX/RX	1 RX / 1 TX	9.6	RX LTI-FE / TX 8b/10b

* Used for debug purposes

Summary

- Three iterations of prototypes produced & tested
  - **2x** V1, **4x** V2, **2x** V3 TDAQi
  - ✓ Overhauled power management and full connectivity
  - ✓ Stable thermal and power performance
- System reaching **pre-production** state
- Firmware progressing well with key blocks in place
  - CI & deployment available
- Planned integration tests with Trigger systems
- Defining final data formats



TileCal Testbeam

TDAQi at the Testbeam