Contribution ID: **85** Type: **Oral**

The Trigger & Data Acquisition interface module of the Tile Calorimeter for the ATLAS Phase- II Upgrade

Thursday 5 October 2023 09:40 (20 minutes)

For the High Luminosity-Large Hadron Colider (HL-LHC) phase, the ATLAS Tile Calorimeter (TileCal) is undergoing a major upgrade with a complete redesign of the on- and off-detector electronics. In the new readout architecture, the calorimeter signals are digitised every 25 ns directly on-detector and transferred to the off-detector Tile PreProcessor (TilePPr) via high-speed optical links. The TilePPr reconstructs the energies from the digitised samples and transfers them through its Trigger & Data Acquisition interface (TDAQi) module to the ATLAS Trigger & DAQ system via fixed and deterministic high-speed optical links at speeds of 11.2 Gbps.

Summary (500 words)

The High Luminosity-Large Hadron Collider (HL-LHC) is a planned upgrade that will increase the instantaneous luminosity by a factor of 5 larger than the LHC's nominal value.To overcome the challenges imposed by the HL-LHC environment and to adapt to the new ATLAS readout architecture, the ATLAS Tile Calorimeter (TileCal) is undergoing a major upgrade with a complete redesign of the on- and off-detector electronics.
In the new readout architecture, the calorimeter signals are digitised every 25 ns directly on-detector and transferred to the off-detector Tile PreProcessor (TilePPr) via high-speed optical links. The TilePPr reconstructs the cell energies from the digitised samples, performs the energy calibration and transfers them to the ATLAS Trigger & DAQ system, all within strict latency requirements.
Within the TilePPr, system, the Tile Trigger & DAQ interface (Tile TDAQi) module receives the reconstructed cell energies and applies summing, sorting and grouping algorithms to build trigger primitives at a rate of 40 MHz. The formatting of the trigger primitives is tailored to the requirements of the various trigger subsystems of ATLAS.
One of the biggest challenges is the latency minimisation for each step of the processing implementation in the TDAQi. High optimisation is required for delivering the trigger inputs to the electron/photon and jet trigger systems (L0Calo), the muon-based trigger system (L0Muon) and to the ATLAS Global Trigger system.
The TDAQi is an FPGA-based Advanced Telecommunications Computing Architecture (ATCA) Rear Transition Module (RTM), operating under the ATCA framework. Consisting of a 14-layer PCB, the TDAQi is equipped with over 70 high-speed transceivers which operate at speeds up to 11.2 Gbps.
An overview of the TileCal electronics upgrade is given along with the latest implementation of the TDAQi prototype. The recent hardware and integration tests results are discussed as well as the next steps.

Author: MKRTCHYAN, Tigran (Heidelberg University (DE))

Presenter: MKRTCHYAN, Tigran (Heidelberg University (DE))

Session Classification: Module, PCB and Component Design

Track Classification: Module, PCB and Component Design