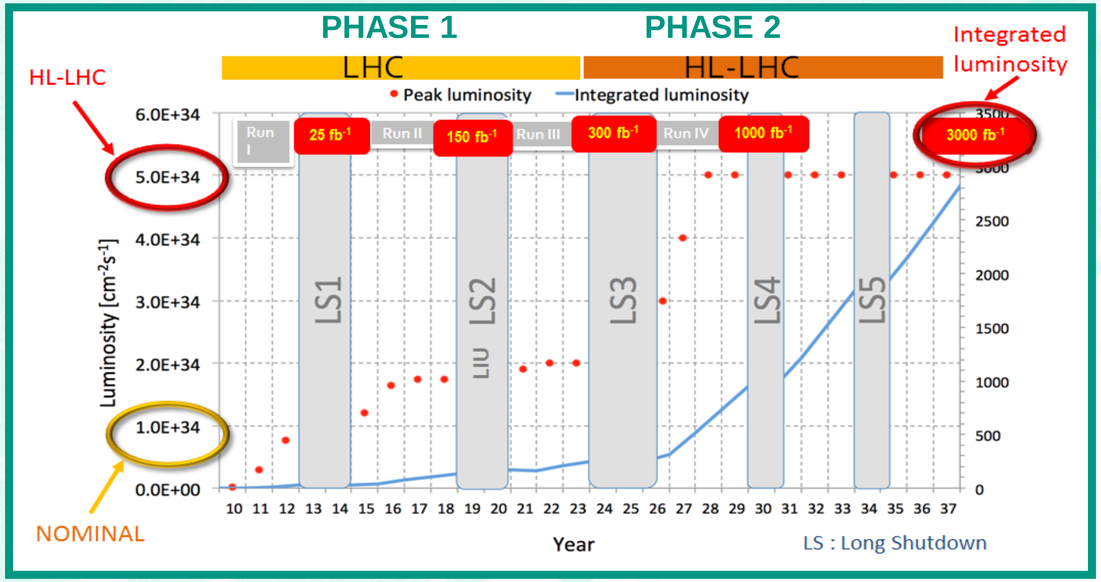
The OBDT-theta board:

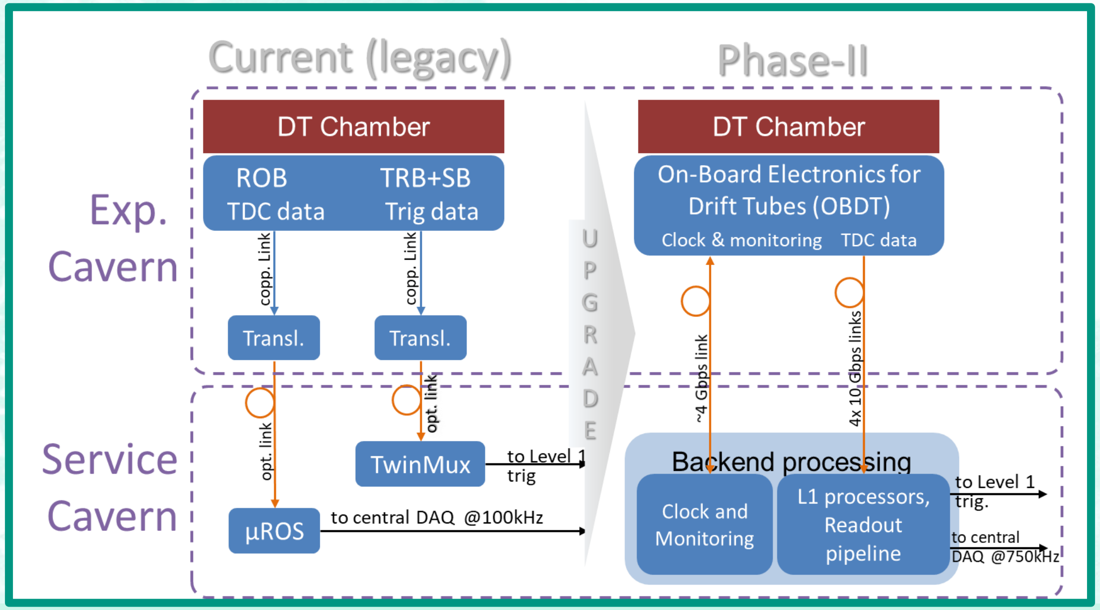
Time digitization for the theta view of Drift Tubes chambers.

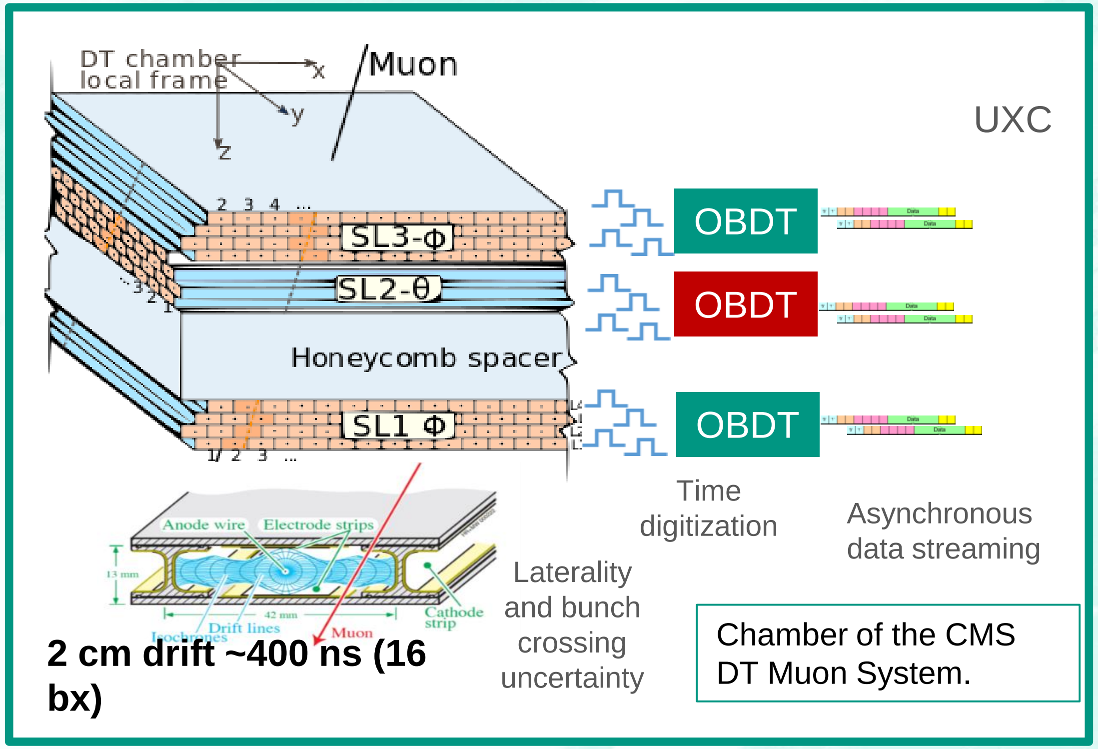
J. Sastre, C.F. Bedoya, S. Cuadrado, J. Cuchillo, D. Francia, C. de Lara, A. Navarro, R. Paz, I. Redondo, D. Redondo.

On behalf of the muon group

Overview







10 x integrated luminosity

7.5 x instantaneous luminosity

- Hw trigger rate will increase from 100kHz to up to 750 kHz
- Present CMS DT electronics needs to be redesigned (present limit is 300 kHz)

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Overview

Requirements

- New detector electronics **to replace** electronics in present Minicrates, attached to DT chambers.
- OBDT in charge of **time digitization** of the chamber signals from the theta superlayer. Front End cables cannot be replaced during installation in LS3.
- **Time resolution** needed of 1 ns.
- Forwards full detector time information in **streaming mode** (no filtering) through lpGBT links (optical links).
- It has to include the chamber legacy **detector control logic**:
  - Control of the Front End Boards.
  - Test pulse generation (calibration of the time measurements).
  - detector control services for the PADC, RPC(secondary) and alignment systems.
  - Monitoring of the DT chamber sensors (temperature, pressure,…).
- **Reduce complexity** in the detector and bring to the control room all of the complex logic (such as event matching or trigger primitive generation).
- **60% power consumption** with respect to present system (estimated total power: < 12 W).
- **Redundancy.** Spare links for both detector control and readout.

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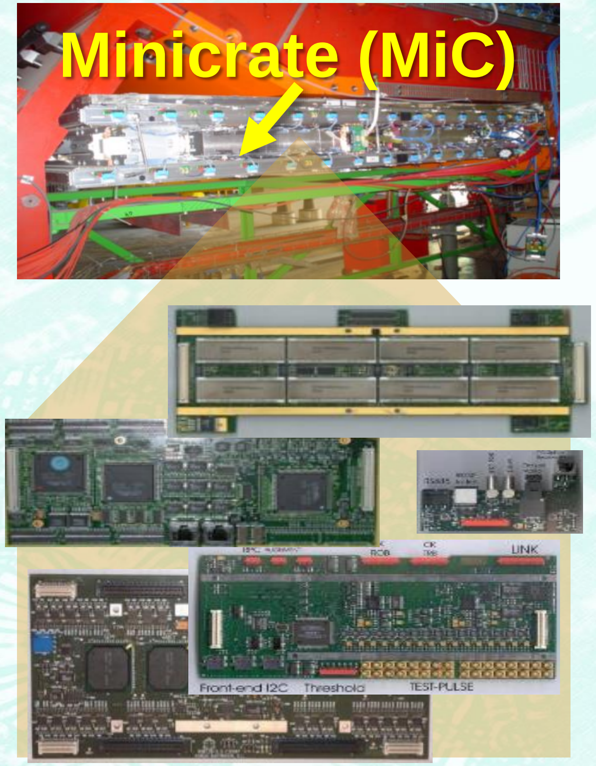
Overview

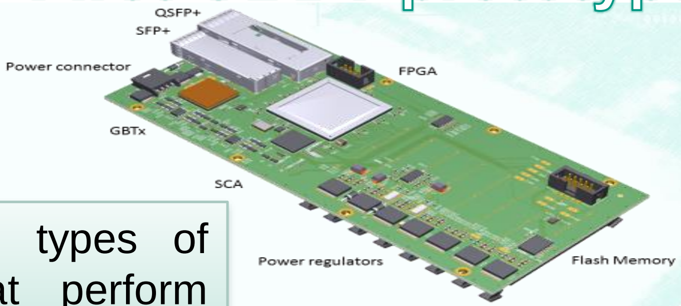
HL-LHC R&D: OBDT prototype

UP TO LS3
(PHASE 1)

HL-LHC
(PHASE 2)



First OBDT prototype



Two single types of boards that perform full streaming of all hits with 1 ns LSB

OBDT-theta

HOSTED IN MIC2

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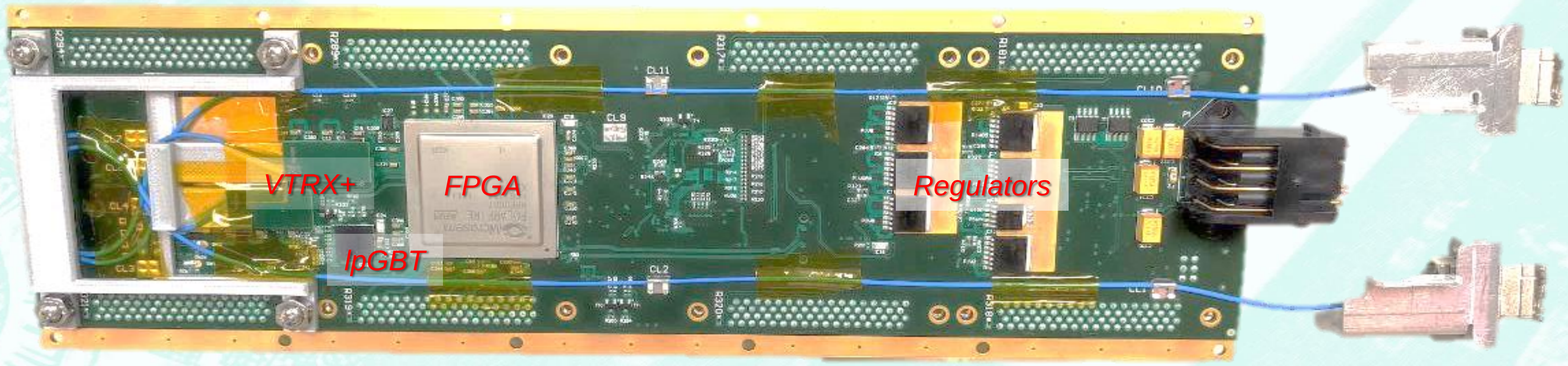
OBDT-theta board

Main components



BOTTOM VIEW

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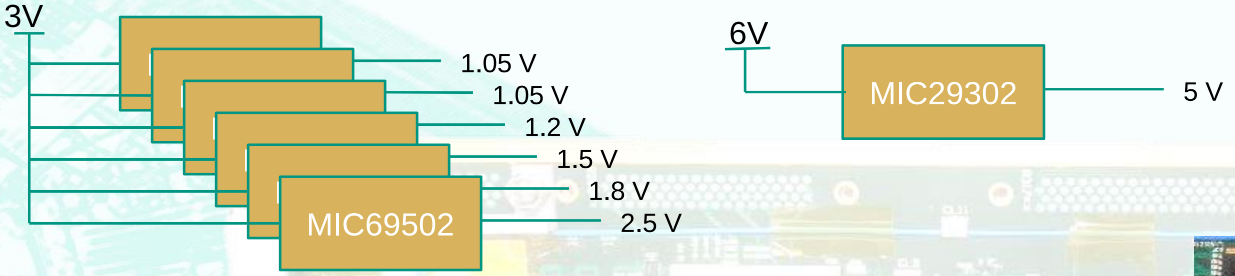
OBDT-theta board

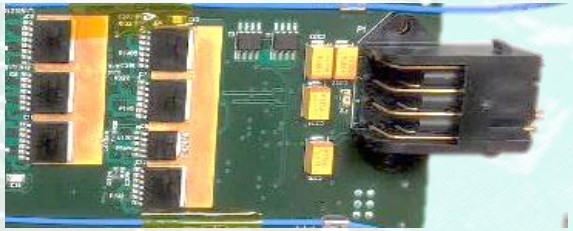
Safety system

- **Detector Safety System**: overcurrent, overvoltage and overtemperature protection embedded on the OBDT-theta. An alarm signal is generated and sent to MONSA system if any of these circumstances appear. MONSA (in the tower racks) can force deactivating the power of the OBDTs.
- If the OBDT DSS system is activated, the DSS logic enables the linear regulators that power the board electronics

Power distribution



Regulators



- Estimated total power: < 12 W.
- 2 power supply rails, (3 V and 6 V).
- Using low drop linear regulators to minimize noise.

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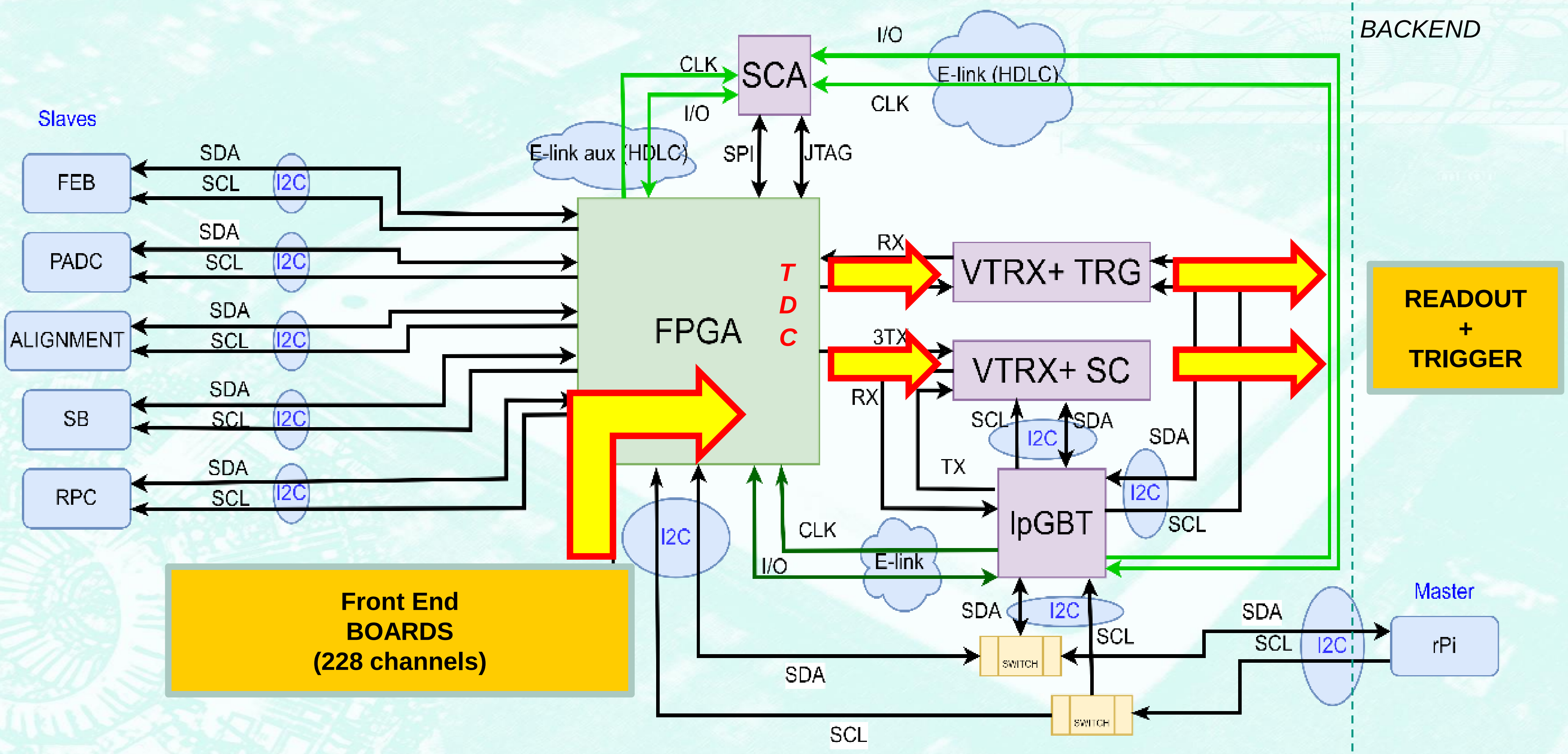
OBDT-theta board

Board that performs the <1 ns time digitization in FPGA of the chamber signals.
Core of the new on detector electronics, inserted into the MiC2 system, attached to the DT chambers



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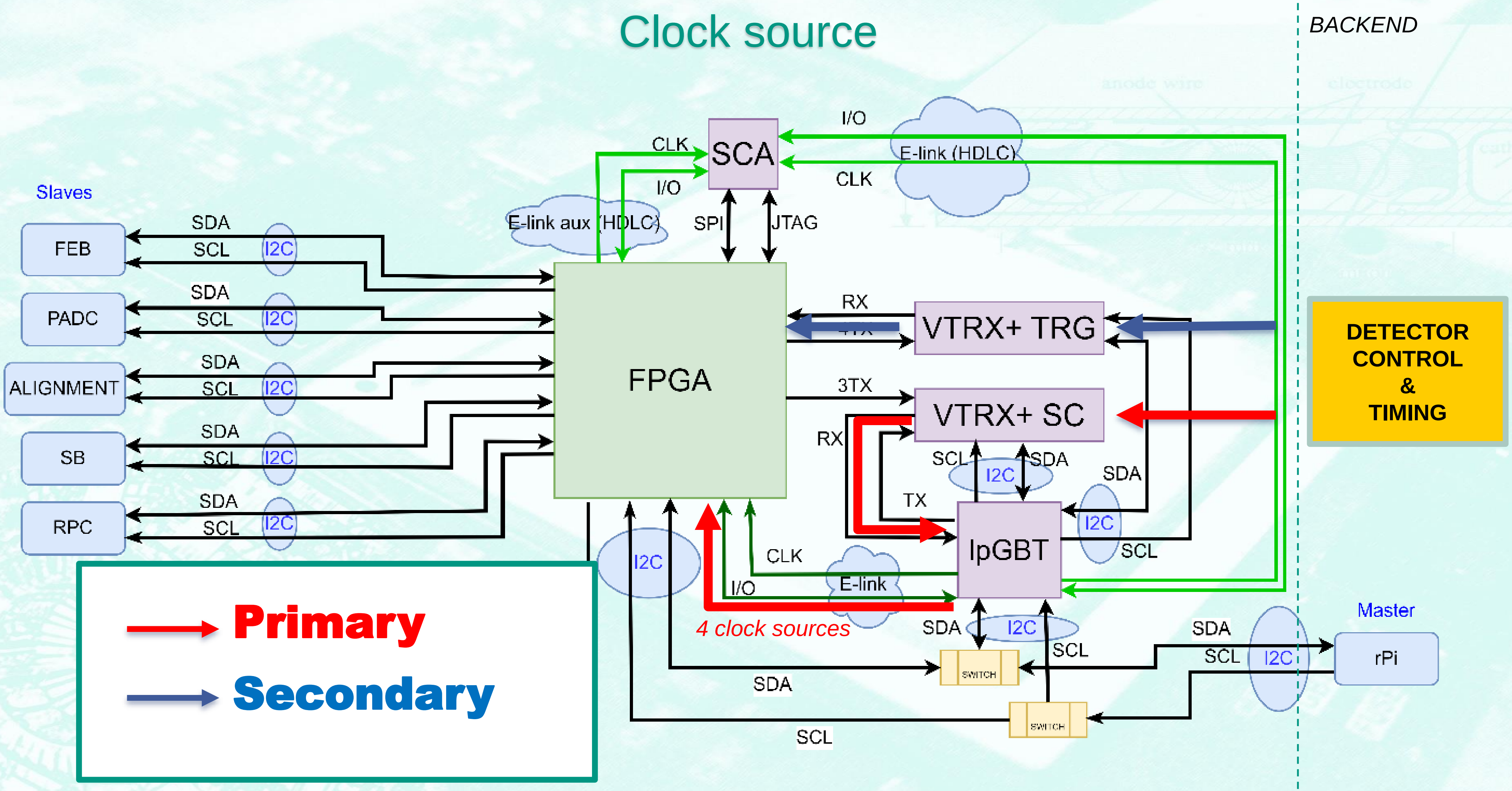
OBDT-theta board

Clock source



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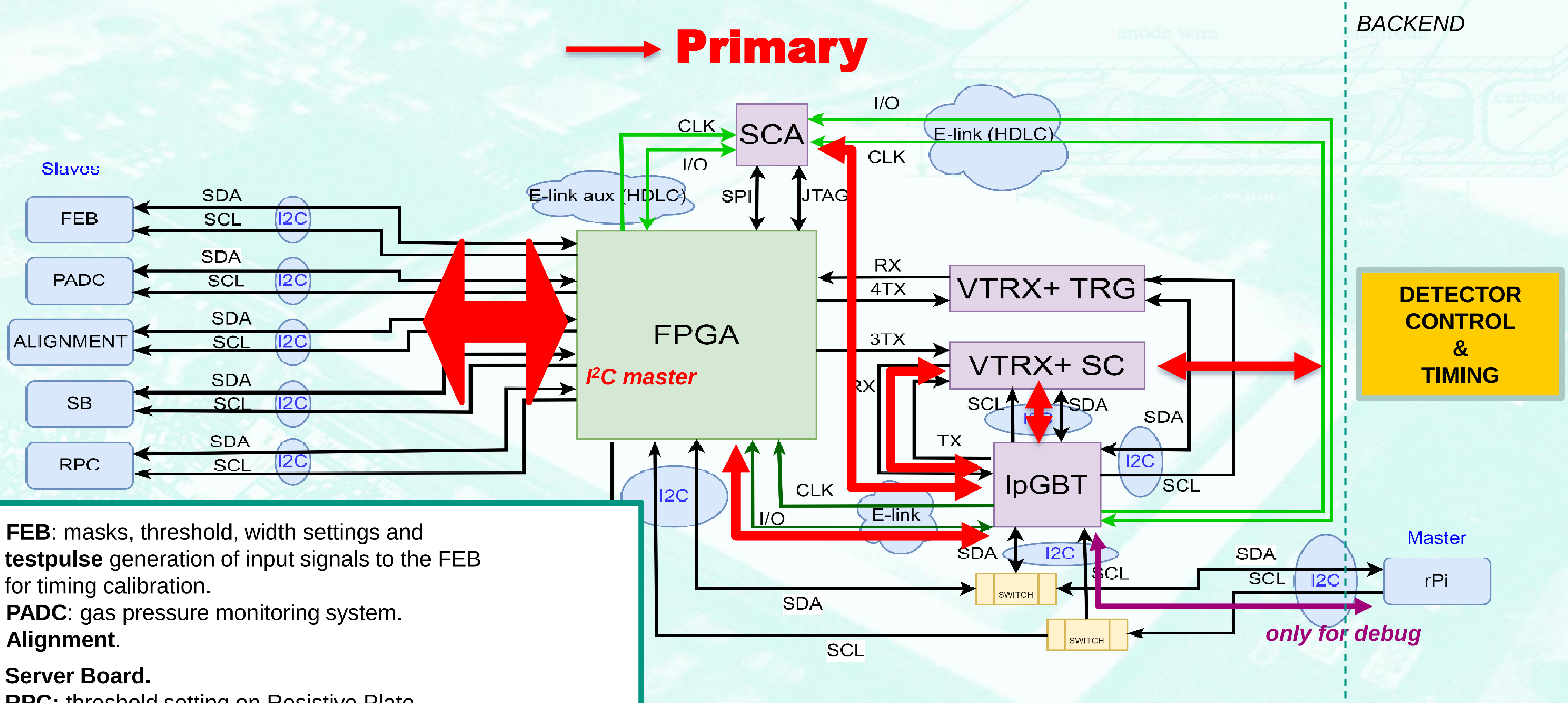
OBDT-theta board

Detector control



- **FEB**: masks, threshold, width settings and **testpulse** generation of input signals to the FEB for timing calibration.
- **PADC**: gas pressure monitoring system.
- **Alignment**.
- **Server Board.**
- **RPC:** threshold setting on Resistive Plate Chambers.

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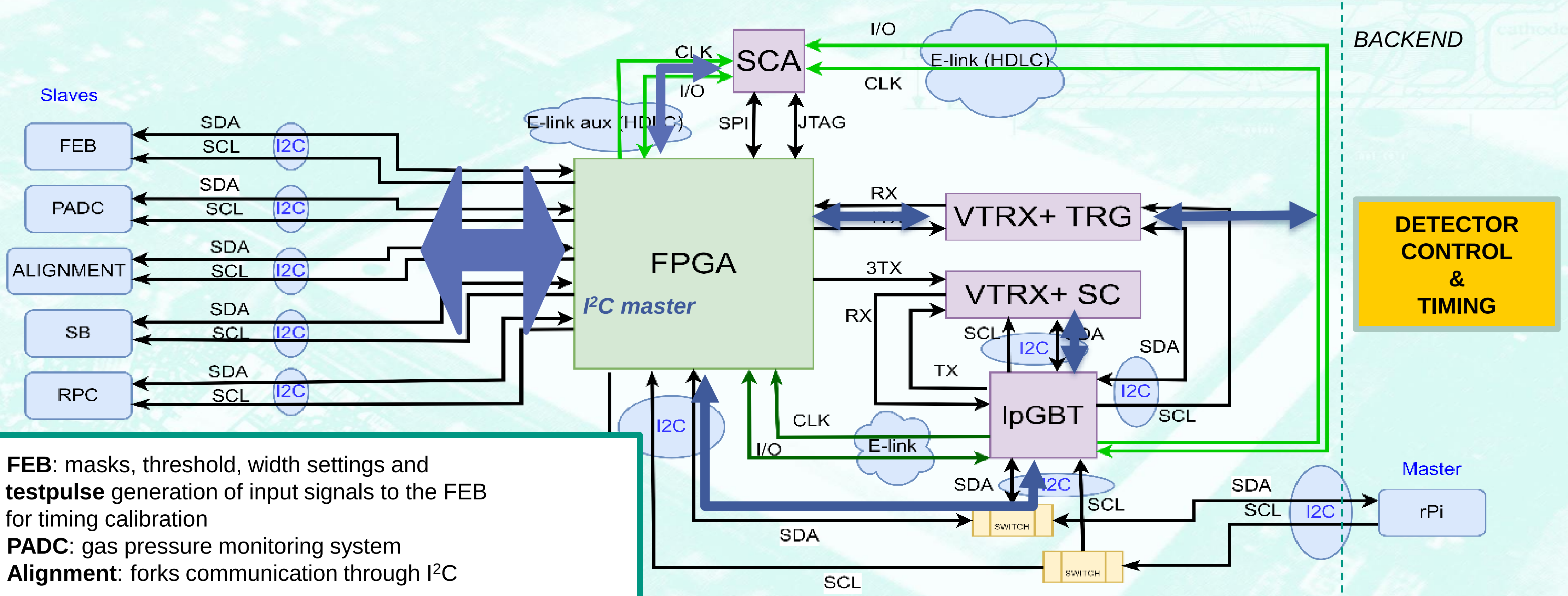
OBDT-theta board

Detector control

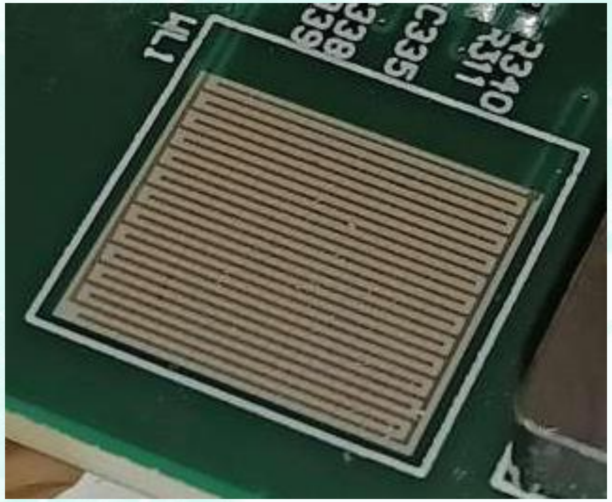
Secondary



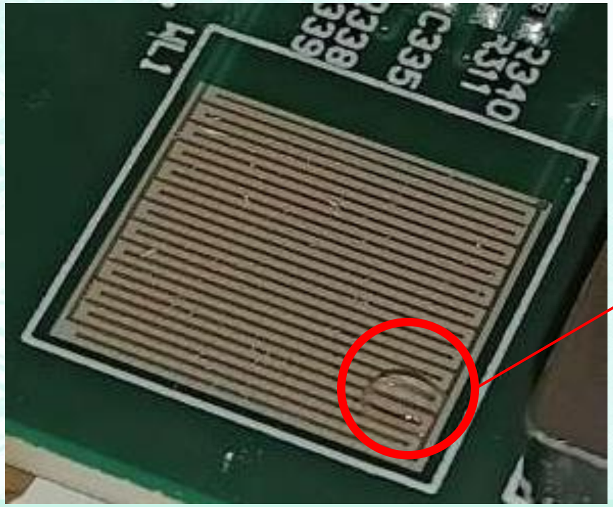
- **FEB**: masks, threshold, width settings and **testpulse** generation of input signals to the FEB for timing calibration
- **PADC**: gas pressure monitoring system
- **Alignment**: forks communication through I^{2}C
- **Server Board**
- **RPC:** threshold setting on Resistive Plate Chambers

Interfaces

Water leak sensor



Clean sensor:
0,0207 V



Water* drop:
0,635 V

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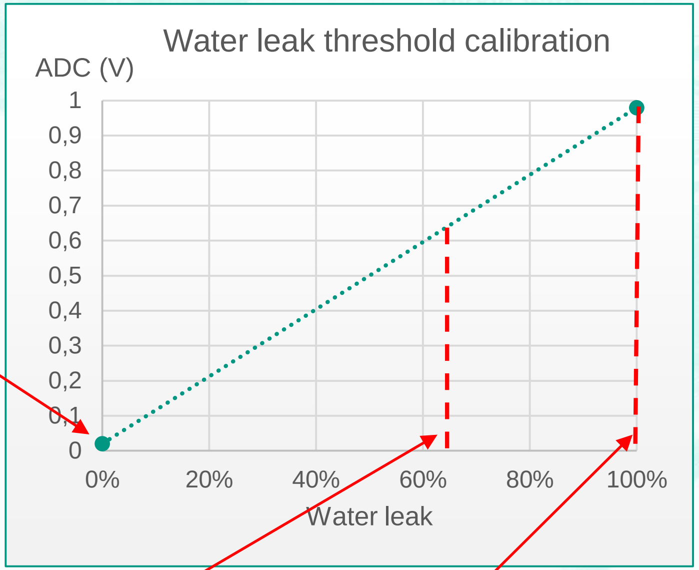
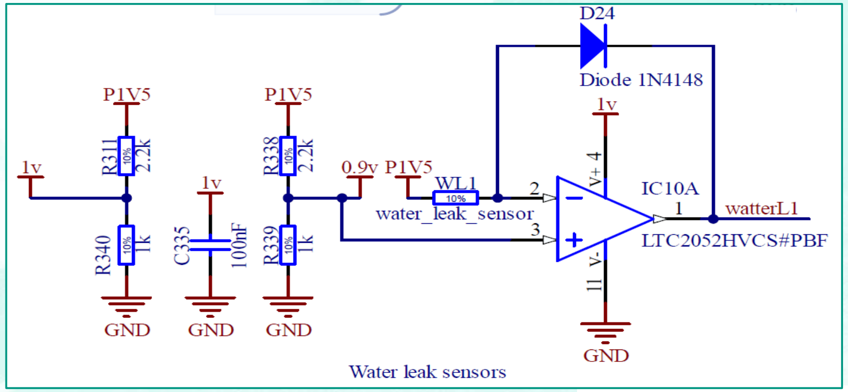


Shortcircuit:
0,985 V



* Tests performed with des-ionized water.

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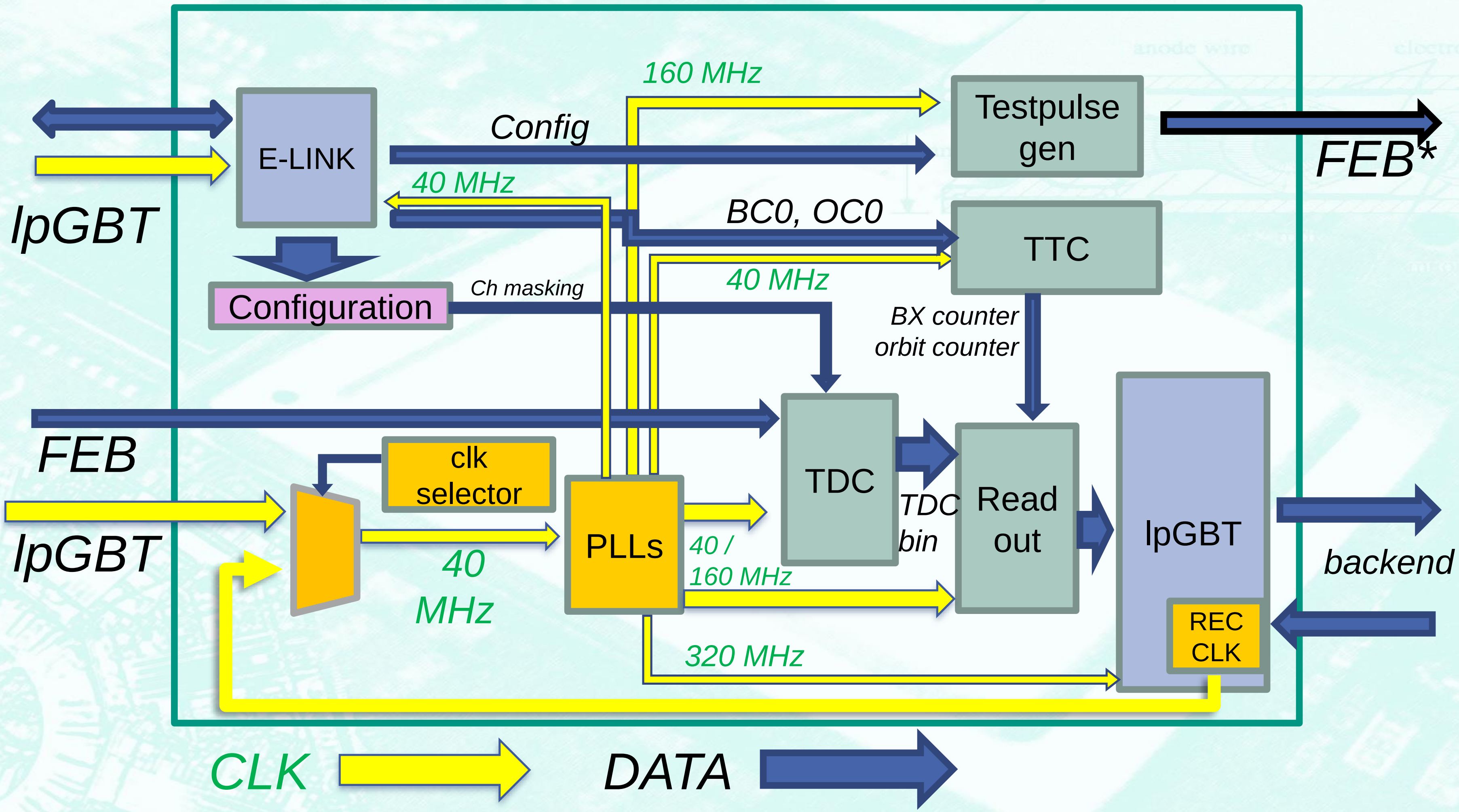
OBDT-theta firmware



Microsemi Polarfire MPF300TS

* *To OBDT electronics for testpulse generation*

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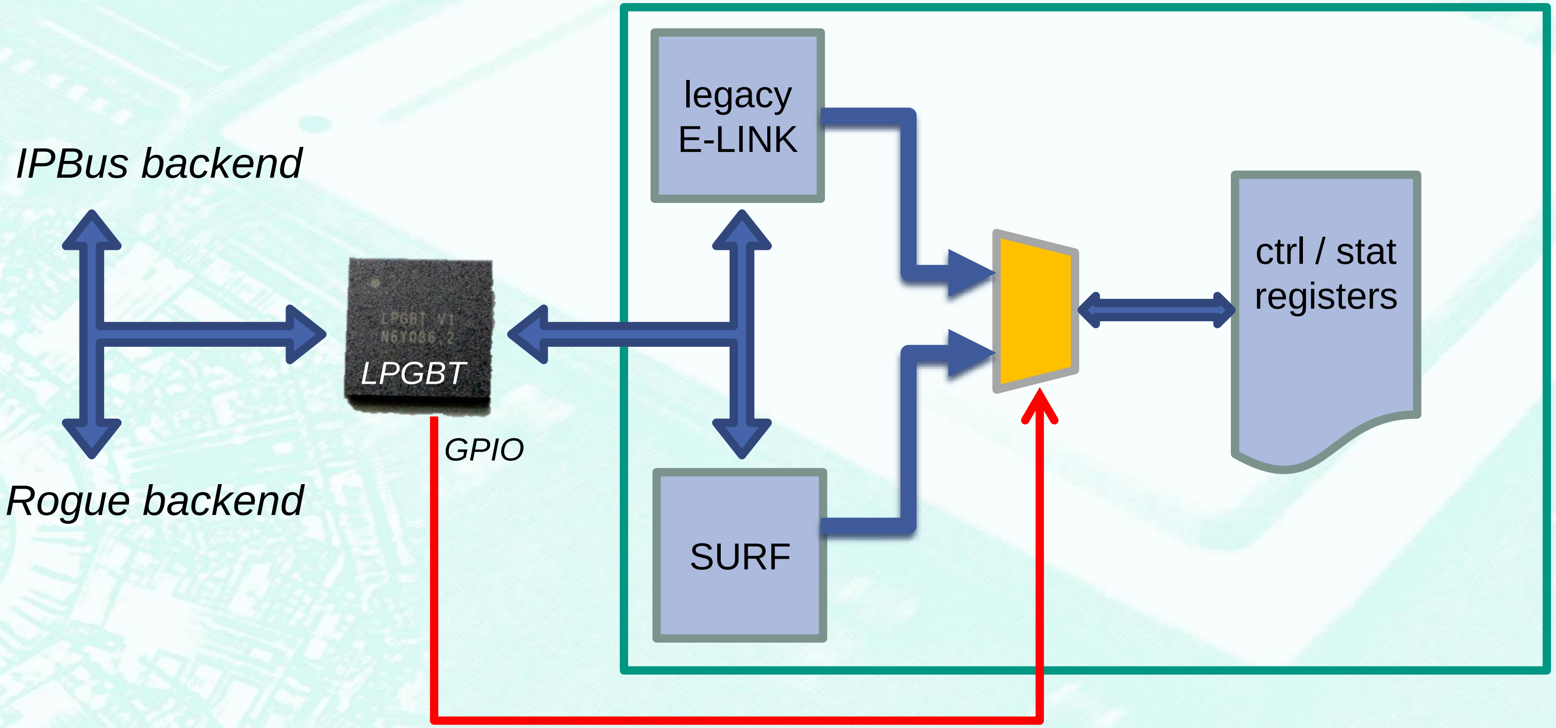
OBDT-theta firmware

Dual detector control

Two different interfaces coexist inside FPGA to communicate with legacy e-link and Rogue / SURF.

- legacy e-link: simple custom protocol based on deserialization of 8-bit words @ 320 Mbps via IPBus protocol.
- Rogue / SURF: Rogue is a higher level python framework for connecting with SURF firmware modules. SURF is an open source VHDL library maintained by TID-ID from SLAC.

This configuration provides an agnostic backend detector control.



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OBDT-theta firmware

Challenges

- Implementation of an **inverted lpGBT protocol** on PolarFire (TX: 10.24 Gbps / RX: 2.54 Gbps).
- Design of an effective **reset schema**: Who resets a specific device?. Why?. When?. How?.
- Implementation of an **automatic** source **clock switching** in FPGA.
- Implementation of **timestamp stability** in FPGA.
- FPGA **automatic configuration of lpGBT** at POR. No possibility of fusing lpGBT.
- lpGBT default configuration loaded at POR sets downlink line driver with an attenuation (gain 1/3) that causes impossibility of using optical links for some VTRx+. Need to configure lpGBT through another way (through secondary link using I^2C bus).
- **Dual detector control**. Two backend will coexist during next few months until migration to final detector control system.
- **Automatic monitoring & storing** data in PolarFire sNVM for post-failure analysis.

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Results

TDC Differential Non-Linearity (DNL)

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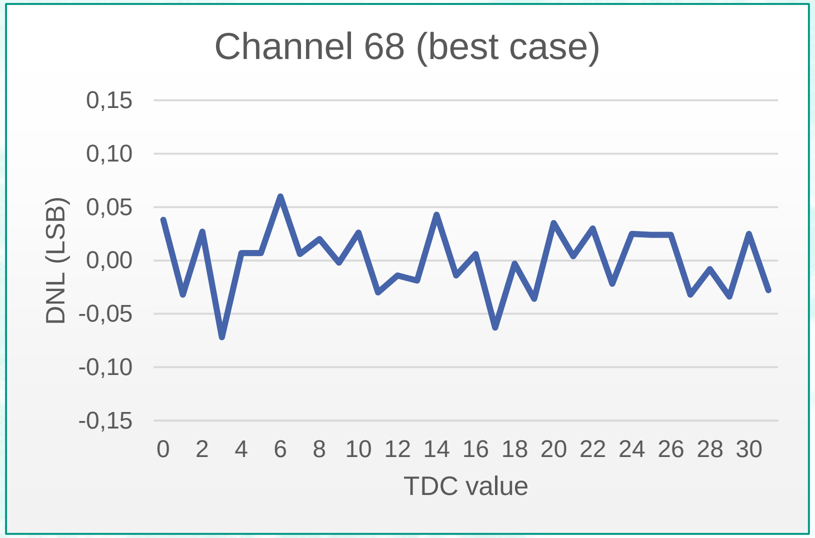

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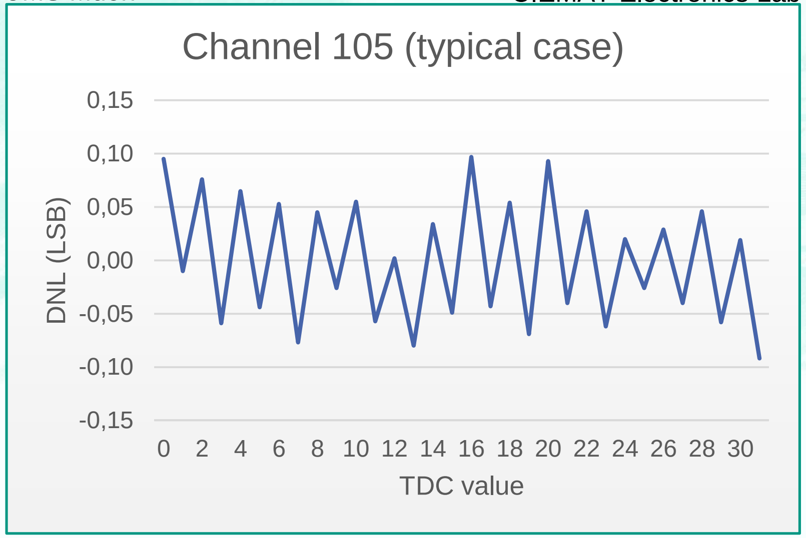

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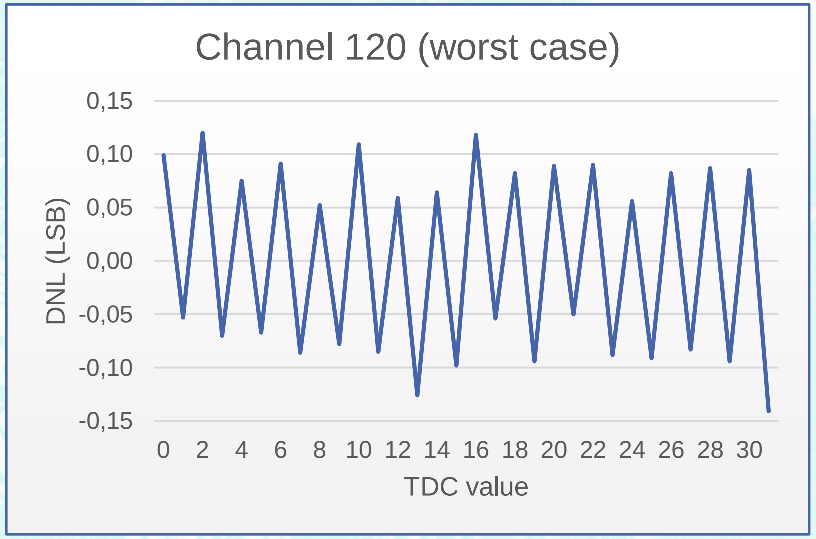

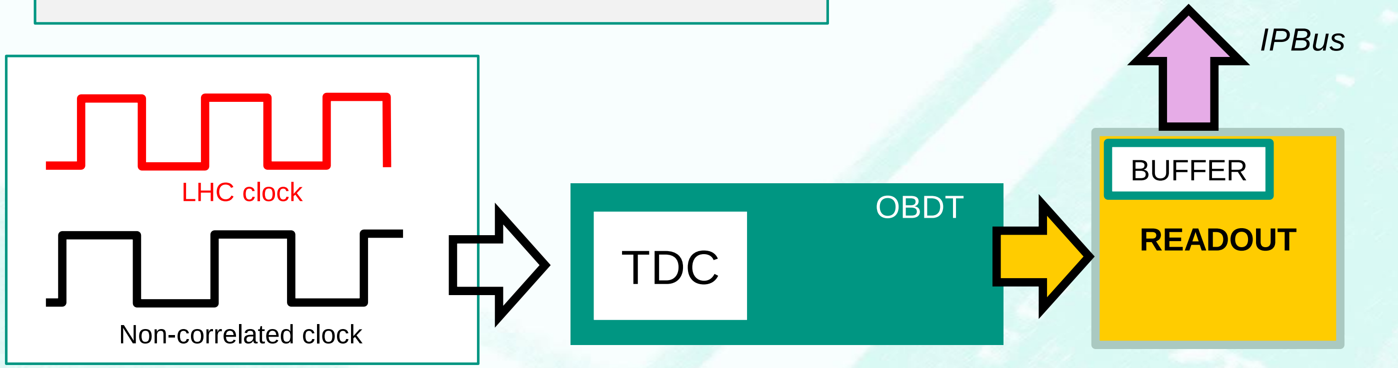

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Results

TDC Differential Non-Linearity (DNL)

- TDC DNL below 20% LSB can be acceptable.

- Most of the channels between 10-11 % LSB.

- Worst channel has a Maximum DNL of 15%, better than expected.

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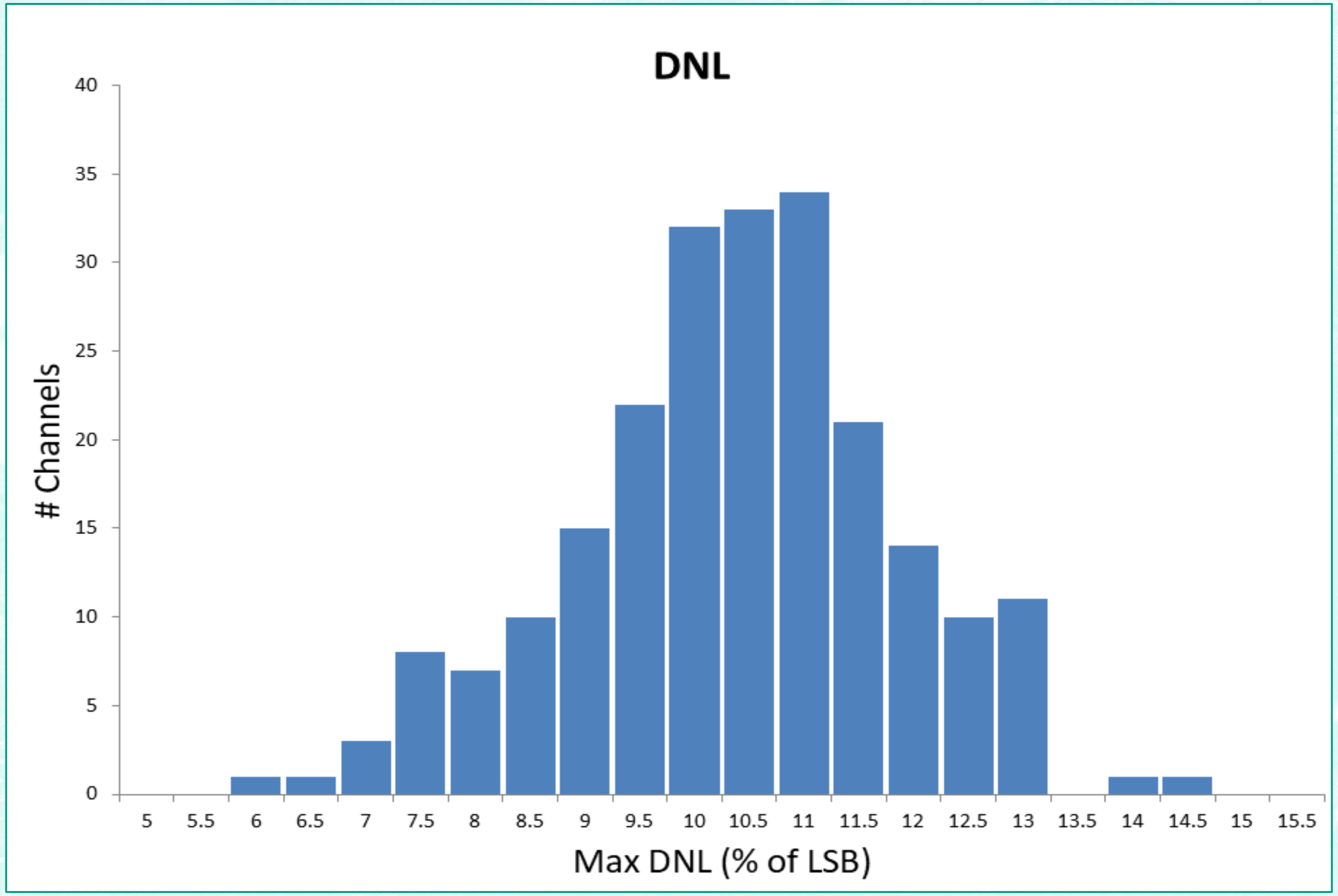

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Results

Time measurement spread

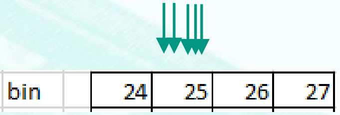
- *Every TDC bin provides a time resolution of 781 ps.*

- *Pulses emitted through all channels at a deterministic frequency (1 BX / 25 ns)*
- *OBDT-theta digitizes that pulses and sends them to the backend.*
- *Backend collects those hits for statistics.*

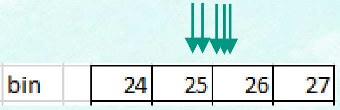
channel	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
0-37	1	1	1	1	1	1	2	1	2	1	1	1	2	2	2	2	2	2	2	2	2	1	2	2	1	1	2	1	1	2	2	2	2	2	2	2	2	2
38-75	2	2	1	2	1	1	2	2	1	2	2	2	1	2	1	2	2	1	2	1	2	2	1	2	2	2	2	1	2	2	2	2	2	2	2	2	1	2
76-113	2	2	1	2	2	1	2	2	2	1	1	1	2	1	2	2	2	2	2	X	1	1	2	2	2	2	2	2	2	1	2	2	2	1	1	1	1	1
114-151	2	2	2	2	2	2	2	2	2	1	2	2	1	2	1	1	2	1	2	2	2	2	2	2	2	1	1	2	2	2	1	1	2	2	1	1	1	1
152-189	2	1	1	1	2	X	2	1	2	2	2	2	2	1	2	2	2	2	1	1	2	2	2	1	2	2	2	2	2	1	2	2	2	2	1	2	2	2
190-227	1	2	2	2	2	2	2	2	2	1	2	1	2	2	1	2	2	1	1	1	1	2	1	2	2	1	2	1	1	1	1	1	2	2	1	1	2	2

TDC time spread map

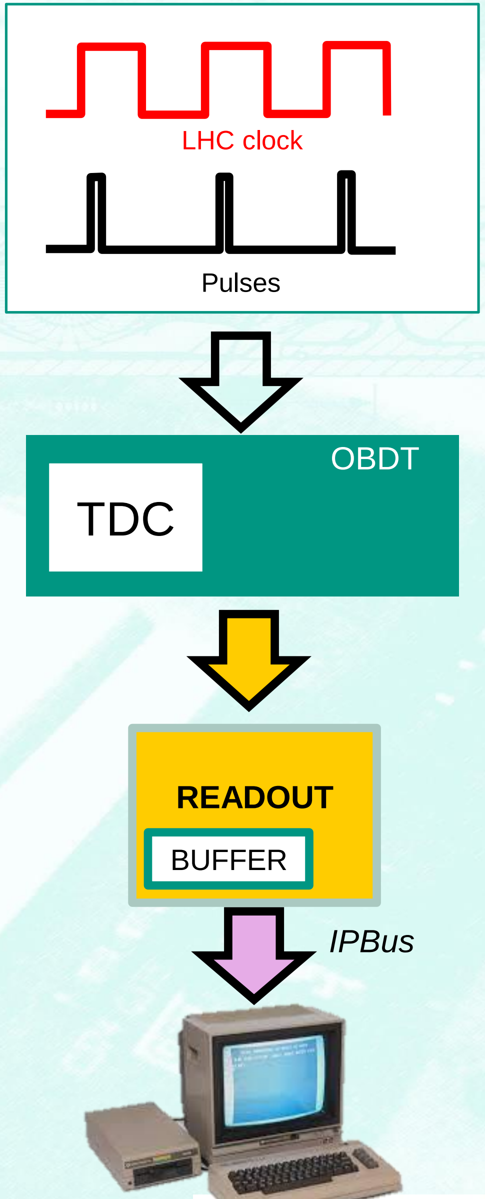
All hits inside a TDC bin



Hits between 2 consecutive TDC bins



Damaged connector



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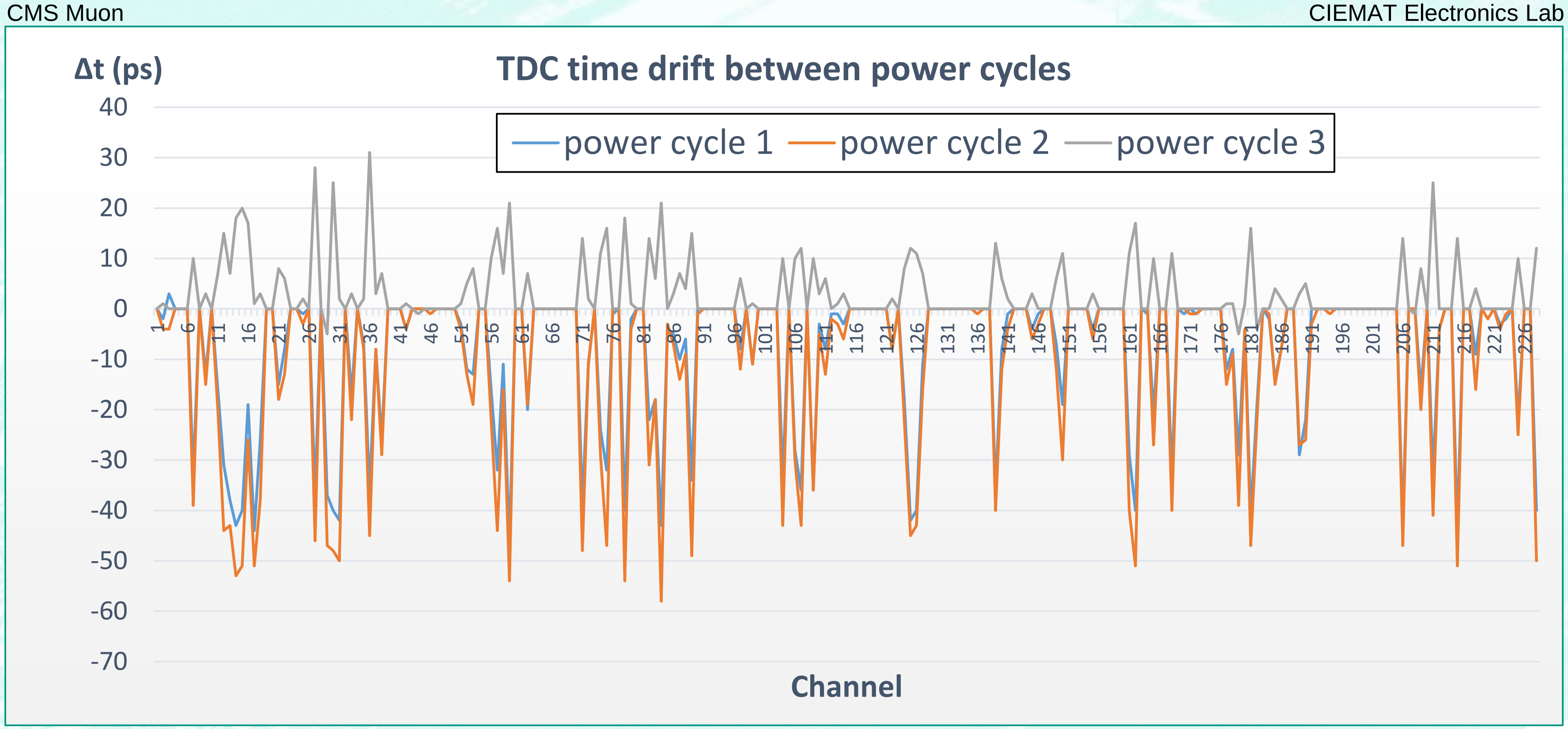
Results

Time stability

Determining the effect of power cycling the OBDT-theta in time stability:

- Previous statistics taken before and after power cycling the OBDT-theta.
- For every channel, it is calculated the difference between average time before and after power cycling.



Results

Time stability

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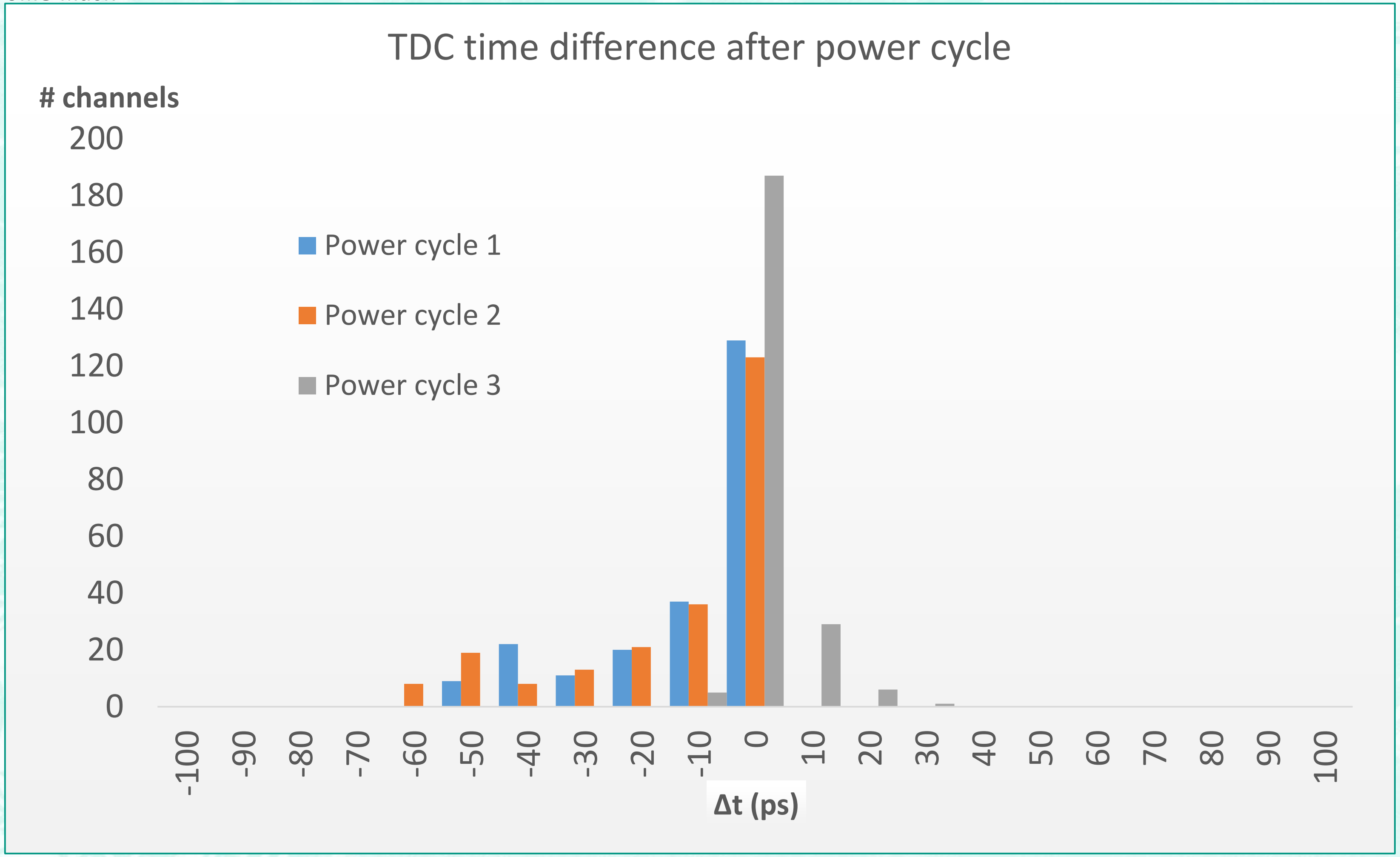

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Results

Crosstalk effect on time resolution measurements

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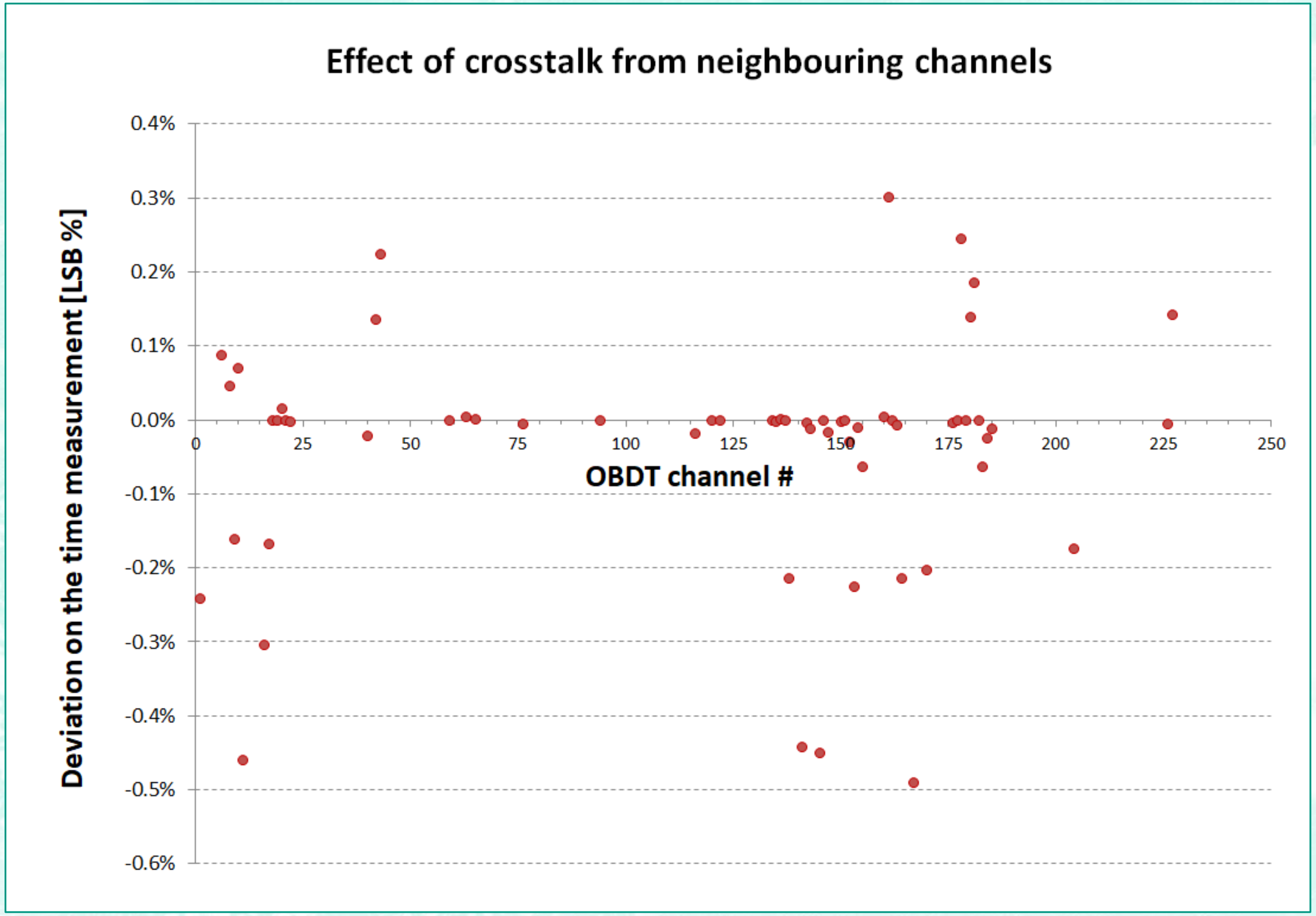

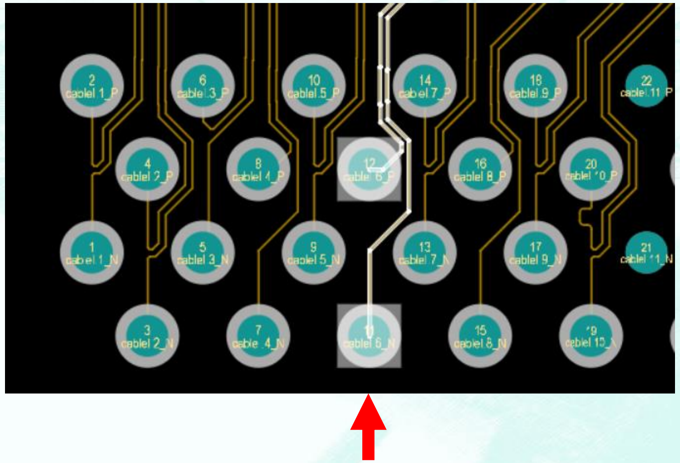

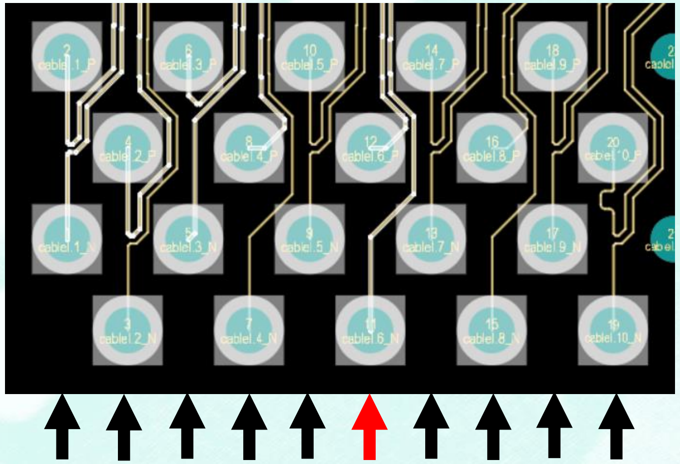

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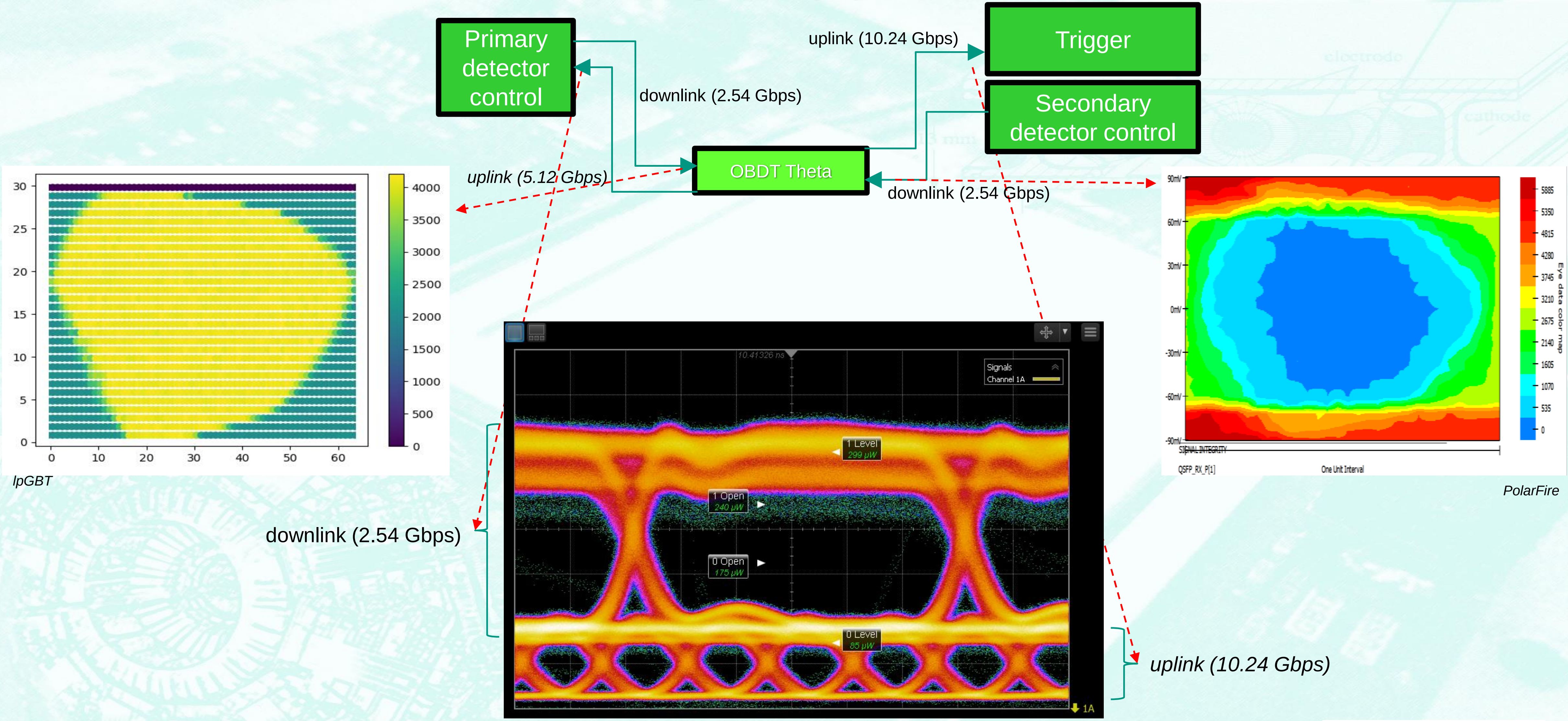
Results

Signal integrity



lpGBT

PolarFire

Keysight DCA-M N1090A

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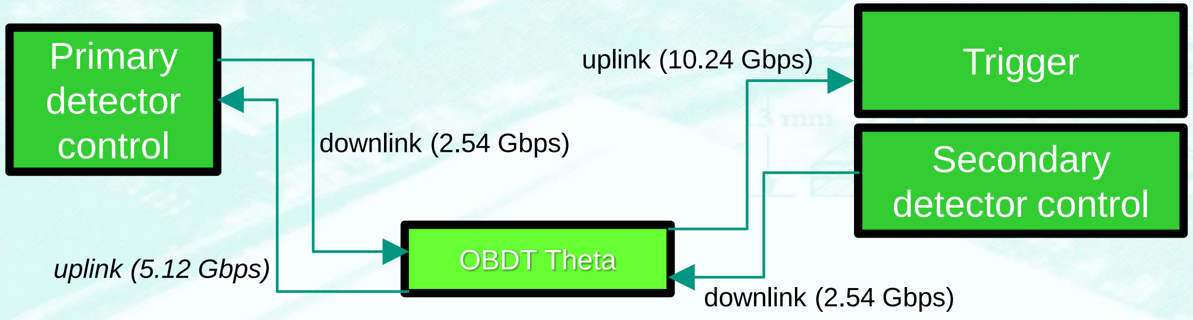
Results

Signal integrity



- *Bit Error Ratio test passed for every link.*
- *Use of a Forward Error Correction counter in different hardware:*
    - *Primary & secondary uplink: TM7 board (custom MP7 board)*
    - *Primary downlink: lpGBT*
    - *Secondary downlink: PolarFire*
- *Duration time: 10 h.*
- *Number of packets: $1{,}44\cdot10^{12}$*
- ***Excellent results for all links**: BER < $2{,}71\cdot10^{-14}$ / Inefficiency < $6{,}94\cdot10^{-13}$ (254 bits/word)*

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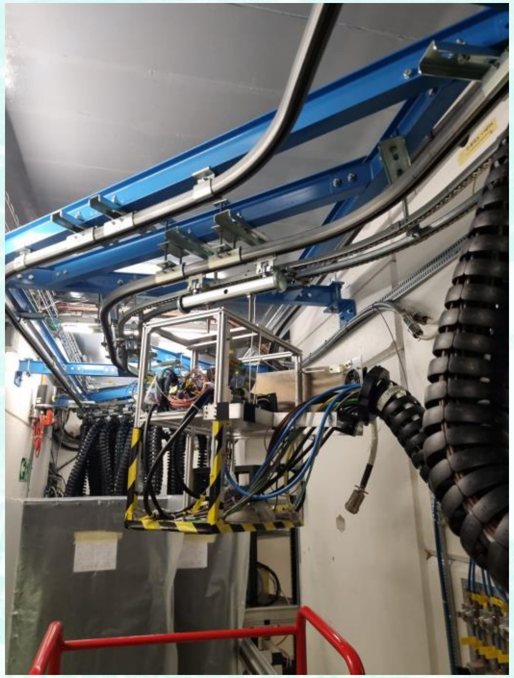
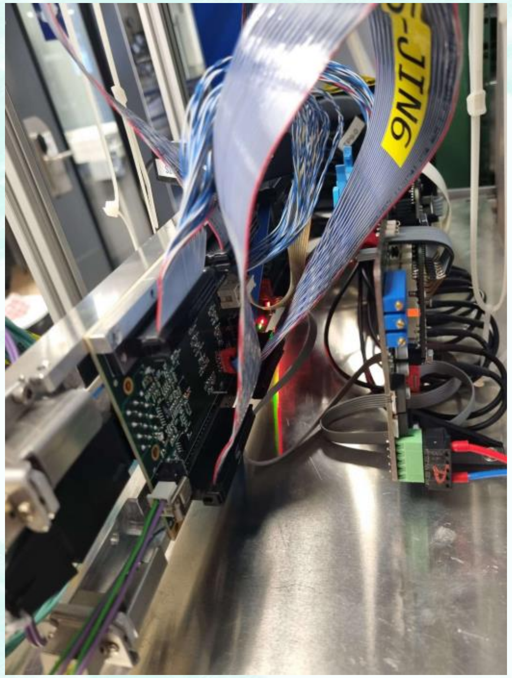
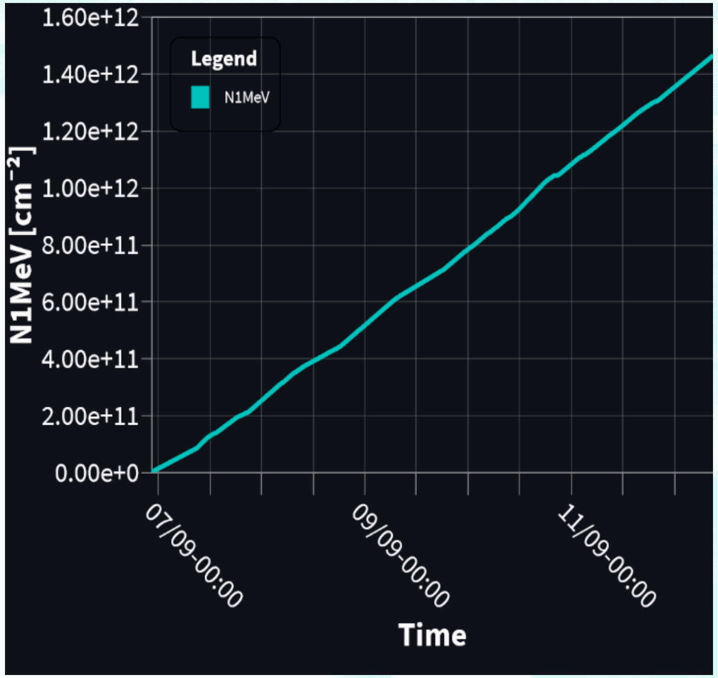
Results

Radiation hardness verification of the OBDT-theta

Previous irradiation of OBDTv1 (GBTx) prototype at CERN CHARM facility reported last year in TWEPP22, also OBDTv2 phi in medical accelerator ➔ Microchip PolarFire can be used with intended functionality for the required fluences.







- This September irradiated present OBDT-theta prototype up to 50 times HL-LHC. The board did not require periodic power cycles or configurations to operate correctly, as it was the case with commercial optics ported by OBDTv1.
- No intervention was required until reaching a dose equivalent to **20 x HL-LHC** for our application.
- Optocoupler ACPL-247 degraded during irradiation until it was not possible to operate the board > 30Gy. (required CRT was probably too high, it can be optimized)
- Data is being analyzed.

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Results

Cooling tests

- Aluminium frame with thermal pads

Thermal conductivity test with 10 different thermal pads, ranging different widths and thermal conductivities.
Temperatures in ºC after 25 minutes.

Thermal Pad, reference	Thermal conductivity [W/m·K]	Material	Width [mm]	Temp SCA	Temp VTRX+	Temp power	Temp mid-board
707-4742-2w	2	Silicone	1,5	36,32	43,54	41,42	37,23
915-6070-8w	8	Silicone	1,5	36,08	43,30	41,09	36,82
MPGCS-040-150-4w	4	Silicone	2	36,02	43,18	40,92	36,31
MP-TG-A6200-150-6w	6,2	Silicone & aluminium oxide	1	35,98	43,18	40,74	36,20
multicomp_MPGCS-060-150	6	Silicone	1,5	35,55	43,06	40,45	36,31
SARCON-150GR-HD	8	Silicone	1,5	36,35	42,70	41,53	35,61
SARCON-200GR-HD	**8**	**Silicone**	**2**	**34,49**	**41,15**	**38,02**	**36,86**
SARCON-GR80A-00-150GY	8	Silicone	1,5	36,04	43,18	41,06	32,66
SARCON-GR80A-00-150GY-3mm	8	Silicone	3	36,15	43,30	41,56	36,24
SARCON-GR80A-0H-150GY	8	Silicone	1,5	33,85	39,84	37,37	36,31

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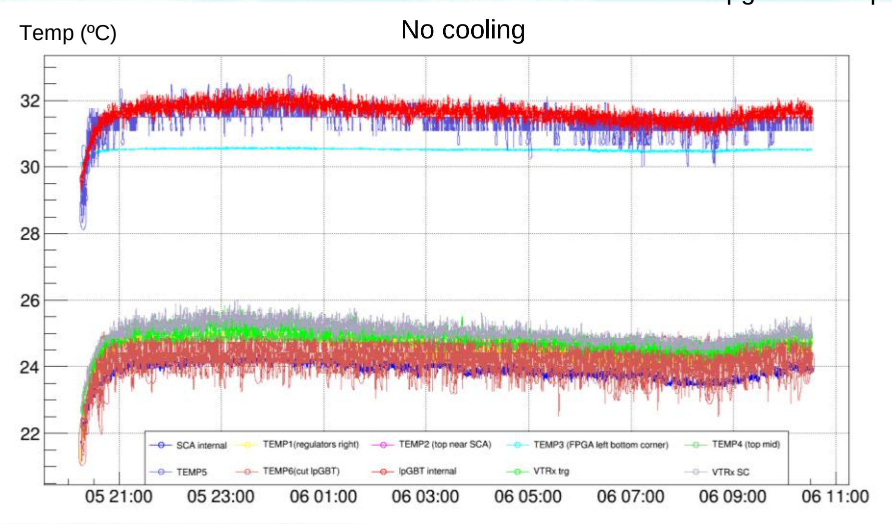
Results

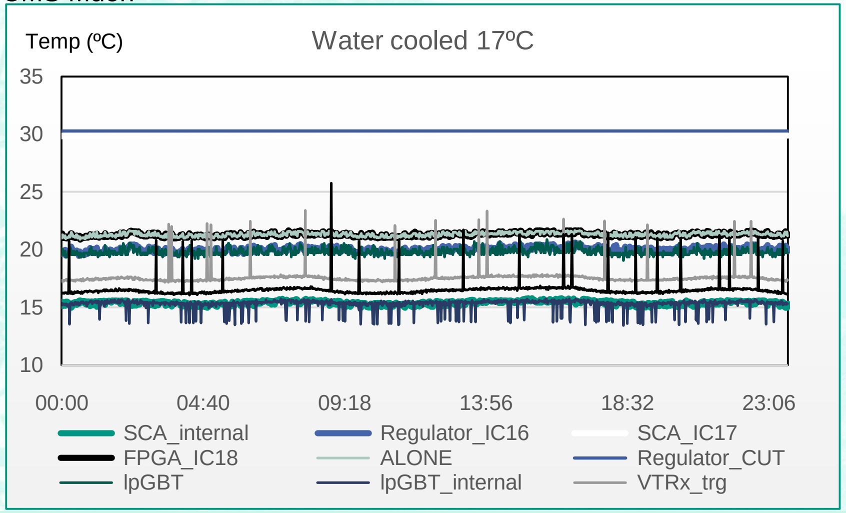
Cooling tests

CMS Muon DT SX5 Upgrade Setup

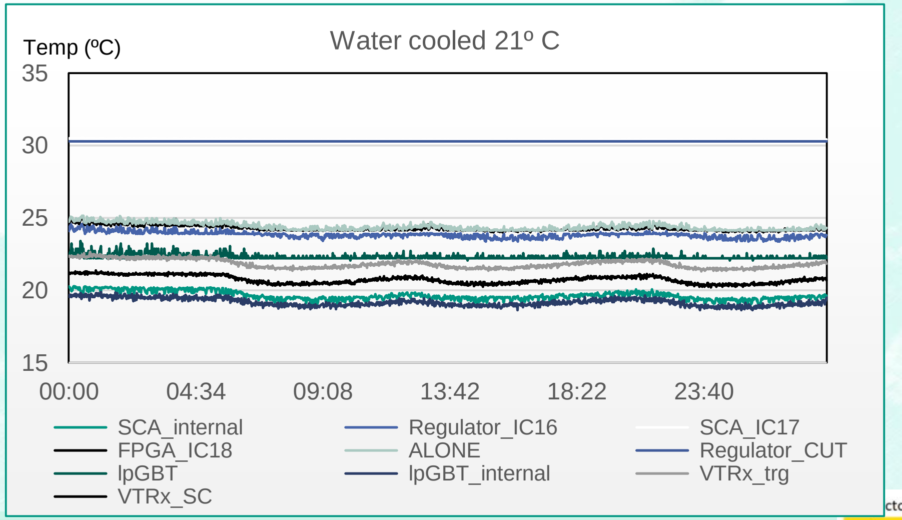


- *Maximum temperature accepted for operation: 40 ºC.*
- *All temperatures remains below 30 ºC.*
- *Hottest point: regulators.*

CMS Muon CIEMAT Electronics Lab



CMS Muon CIEMAT Electronics Lab



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Summary

- Part of a first set of OBDT-theta boards are being tested in laboratory (CMS-SX5 and CIEMAT-Madrid).
- Currently, 2 OBDT-theta boards are installed in chambers at CERN and they are being used for the Slice test at Point 5 (CMS).
- A full chain up to the BMTL1 is operational.
- Operation includes parasitic cosmics and collisions data taking as well as calibration test pulse runs.
- Final pre-production launched now.
- Preparation of a semi-automatic testbench setup for functionality testing is ongoing.
- Summarizing, OBDT-theta prototypes show very good performance, with satisfactory validation tests.

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Thanks

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Back-up

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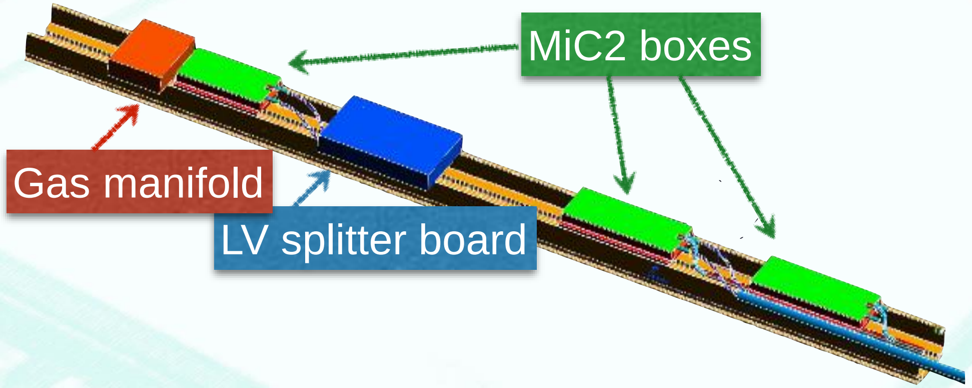
DT Phase 2 upgrade: Installation

Chamber type	Number of SuperLayers	Channels per SL_ϕ	OBDT per SL_ϕ	Channels per SL_θ	OBDT per SL_θ	Total OBDT per chamber	Total OBDT per Wheel	Total chambers	Total OBDT
MB1	$2\ \phi$ and $1\ \theta$	196	1	224	1	3	36	60	180
MB2	$2\ \phi$ and $1\ \theta$	228	1	224	1	3	36	60	180
MB3	$2\ \phi$ and $1\ \theta$	288	2	224	1	5	60	60	300
MB4	$2\ \phi$	384	2			4	40	50	200
$MB4_{small}$	$2\ \phi$	288	2			4	16	20	80
								Total Boards	940

From Phase 2 Muon TDR



- The current MiC extrusions are preserved in situ and 3 or 4 MiC2 boxes (one/two per SuperLayer), are attached to each extrusion.(MB3 and large MB4 chambers get 2 MiC2s per Superlayer due to their larger dimensions).
- In total we have 420 SLs out of 660 SLs for which a 228 channel OBDT will be optimal
- The limited space in the MB1 and MB2 chambers limits the number of boards to OBDT/SuperLayer.

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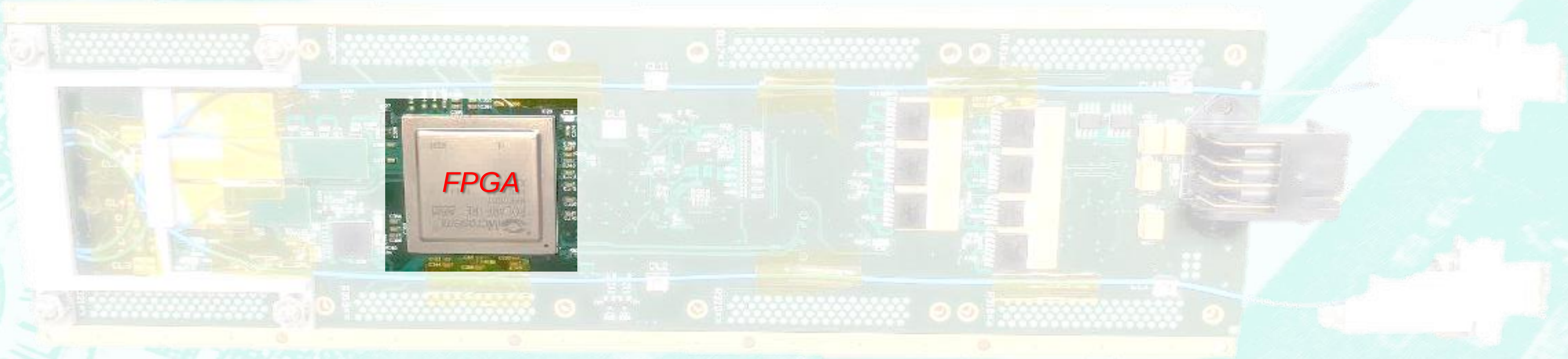
OBDT-theta board

Main components

FPGA:

- Microchip PolarFire MPF300T
- 300.000 logic elements.
- 16 High-speed transceiver lanes (up to 12.7 Gbps)
- Radiation tolerant



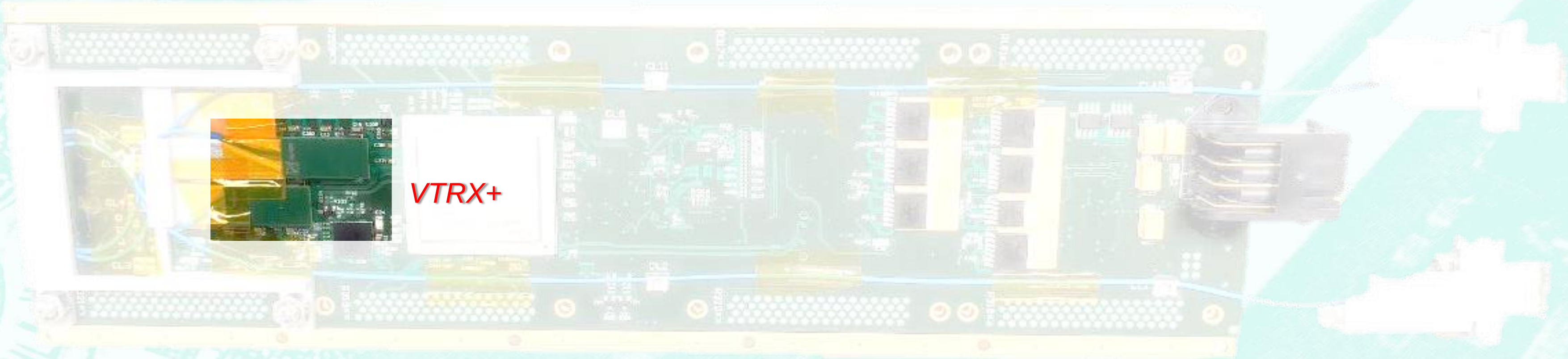
BOTTOM VIEW

OBDT-theta board

Main components

<u>Versatile Link$^+$ Transceiver (VTRx$^+$):</u>

- Radiation tolerant modules.
- They provide a multi-gigabit per second optical physical data.
- 4 TX lanes (up to 10.24 Gbps) / 1 RX lane (2.54 Gbps).
- Two of them mounted:
    1. Main detector control / secondary readout.
    2. Main readout / secondary control.



BOTTOM VIEW

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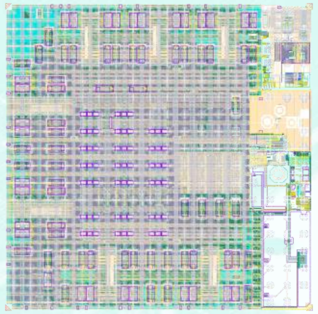
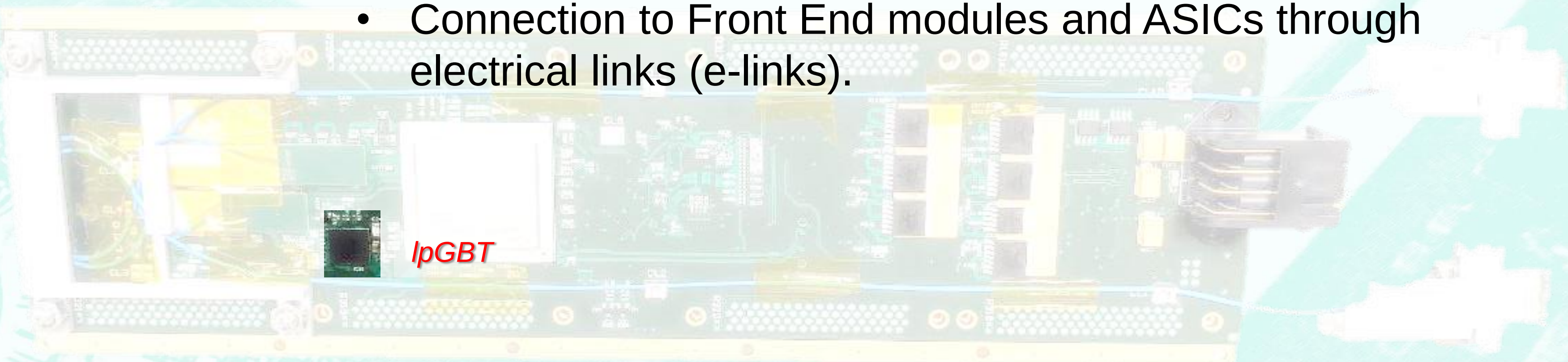
OBDT-theta board

Main components



<u>Low Power Giga Bit Transceiver (lpGBT):</u>

- Radiation tolerant ASIC.
- Multipurpose high speed bidirectional optical links.
- Assymetric data rate:
  - downlink 2.54 Gbps
  - uplink 10.24 Gbps
- Custom protocol with FEC correction.
- Precise timing control (4 clock sources routed to FPGA).
- detector control interfaces (GPIO, I^2C, ADC, DAC).
- Connection to Front End modules and ASICs through electrical links (e-links).



BOTTOM VIEW

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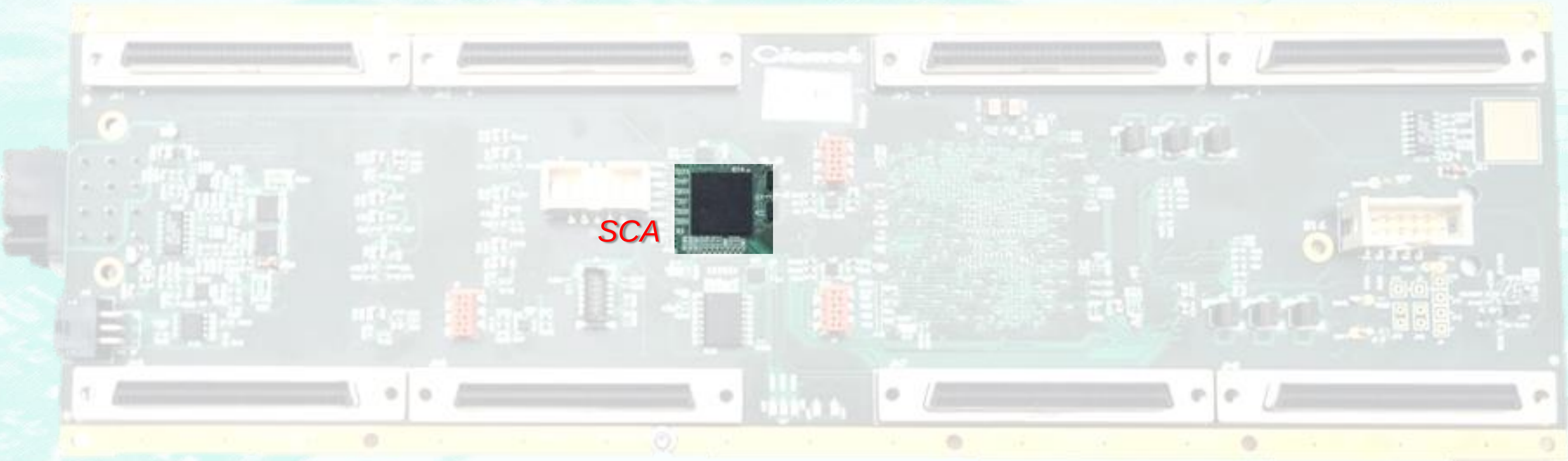
OBDT-theta board

Main components



<u>detector control Adapter (SCA)</u>

It distributes control and monitoring signals.

Interfaces:

- GPIO
- ADC
- DAC
- JTAG
- SPI

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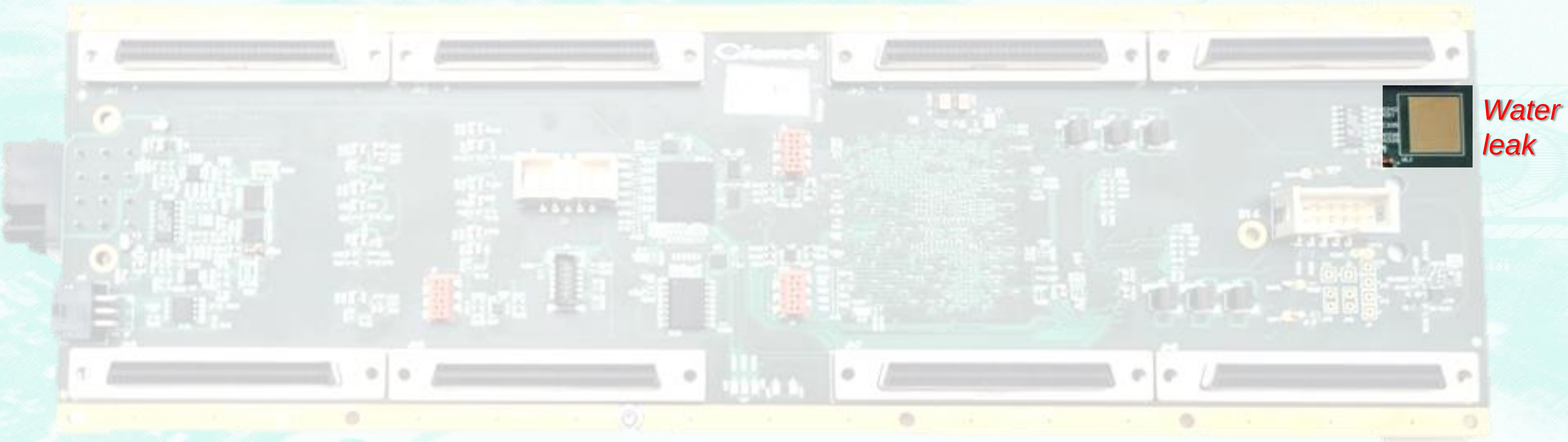
OBDT-theta board

Main components



<u>Water leak sensor</u>

It distributes control and monitoring signals.

Interfaces:

- GPIO
- ADC
- DAC
- JTAG
- SPI

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OBDT-theta board

detector control

- **lpGBT**: 1 master I²C → VTRx+ SC
- **SCA**:
  - 29 ADC's for monitoring:
    - Voltages and currents
    - Temperature
    - Humidity
    - Water leak
    - FEB monitoring signals
    - VTRx+ signal strength
  - 1 DAC to send level signal to FEB.
- **FPGA**:
  - 7 master I²C:
    - FEB, PADC, alignment, SB, RPC
    - lpGBT auxiliary link
    - VTRx+ Trg
  - SCA auxiliary link SCA

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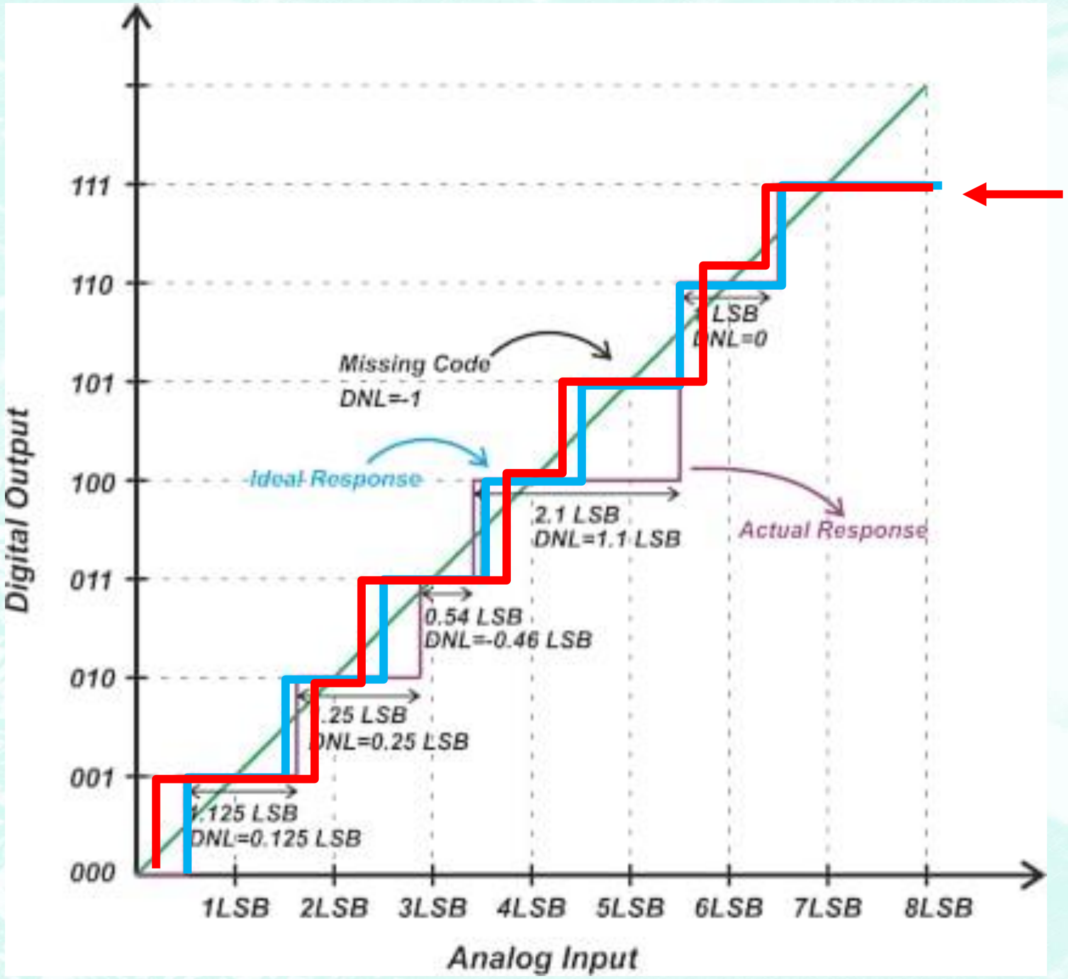
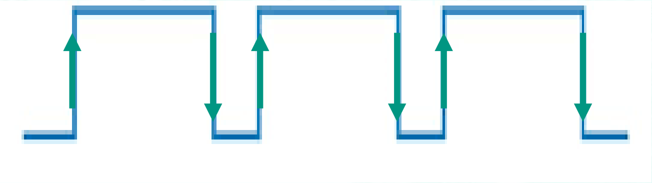
Results

TDC Differential Non-Linearity (DNL)

allaboutcircuits.com

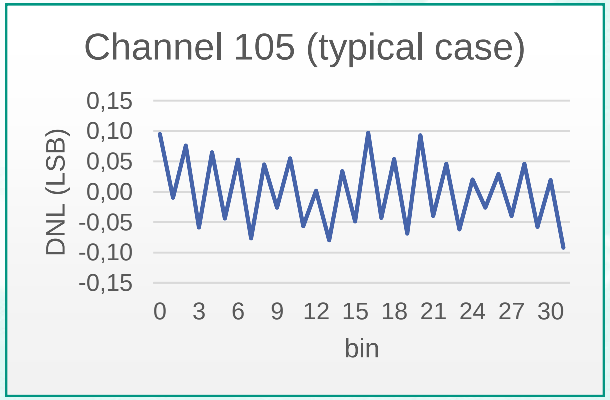


Non 50% duty-cycle clock source



CMS Muon

CIEMAT Electronics Lab



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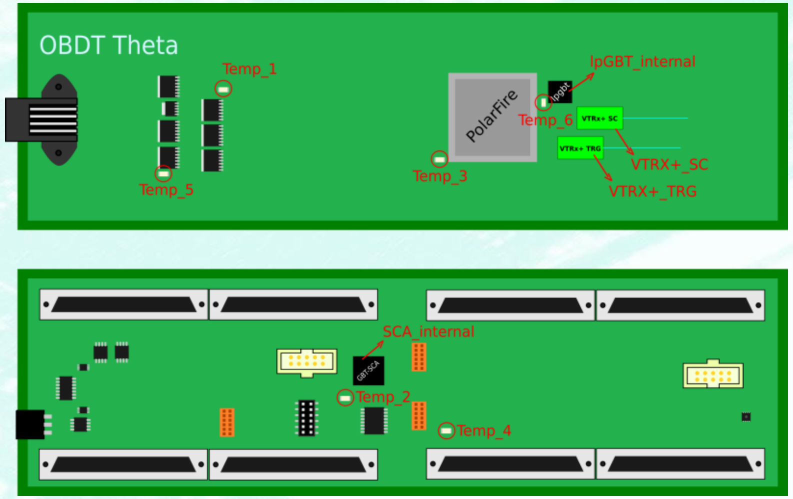
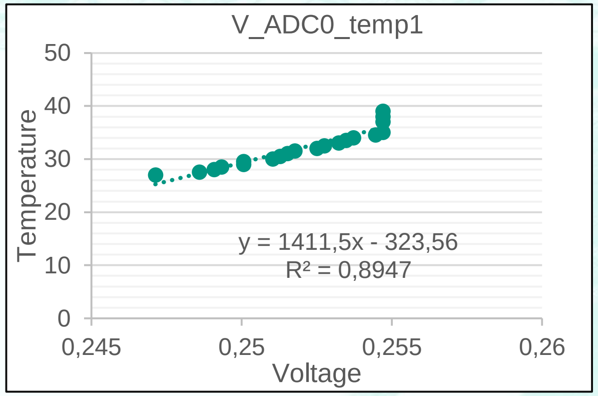
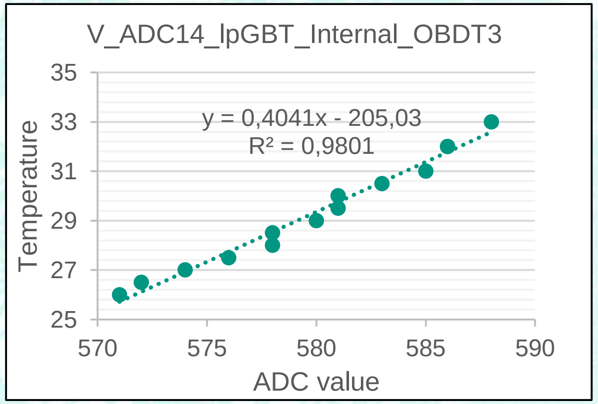
Interfaces

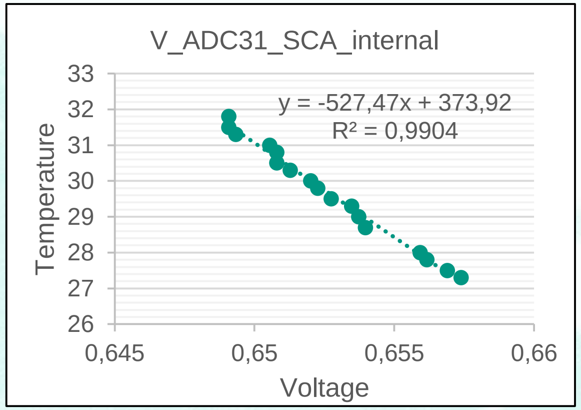
Temperature sensors calibration

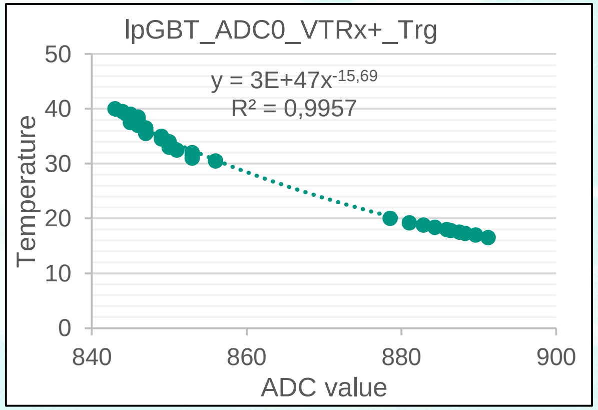


1. Pt1000 resistors.
2. NTC resistors.









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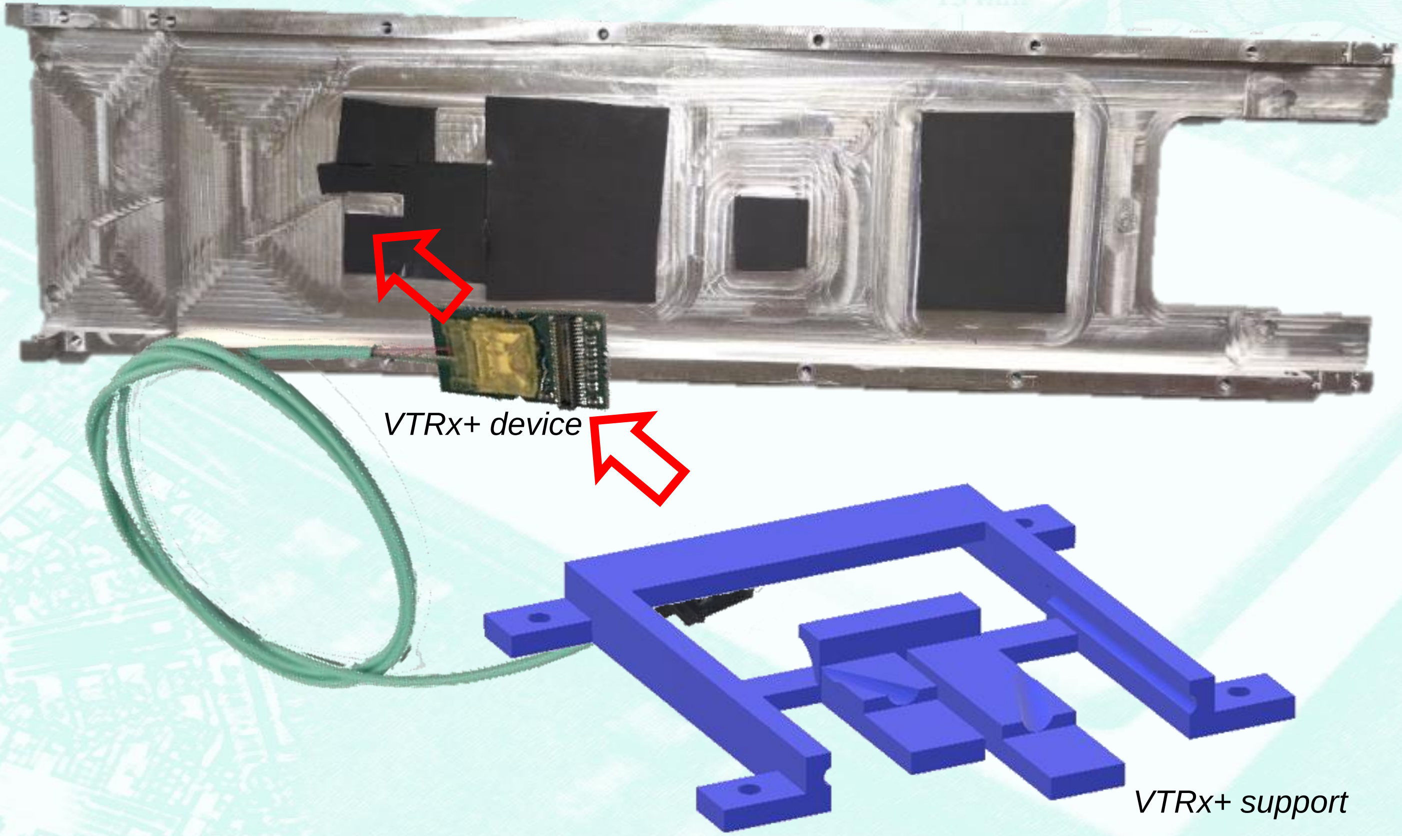
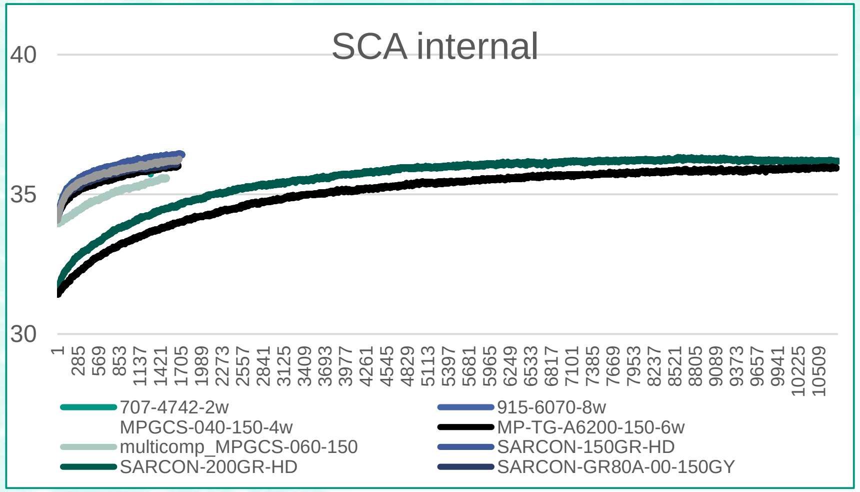
Results
Cooling tests

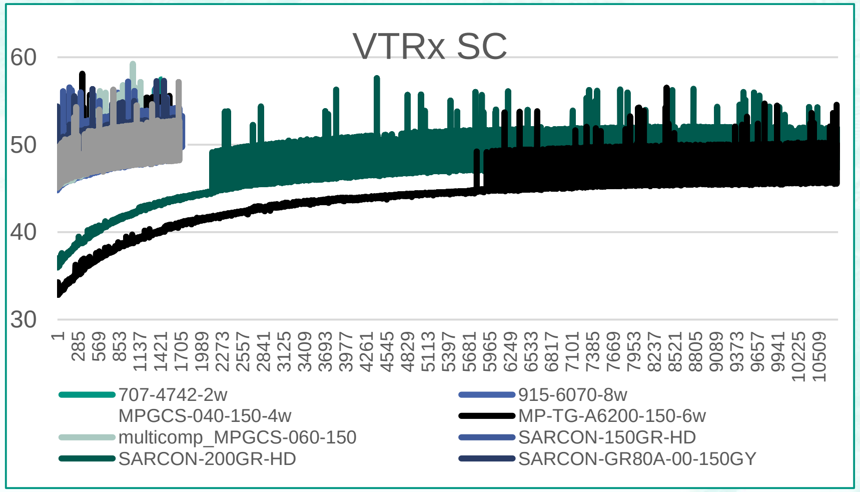
Aluminium frame with thermal pads

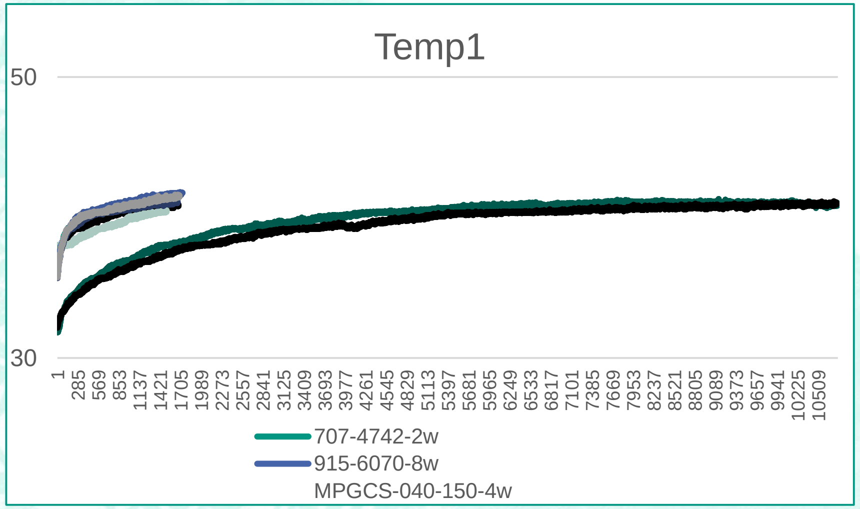


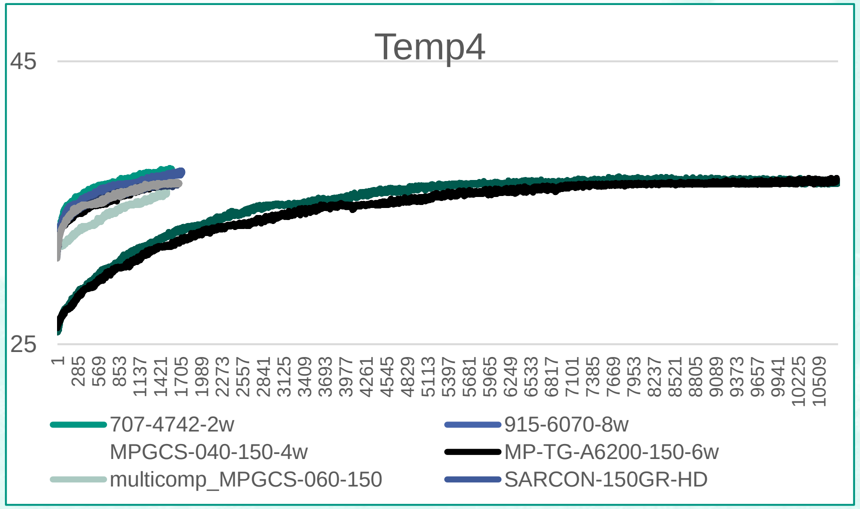
Results

Cooling tests









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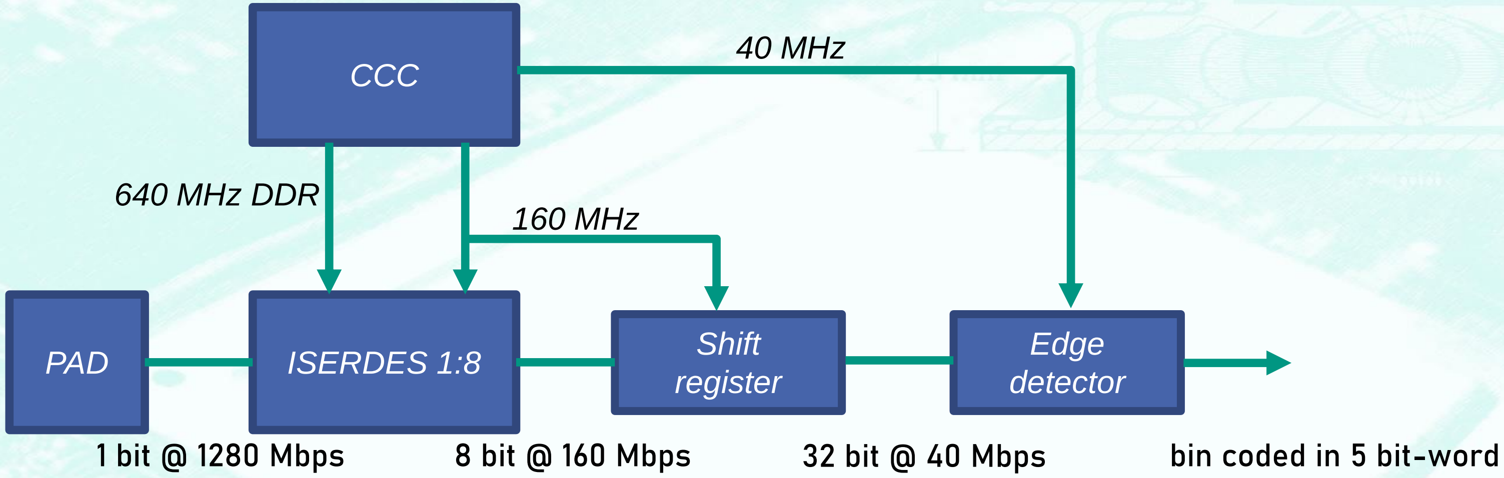
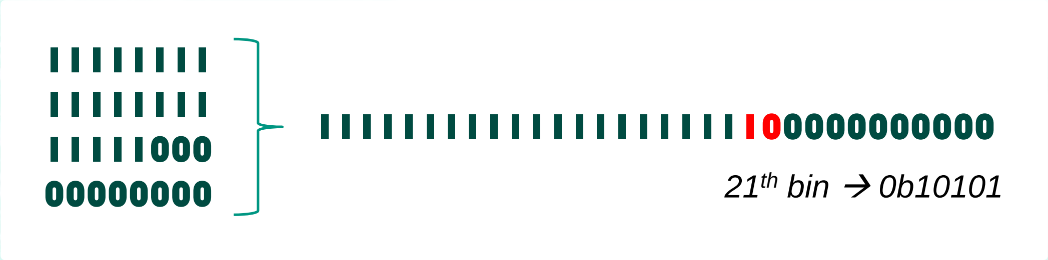
OBDT firmware

TDC block



Max. time resolution: 32 bin → LSB = 25/32 ns = 0,78 ns



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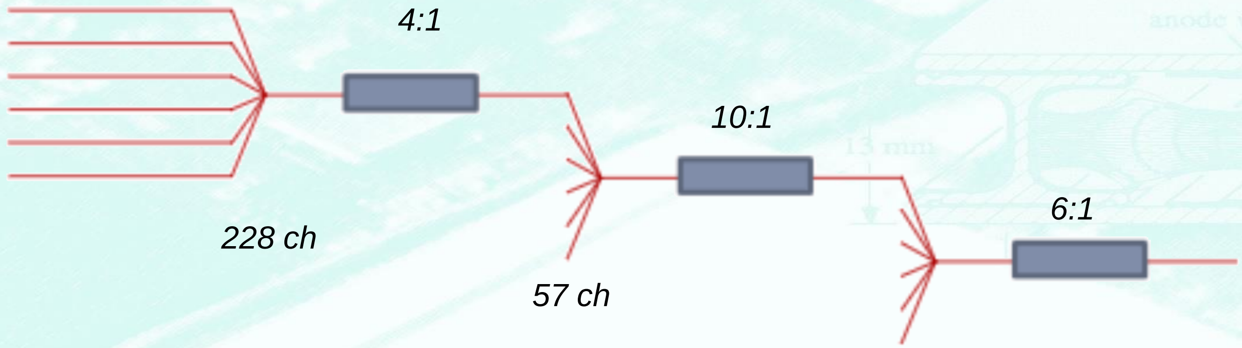
OBDT firmware

Readout block

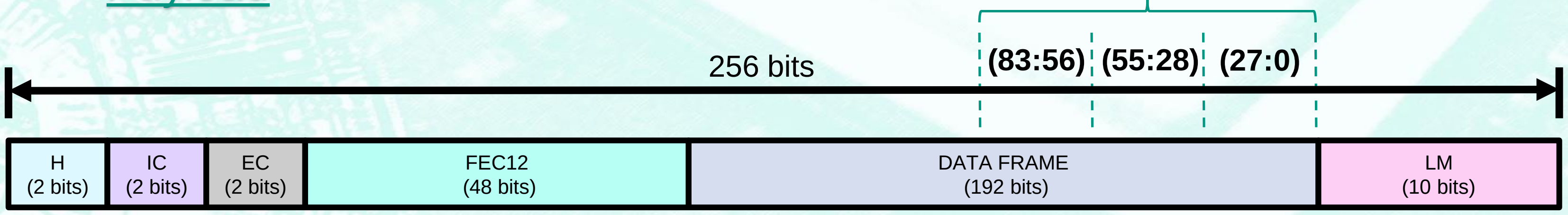


The TDC hits are merged through three-stages fan-in (4-to-1, 10-1 and 6-1) to the input port of the lpGBT block.

3 readout hits (3 x 28 bits) / frame

TDC count (24:20)
Bunch counter (19:8)
Channel (7:0)

Payload



lpGBT frame 10G FEC12
256 bits @ 10,24 Gbps

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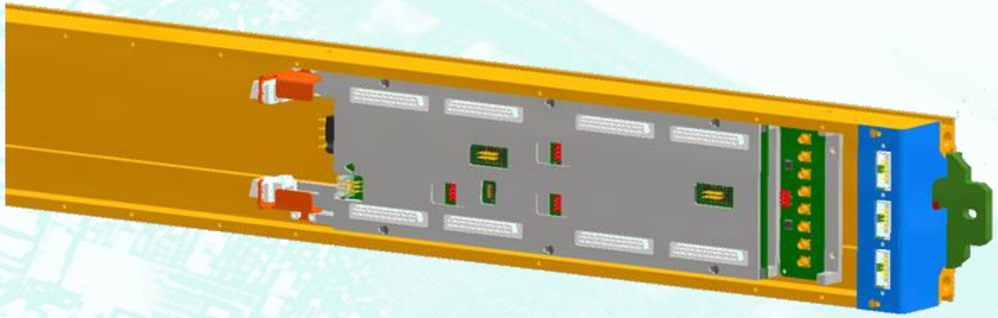
Results

Cooling tests

- Frame
- Thermal pad
- Minicrate
- Minichiller



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DT Phase 2 backend

- Selection of final ATCA board is on process. Most of the present L1 Trigger boards could work for us, decision is not urgent.
- Demonstrators are based on Phase 1 electronics, aka TM7 board.
- This board is the present TwinMux and uROS board installed in the CMS detector in USC, with different firmware. Twinmux performs DT+RPC merging, uROS is the new DT Readout System.

For phase 2 we needed demonstrator boards for detector control and TP generation:

TCDS distribution and detector control => **MOCO board**

Present functionality:

- Configuration and monitoring of the OBDT.
- Handles clock and TCDS
- IPBUS communication
- One bidirectional GBT link to OBDT

Next steps:

- Integrate 12 GBT links (RX/TX) in the same MOCO board

Virtex 7
XLXXC7VX330T-3FFG1761E

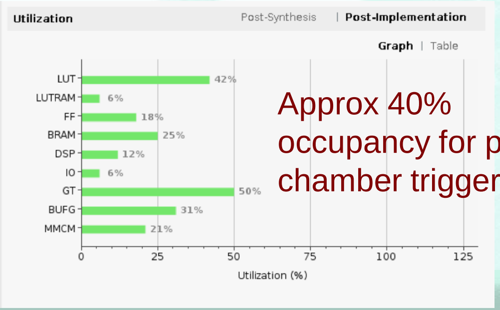
Trigger primitive generation => **AB7 board**

Present functionality:

- Generates TP primitives
- Performs event matching and readout

Next steps:

- Integrate 4 GBT links (RX/TX) in the same AB7 board



Approx 40% occupancy for phi chamber trigger

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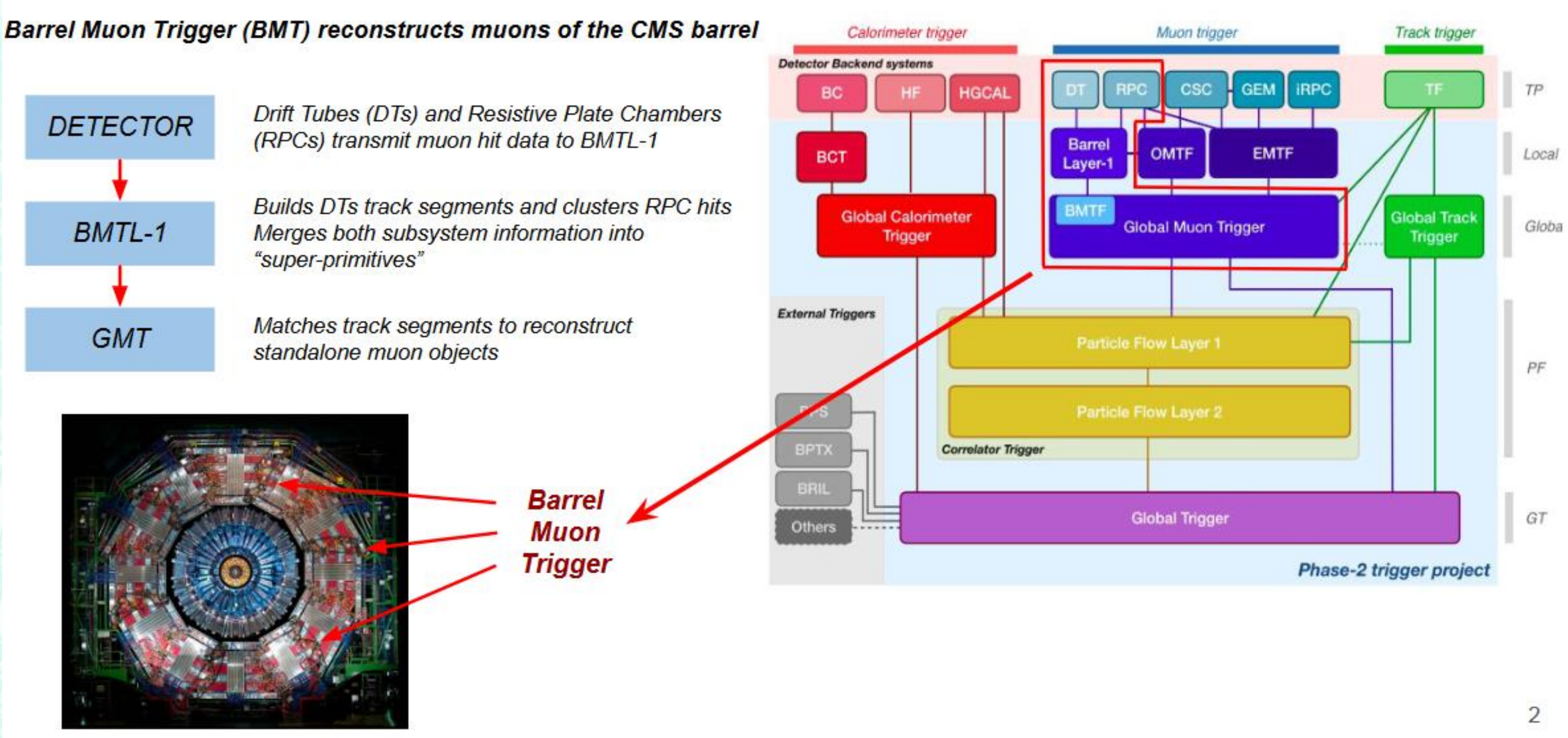
DT Phase 2 backend



"An ATCA Processor for Level-1 Trigger Primitive Generation and Readout of the CMS Barrel Muon Detectors".
Ioannis Bestintzanos, BMTL-1 team
TWEPP 2022 Topical Workshop on Electronics for Particle Physics

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