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The OBDT-theta board: time digitization for the theta view of Drift Tubes chambers.

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We present the design and performance of the new On-Board electronic for the Drift Tubes (OBDT) for the superlayer theta along the direction parallel to the beam-line, built to substitute part of CMS DT Muon on-detector electronics. The OBDT-theta is responsible of the time digitization of DT chamber signals for the theta view, allowing further barrel muons tracking and triggering. It's also in charge of part of the slow-control of the DT chamber systems. A prototype is being tested in the laboratory and in a demonstrator inside CMS, as well as the full functionality in real conditions, showing satisfactorily results.

Summary (500 words)

The on-detector electronics of the CMS Muon DT chambers will need to be replaced for the HL-LHC operation due to the increase of occupancy and trigger rates in the detector, which cannot be sustained by present system. The OBDT-theta boards, together with OBDT-phi boards, will be located inside minicrate mechanics attached to the DT chamber, inside the CMS volume. It will be in charge of performing the 1 ns time digitization of the DT chamber signals of the theta view and the multiplexing for further transmission to the readout and trigger backend electronics. This board is also in charge of some of the slow-control tasks needed by part of the DT chamber system. There will be 180 boards representing roughly 1/5 of all the OBDT boards in the system. The OBDT-theta board has been built around a Microsemi Polarfire FPGA, responsible of the time digitization of up to 228 input signals. It implements a deserialization method which runs at 600 MHz and allows obtaining a time bin of 0.833 ns. The input data is forwarded to the output optical link for data transmission to the readout and trigger chains. Communication for this prototype is based on two VTRx+ transceivers that provide two bi-directional links for slow-control and six transmitter links, capable to output data up to 10.24 Gbps to the backend system. One of the bi-directional links goes to the lpGBT chip in the OBDT board, that provides the main slow-control functions and reception of LHC clock and some TTC signals. The other one is directly connected to the FPGA serving as a secondary slow-control to recover OBDT in case of loss of main slow-control. The protocol implemented so far follows lpGBT protocol for all links. The lpGBT chip plus a SCA chip in the board allow clock and synchronization reception as well as e-link implementation for configuration and monitoring of the Microsemi FPGA. Through this link it is also possible to implement the different slow-control functionality of the barrel system, such as setting the front-end discriminators thresholds and bias values, implementation of the I2C links for temperature monitoring and channel masking, communication to the PADC, RPC and Alignment slow-control chains and finally, control of the test pulse generation mechanisms that allows to perform the DT chamber time measurements calibration for the theta view superlayers. A prototype of this board has been produced and is being tested both in the laboratory and also in different test stands with DT chambers and other phase-2 electronics prototypes. The different functionality of the OBDT-theta board has been verified and the overall architecture has been validated both through specific tests and through cosmics ray and LHC collisions data taking integrated with the rest of the DT system. The OBDT-theta architecture together with its performance results will be presented in this contribution, showing the goodness of the design for the expected functionality during HL-LHC.

Author: SASTRE ALVARO, Javier (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES))

Co-authors: NAVARRO TOBAR, Alvaro (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); DE LARA, Clara (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); FERNANDEZ BEDOYA, Cristina (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); REDONDO FERRERO, David Daniel (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); FRANCIA FERRERO, David (Cent.de Investigac.Energeticas Medioambientales y Tecnol. (CIEMAT)); REDONDO FERNANDEZ, Ignacio (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); LEON HOLGADO, Jaime (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES)); CUADRADO CALZADA, Sergio (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES))

Presenter: SASTRE ALVARO, Javier (CIEMAT - Centro de Investigaciones Energéticas Medioambientales y Tec. (ES))

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