Test Bench of a 100G Radiation Hardened Link for Future Particle Accelerators

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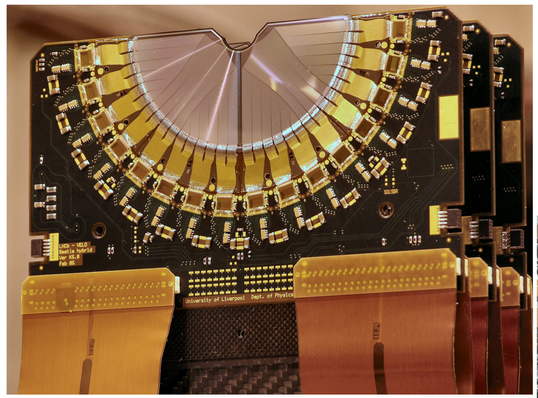
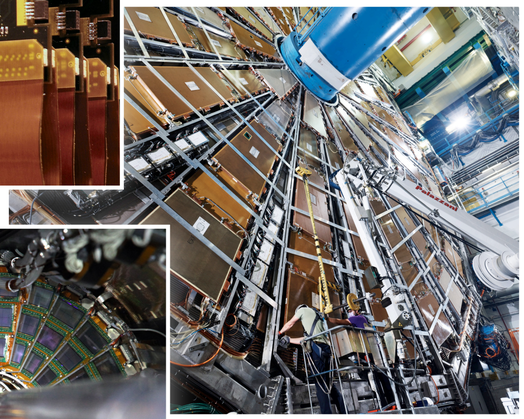
Outline

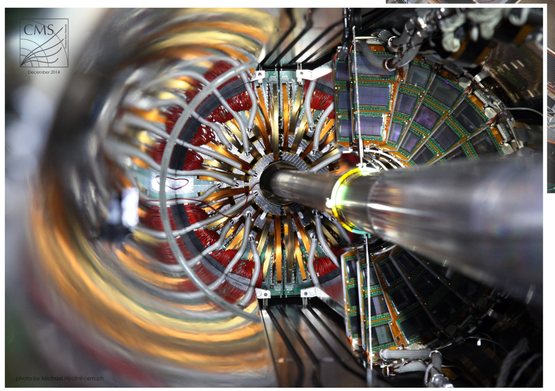
- Introduction to the project
- Novel concepts for high speed data communication
- Emulation of the DART28 device on programmable logics
- Firmware for the back-end electronics
- Testing methodology and characterisation board
- Board architecture and involved challenges
- Conclusions

Data Links for Future Accelerators and Detectors



Front-End
Detectors

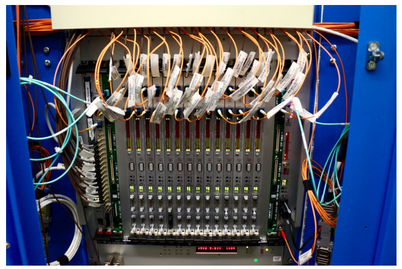




Data Uplink

Orders of
1 PB/s

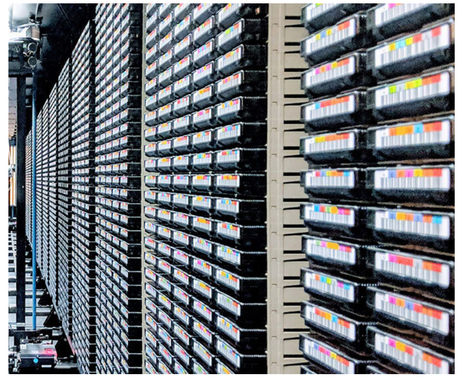
Back-End
Data Readout

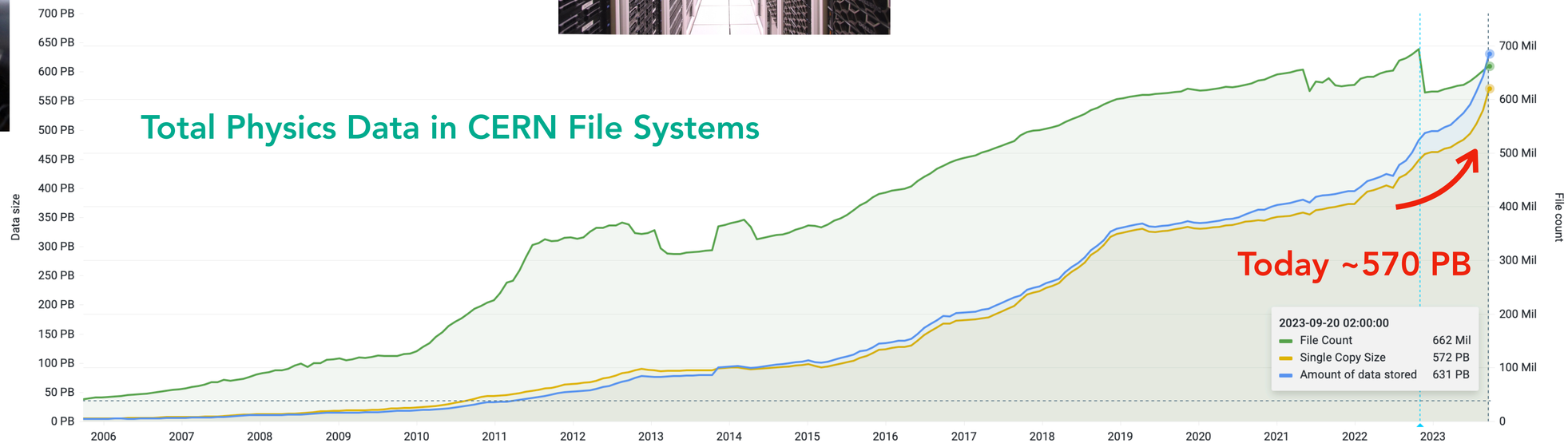


Data Saving

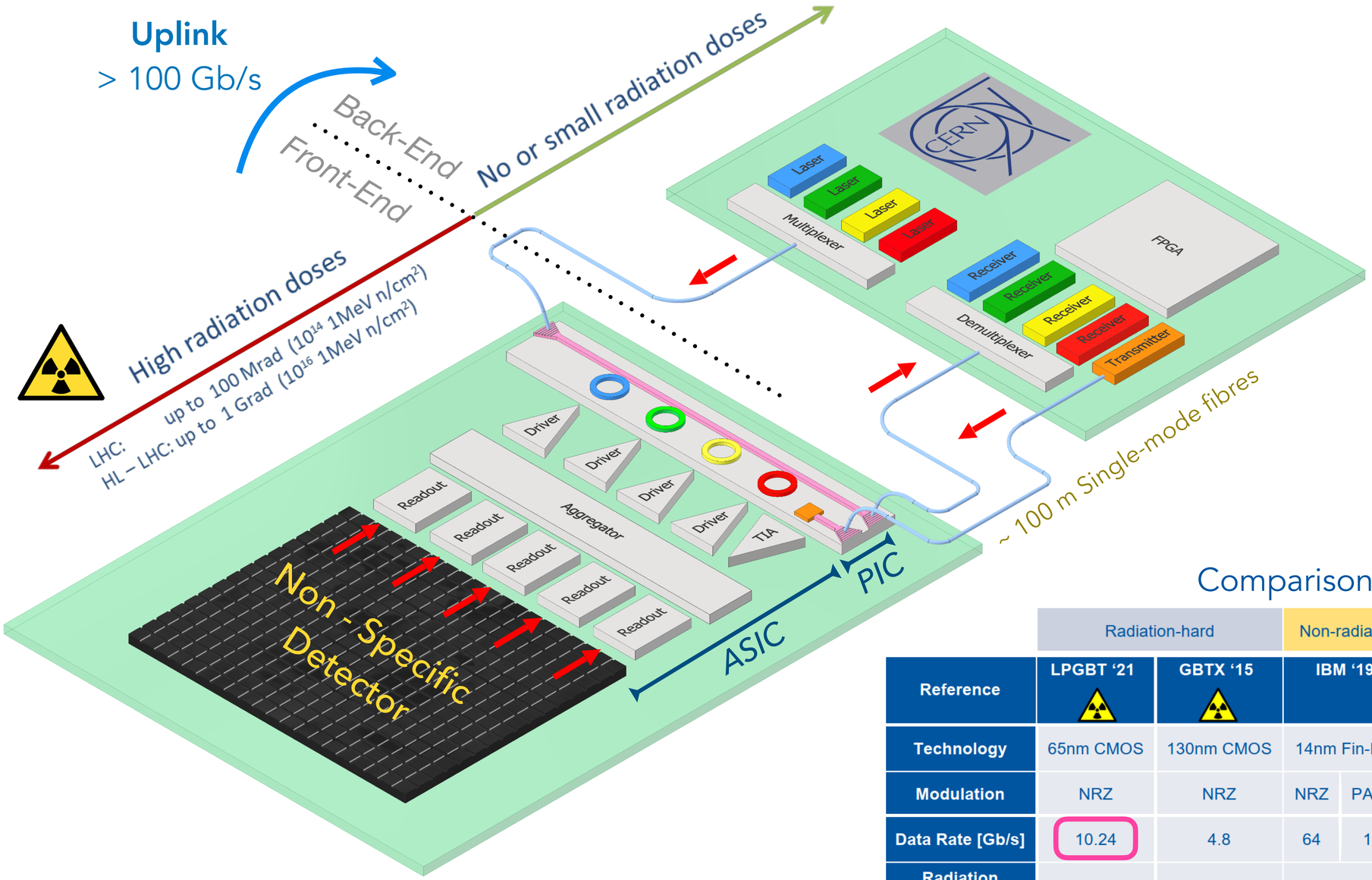
Burst
> 100 GB/s

Storage





Novel Concepts by EP-ESE Group



- 4x Lanes with NRZ symbols of 25.6 Gb/s each
- Serialiser ASIC relying on CMOS technology at 28 nm
- Exploitation of Silicon Photonics Integrated Circuits
- Optical wavelength multiplexing for band aggregation
- Low power and low mass

Comparison with other solutions (@ 2021)

	Radiation-hard		Non-radiation-hard (research)		Non-radiation-hard (commercial)				
Reference	**LPGBT '21**	**GBTX '15**	**IBM '19**		**Xilinx '21**	**Xilinx Ultra scale+**		**Intel Agilex F-Series**		**Xilinx Virtex-6 '09**
Technology	65nm CMOS	130nm CMOS	14nm Fin-FET		7nm Fin-FET	16nm Fin-FET		10nm Fin-FET		40nm CMOS
Modulation	NRZ	NRZ	NRZ	PAM-4	PAM-4	NRZ	PAM-4	NRZ	PAM-4	NRZ
Data Rate [Gb/s]	10.24	4.8	64	128	112	32.75	58	32	58	11.2
Radiation Hardness	200 Mrad	100 Mrad	Not applicable		Not applicable	Not applicable		Not applicable		Not applicable

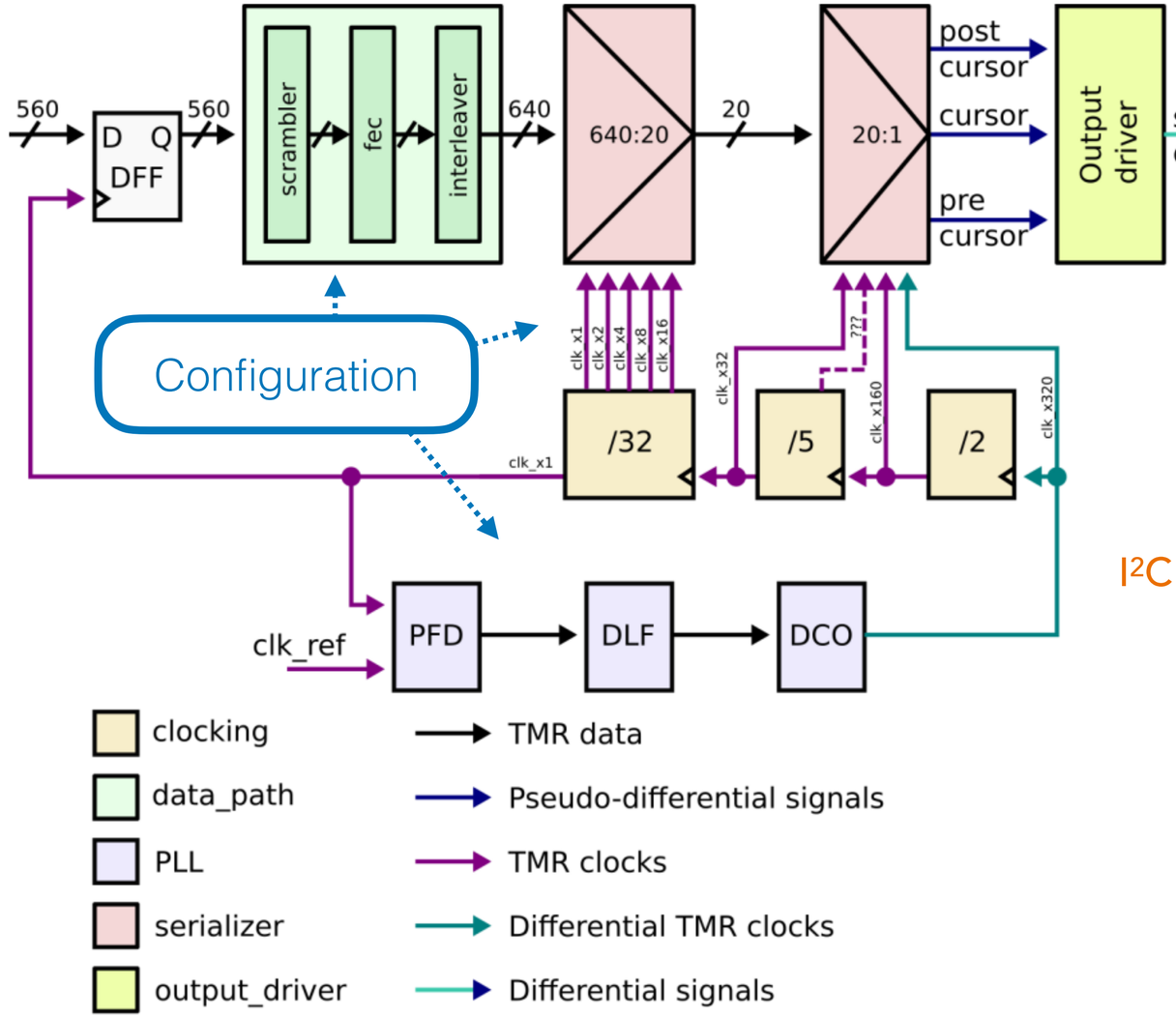
CERN SoA

Overview of DART28 Architecture

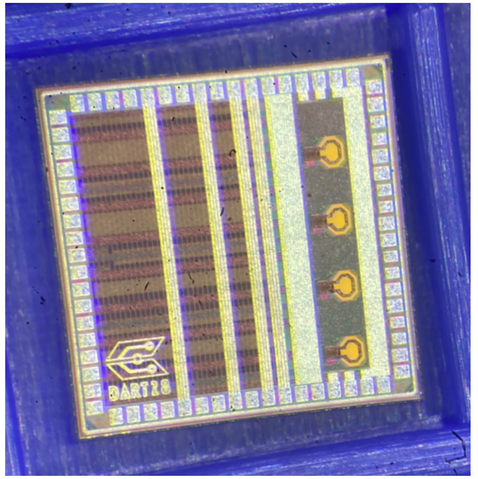
The **DART28** (**D**emonstrator **A**SIC for **R**adiation-Tolerant **T**ransmitter in **28** nm) represents the proof of concept for fast data serialisation and driver

Dummy user data Generator

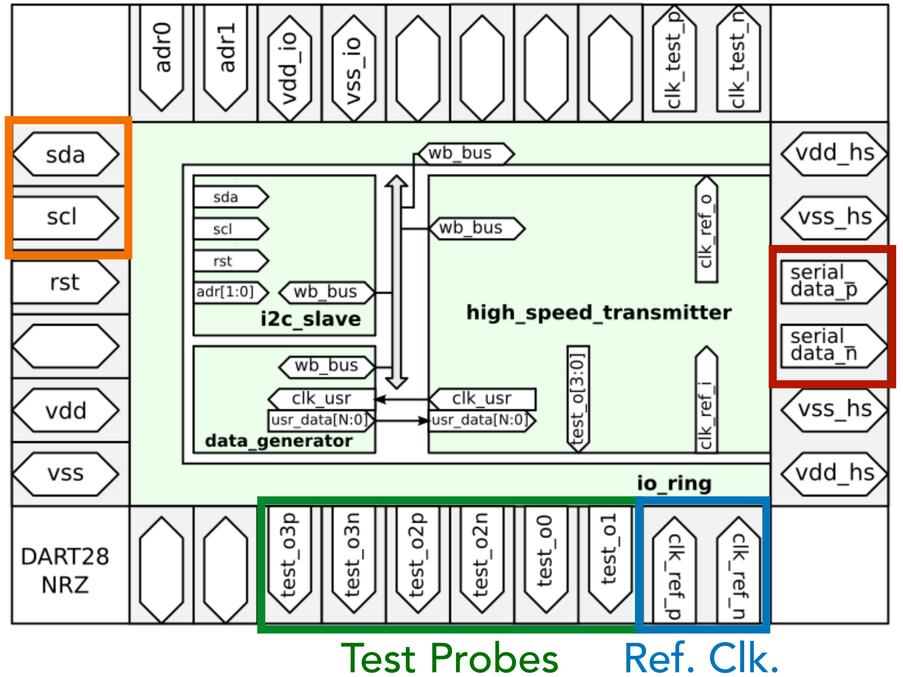
- PRBS
- Bit Patterns
- Synth. Clocks
- Counters
- Constant



DART28 die

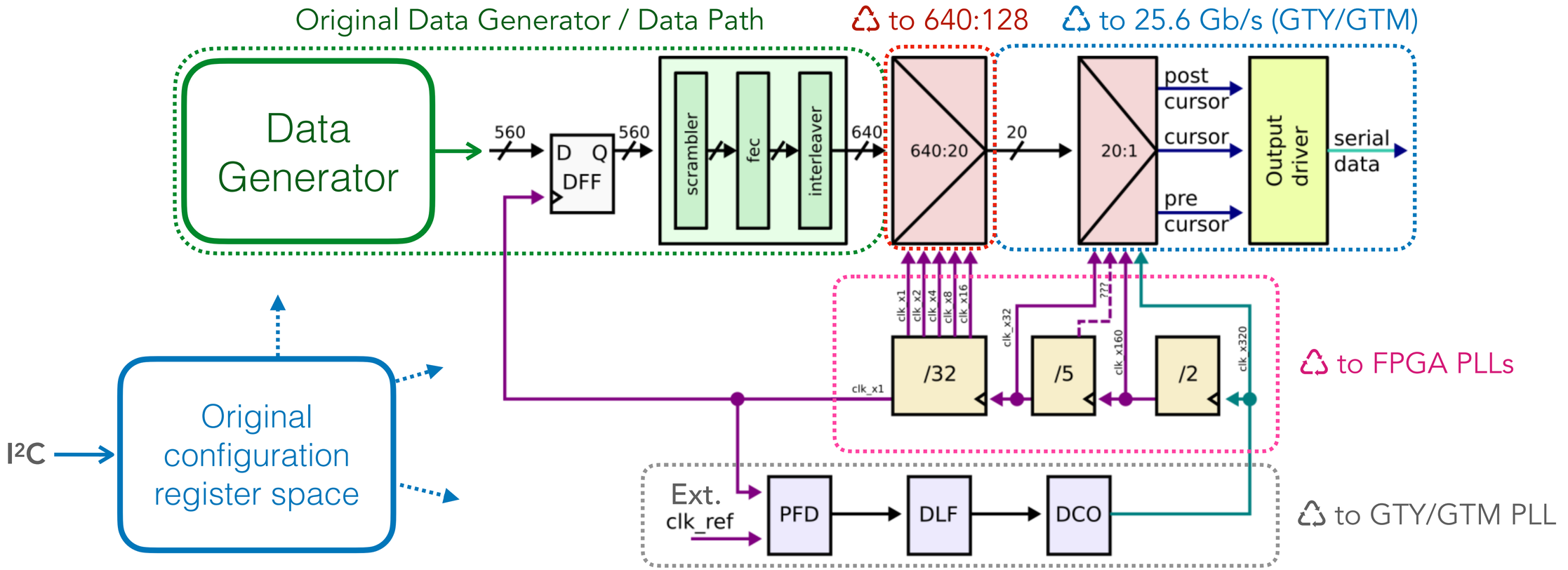


I/O Overview



FPGA based Emulator

1. Target agnostic HDL codes (Verilog) are ported to the FPGA;
2. Specific primitives are replaced with FPGA ones: transceivers, PLLs, I/Os;
3. Additional diagnostic cores can be added if required.



Benefits brought by the emulator

at System Level:

- To enable an **effective test-bench engineering** in view of the prototype delivery
- To **test the RTL functionality** without the need for the actual ASIC
- To **qualify the equipment / components involved** into the test-bench (QSFP modules, cabling, clocks, …)
- To **tailor the own project features** on the basis of commercially available solutions (Transceivers)

at RTL design:

- It allowed to **correct bugs in the RTL codes** and to **optimise the implementation** of logics
- The analysis of the codes from a different perspective and tools
- To tune the initial device configuration

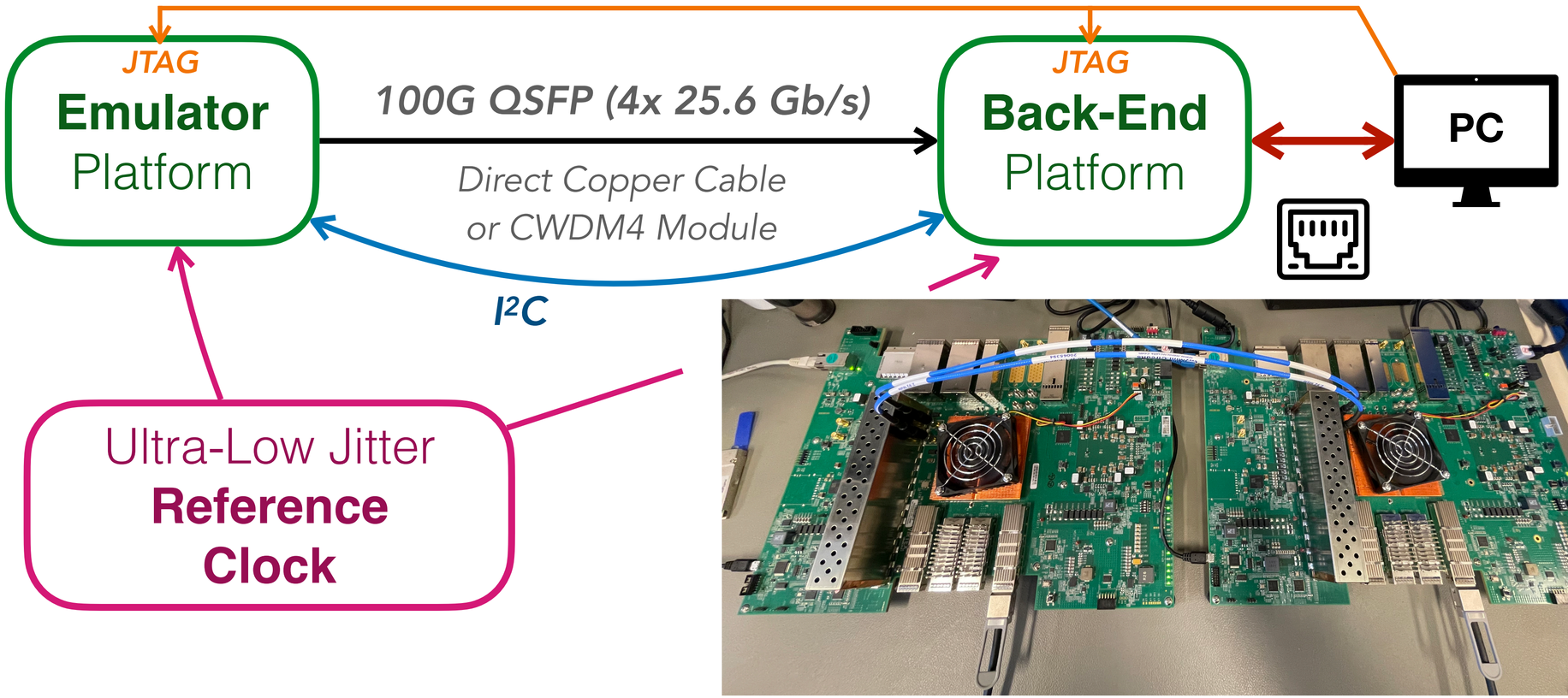
Emulator Setup

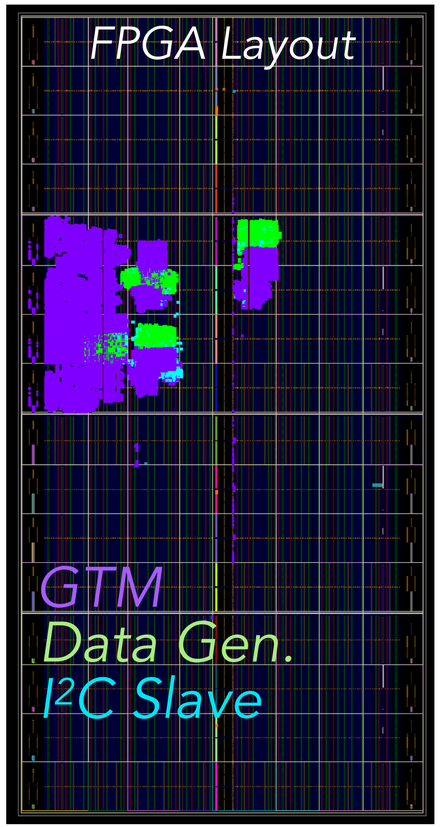
An AMD VCU129 Evaluation Board has been adopted, featuring the Virtex UltraScale+ XCVU29P

Resource	Utilization	Available	Utilization %
LUT	69551	1728000	4.02
LUTRAM	1213	791040	0.15
FF	70990	3456000	2.05
BRAM	64	2688	2.38
DSP	280	12288	2.28
IO	14	448	3.13
BUFG	78	1344	5.80
MMCM	8	16	50.00
PLL	1	32	3.13

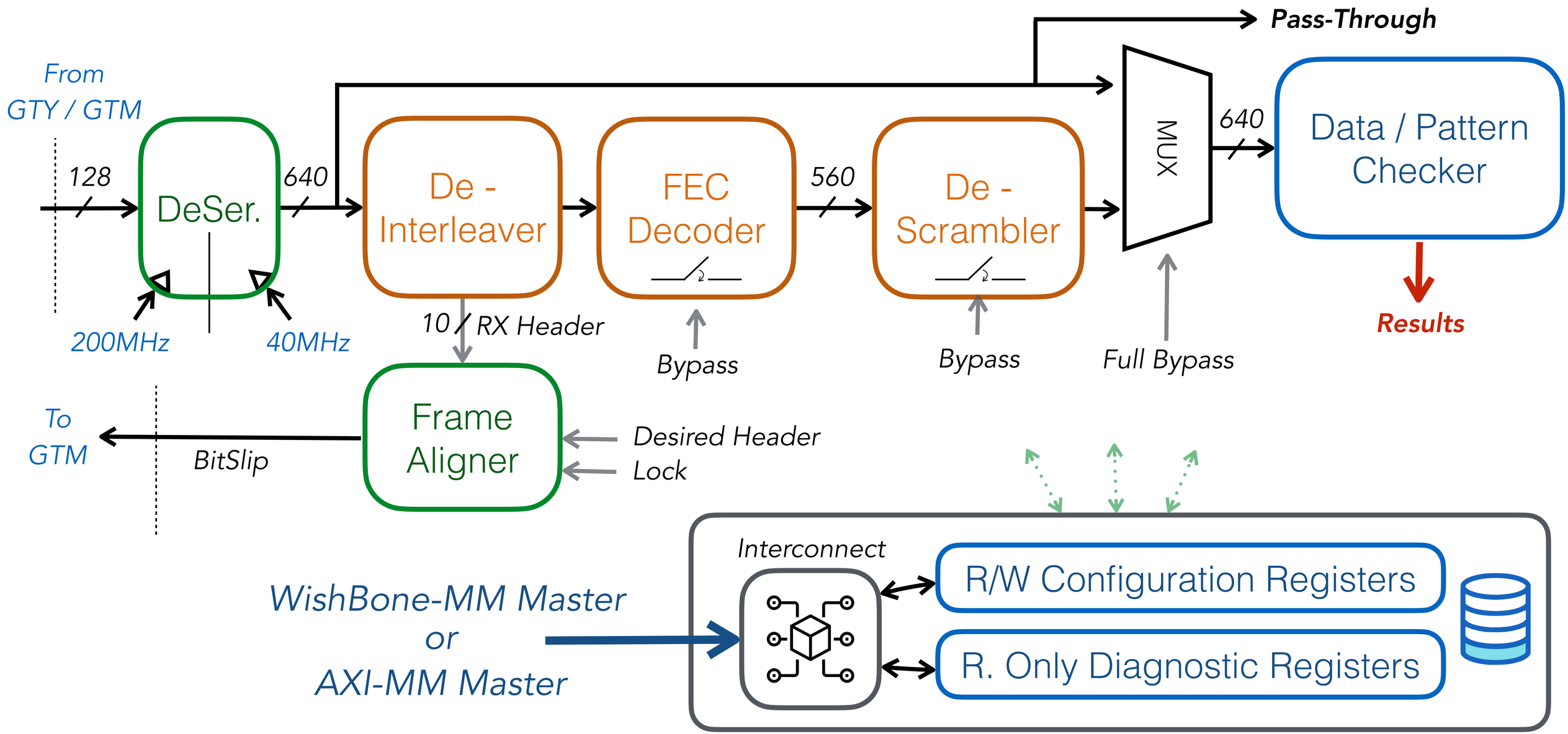
FPGA Key Specifications

GTM 56Gb/s PAM4 Transceivers	48
GTY 28Gb/s Transceivers	32
100G / 50G KP4 FEC	24 /48
100G Ethernet w/ KR4 RS-FEC	15
Block RAM + UltraRAM (Mb)	454.5
DSP Slices	12,288
System Logic Cells (K)	3,780

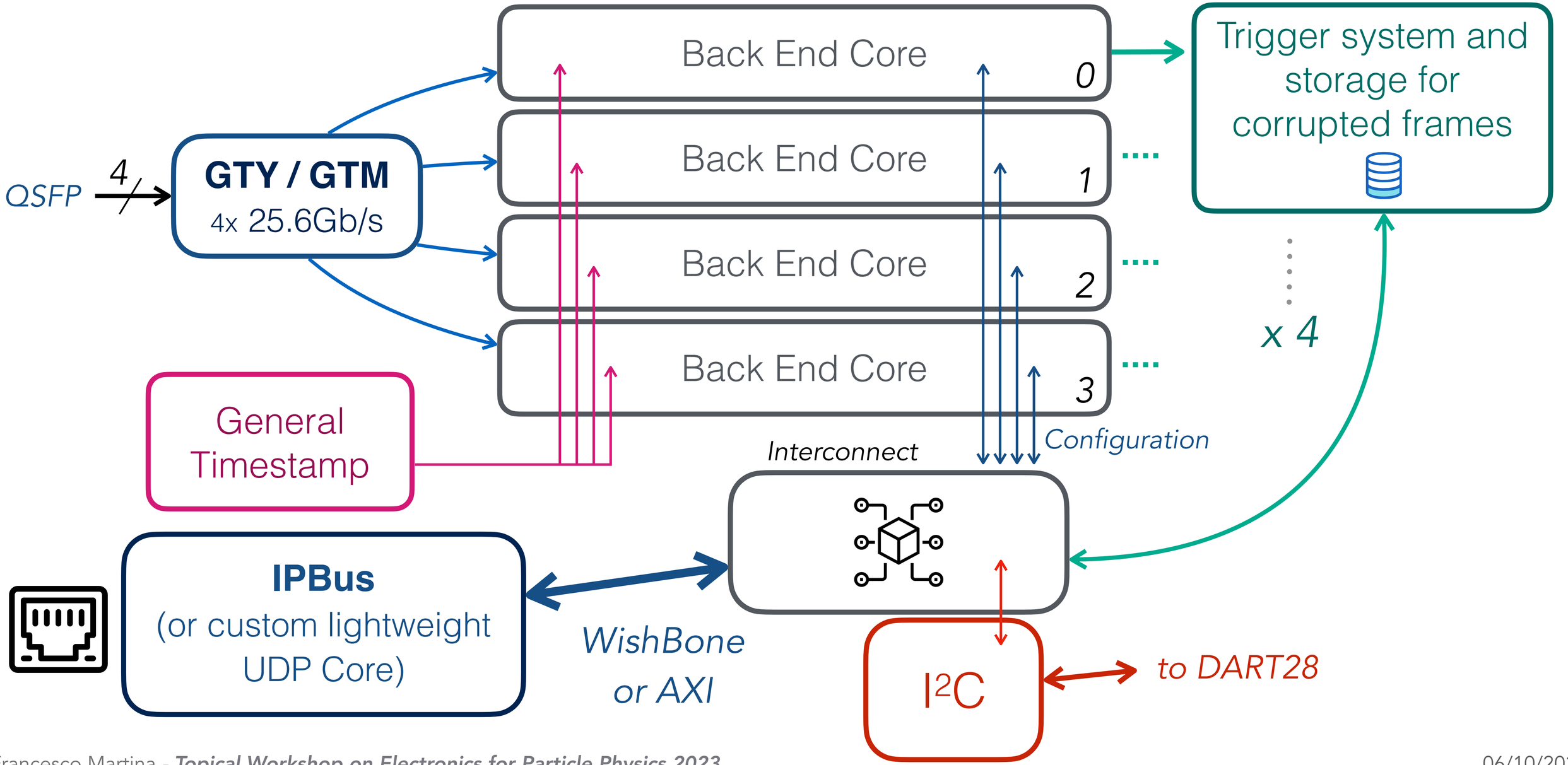




The DART28 Back-End Core



Overall Back-End Firmware for Testing



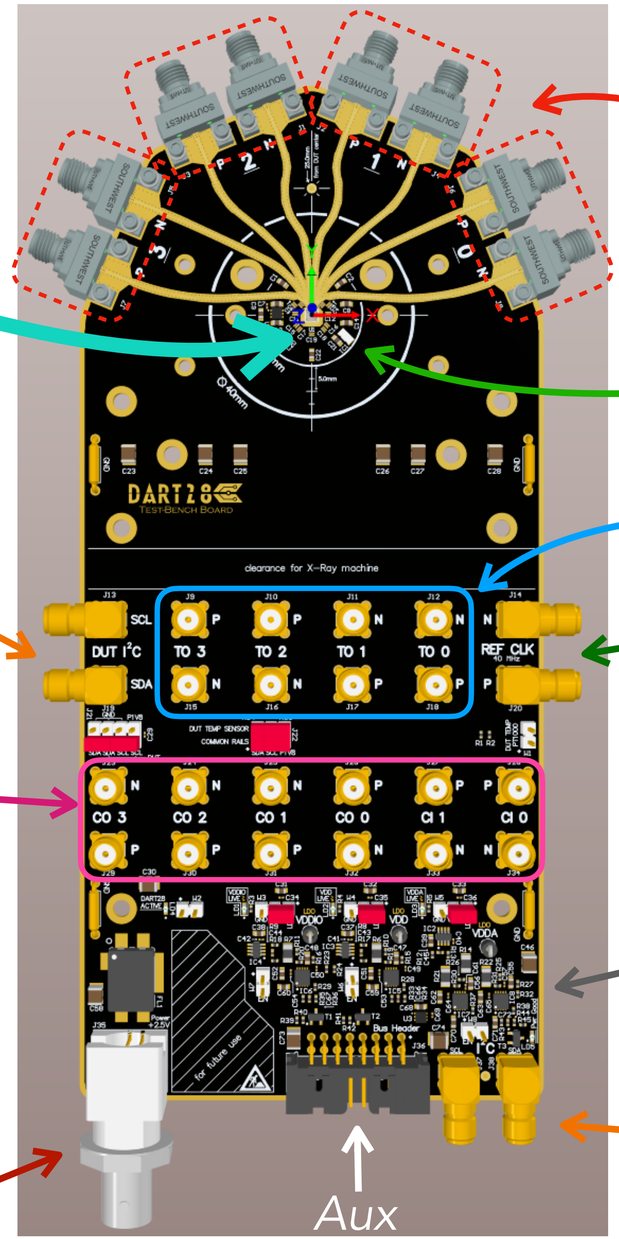
DART28 Test-Bench Subjects

- The basic electrical behaviour of the device: **current / power consumptions**
- Configuration environment: **I²C access, register map operations**
- Time domain signal integrity of the high speed links (HST) : **eye diagram, jitter analysis**
- Frequency domain signal integrity of HST: **phase noise analysis**
- System level studies of data transmission with FPGA: **bit error ratio analysis, FEC / Scrambler / Interleaver test**
- Detail analysis of the **embedded PLL**
- Advanced features for the eye quality enhancement: **pre/post emphasis**
- Device **operation at different voltage / temperature corners**
- Production **technology validation**
- Radiation test for Total Ionising Dose (**TID**) and Single Event Upset (**SEU**): X-Rays and Heavy-Ions

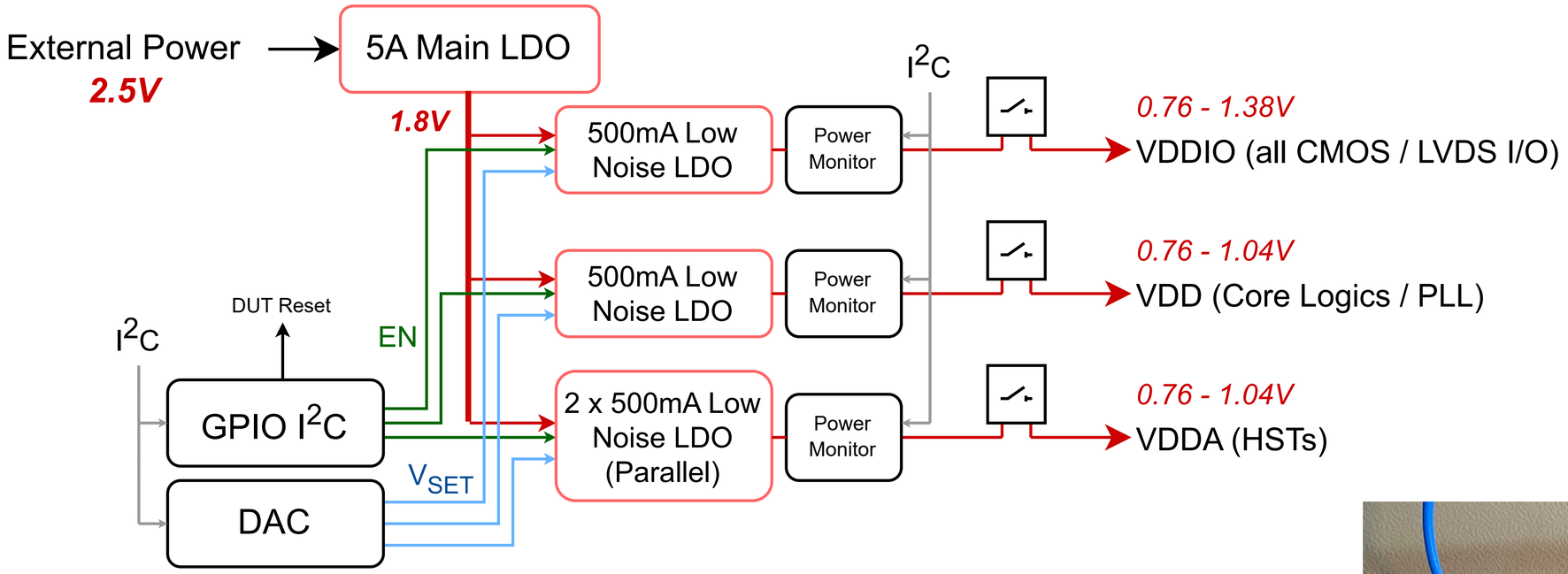
Characterisation Board

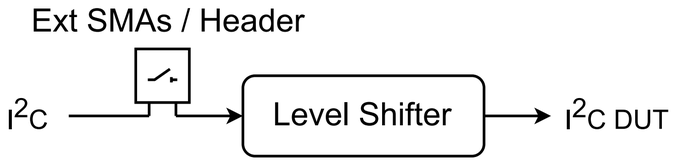
Key Features

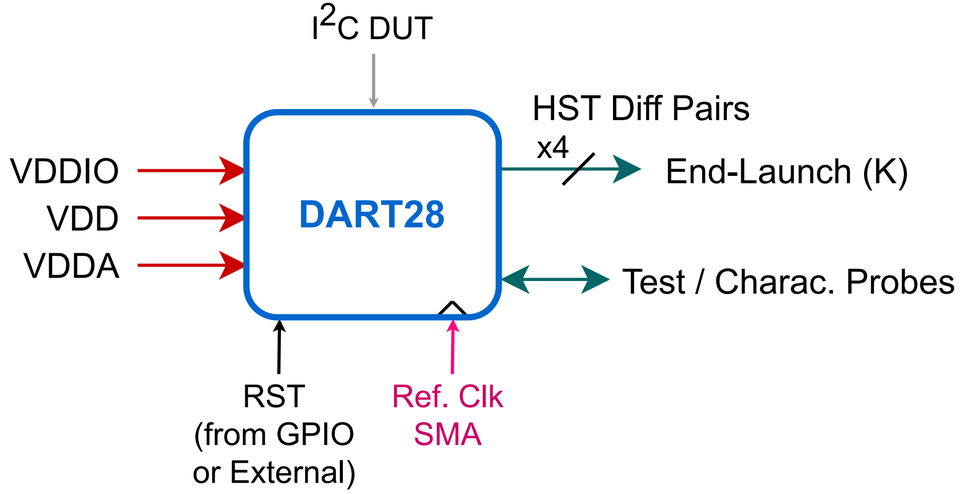
- Wire-bonding support (layout + ENEPIG finish)
- Ultra-low transmission loss Megtron 6 substrate
- Length minimisation for the high speed lanes
- High performance end-launch connectors
- Access to the full features of the tested device
- Low noise power regulators on-board
- High accuracy voltage / current monitors
- Temperature monitoring
- Mechanically compatible with assembly and testing equipment (wire-bounder, X-Rays, heavy-ions facility)



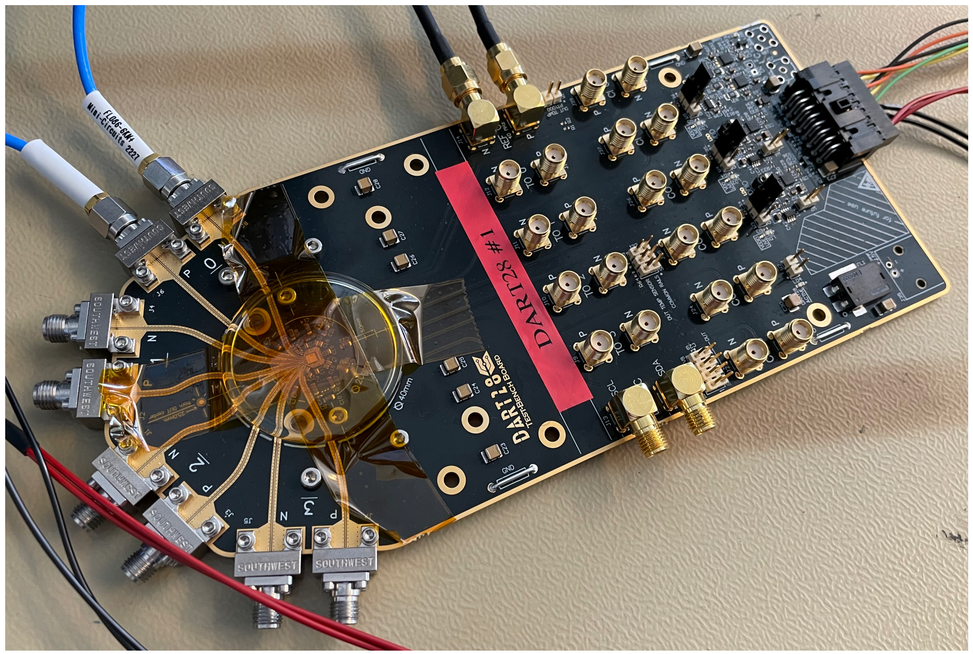
Overview of the Board Electrical Architecture





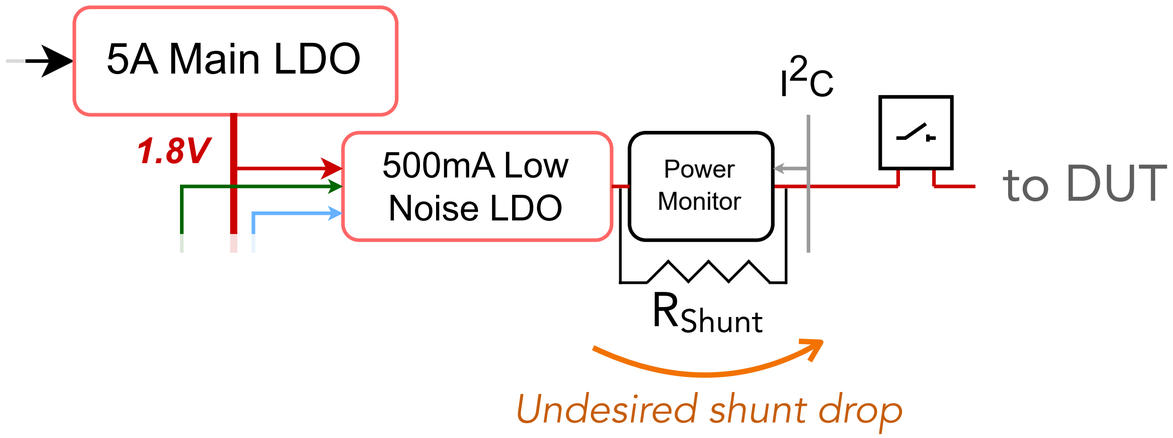


Assembled Board

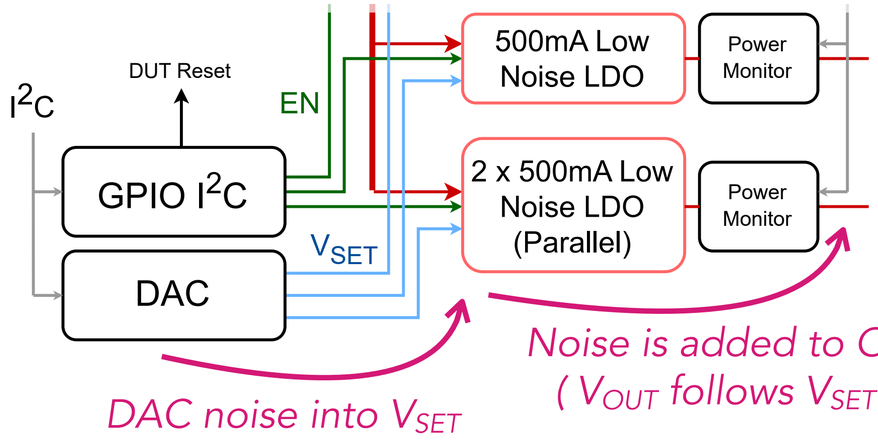


Some Design Challenges

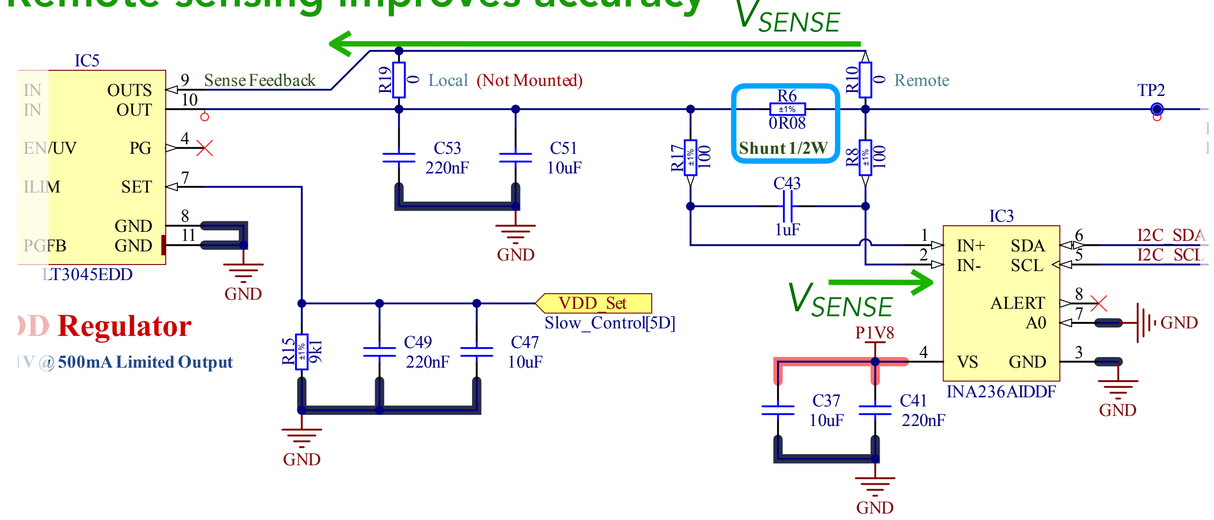
Voltage Control Accuracy



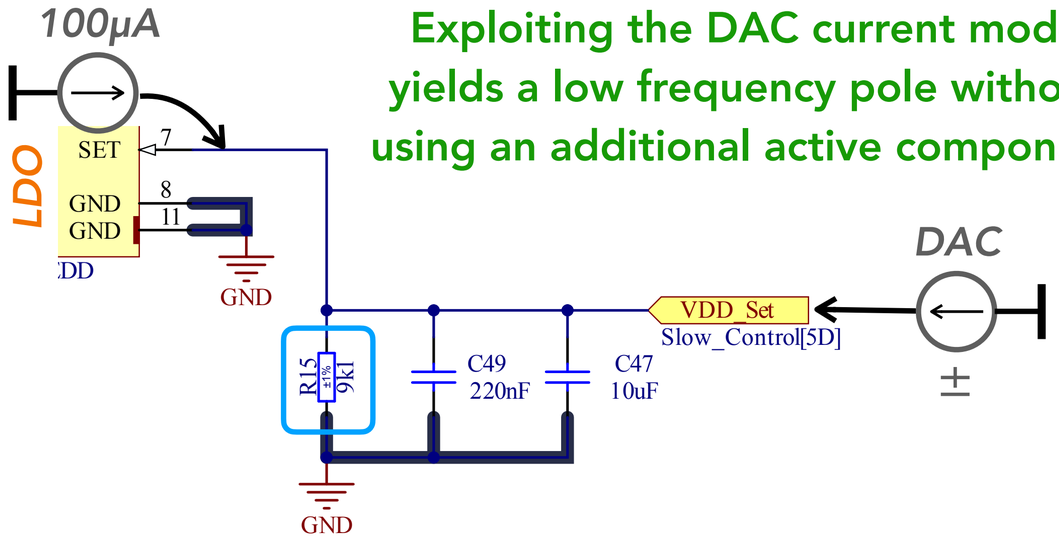
Noise Injected by DAC



Remote sensing improves accuracy

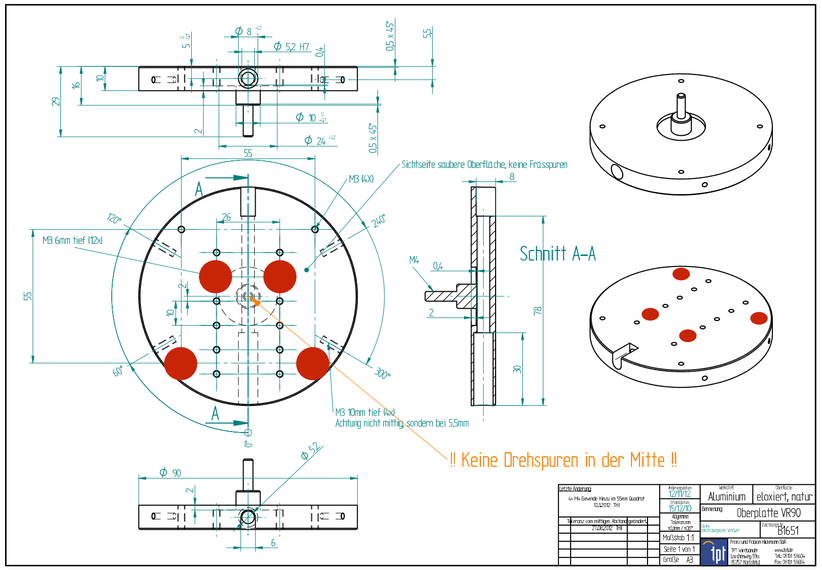


Exploiting the DAC current mode yields a low frequency pole without using an additional active component

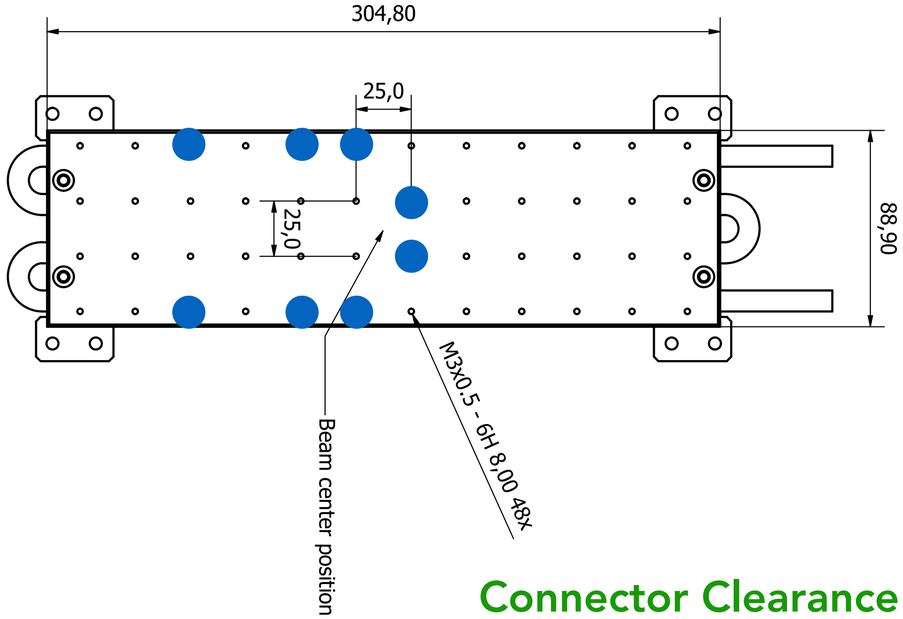


Some Design Challenges

Wire-Bonding Support

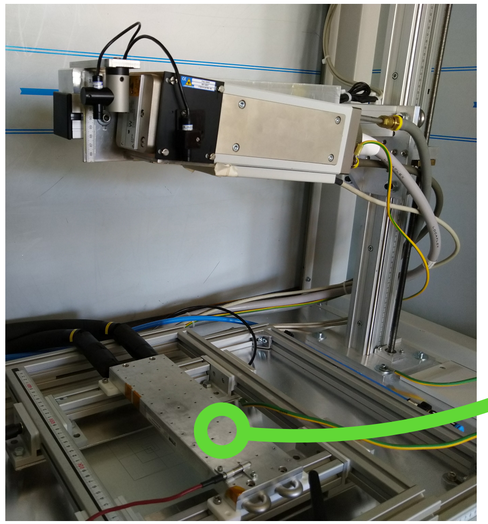


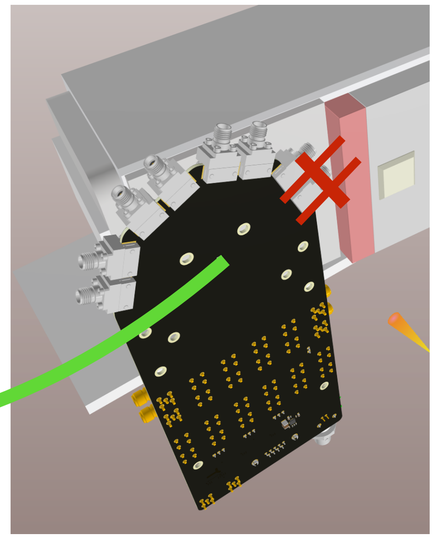
Support for Radiation Tests



Wire-Bonding Machine

Connector Clearance





X-Rays Head

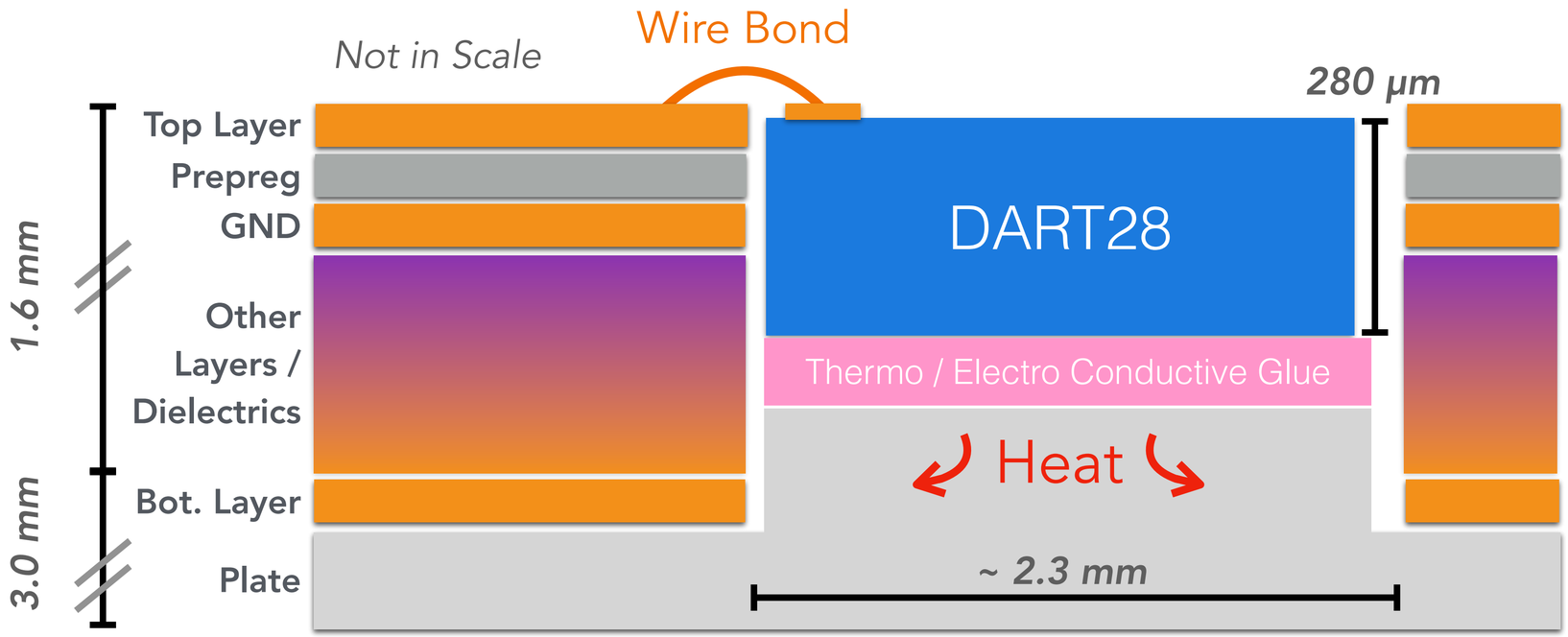
Some Design Challenges

Wire-Bonding Optimisation

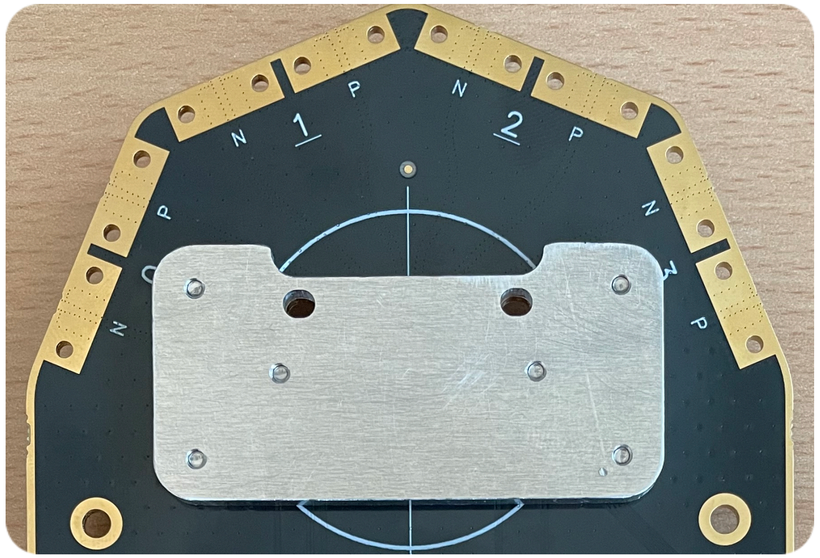
The wire length must be minimised
by levelling of surfaces

To reduce the parasitic inductance in series to power rails

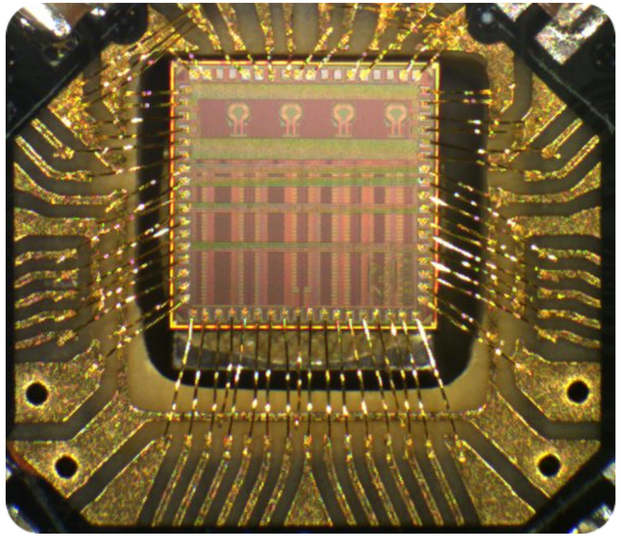
To improve the signal integrity in the high speed lanes



Support Plate for the Device



Wire-Bounded DART28



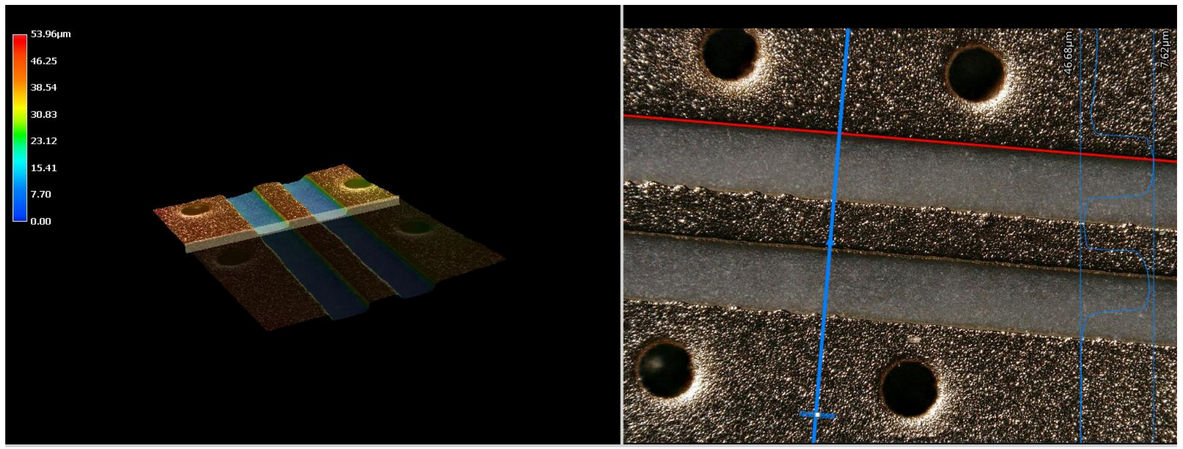
Some Design Challenges

Routing Optimisation

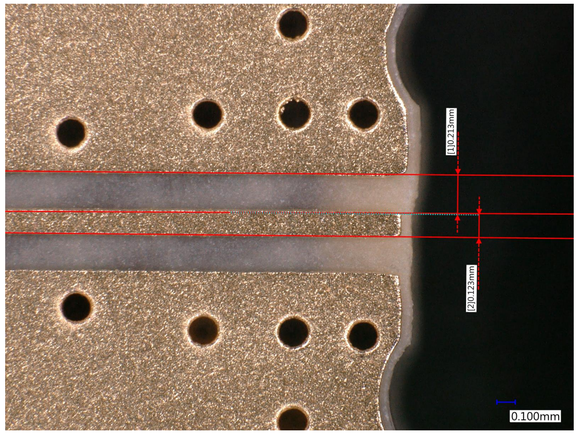
The high speed lanes require careful considerations at the layout design stage:

Characteristic impedance control

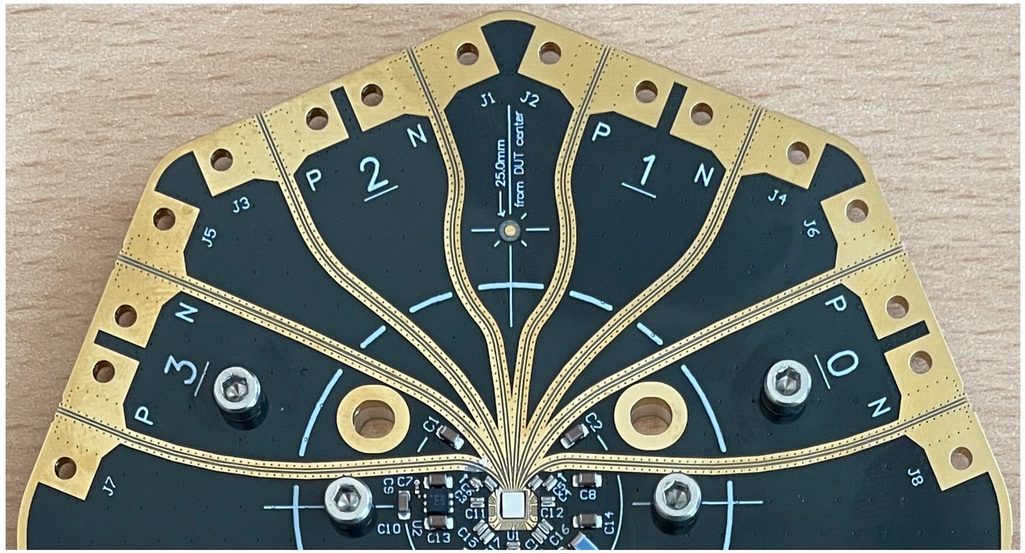
Single ended 50ohm coplanar micro-strip is chosen



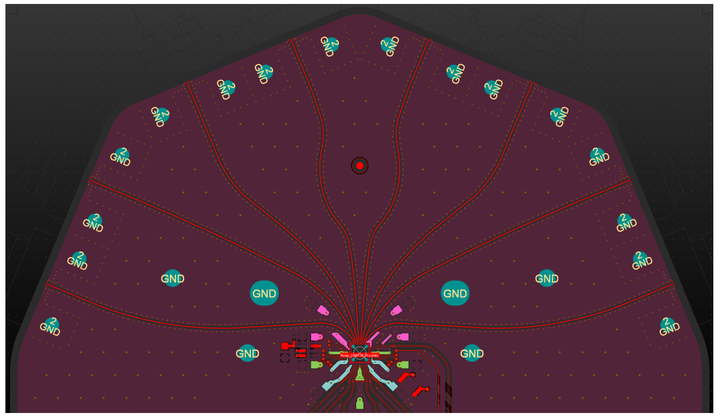
End-Launch transition mitigation

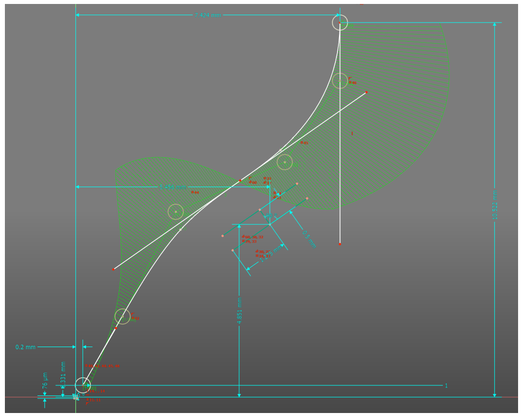


Smooth routing to maintain geometry characteristics



performed by the CAD Softwares: Altium Designer and FreeCAD

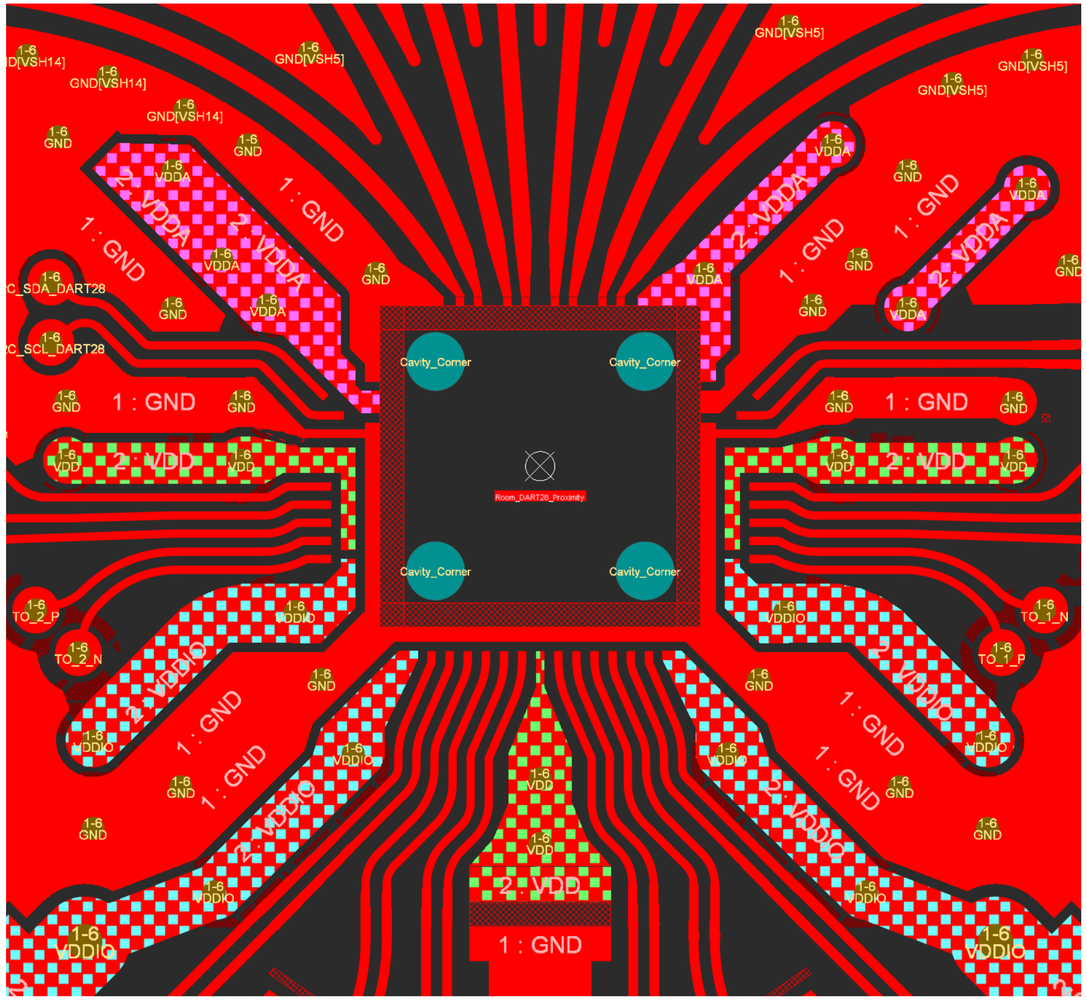




Some Design Challenges

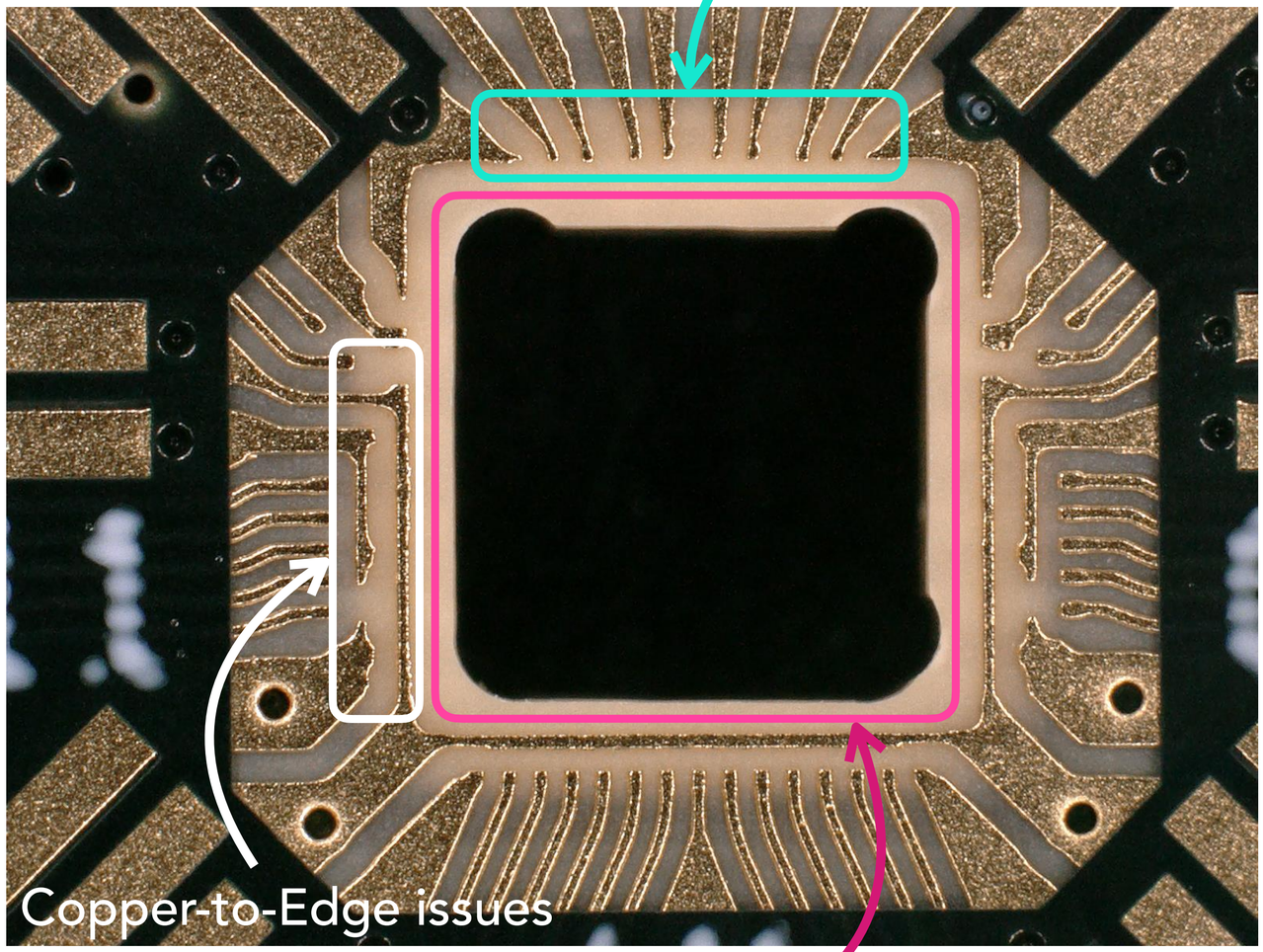
Maximum manufacturing capabilities must be deployed

3 mil (75 µm) trace / gap width are extensively used



Top layer close to the DUT cut-out

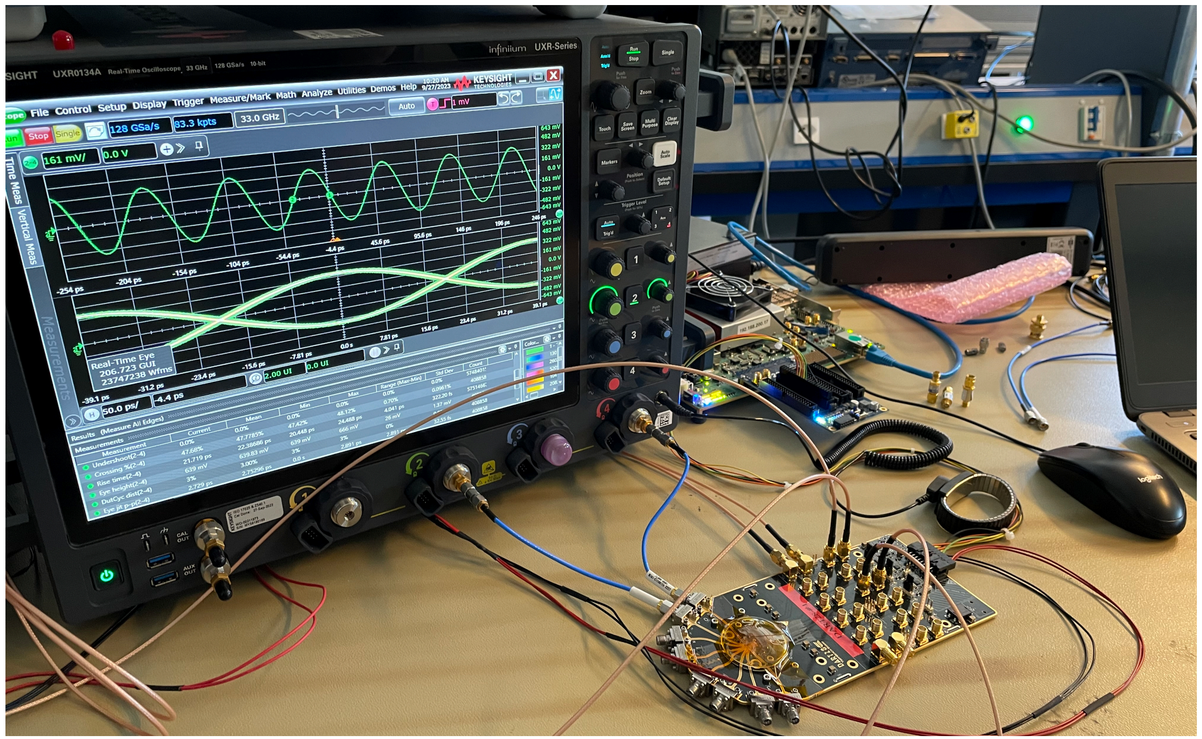
Risk of Over-Etching



Milling resolution at the limit

Conclusions

- A concept for a rad-hard 100G communication link in future HEP plants has been proposed
- A first prototype of the serialiser and driver has been delivered in August and it is currently under test, while the prototype for photonics will be delivered by the end of the year.
- The emulation activity has benefited both the system level and the design of the RTL logics
- The development of the back-end firmware is ongoing to fulfil all the required features
- Plans for the device testing have been stated and the test-bench architecture is established
- The features of the board have met the requirements and improvements for the future are underway
- Irradiation sessions have been booked for this year



Questions?

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