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Test Bench of a 100G Radiation Hardened Link for Future Particle Accelerators

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Pioneering physics experiments require increasingly faster data transfers and high-throughput electronics, which drives the research towards a new class of serialisers and optical links. In this framework, the DART28, a 100 $Gbps$ radiation tolerant serialiser and driver, has been designed in 28 nm CMOS technology and submitted in April 2023. The development has been coupled with an FPGA based emulation, which provided an early assessment of its behaviour, a scalable system-level demonstrator and an effective evaluation tool for compatible commercial solutions. The challenges faced in this research and the architecture of both the hardware setup and the firmware will be described.

Summary (500 words)

The most recent activities of the Electronic Systems for Experiments Group at CERN include the engineering of cutting-edge solutions for high-throughput data communication between the experimental area and the readout infrastructure for future detectors (in the framework of the CERN EP R&D programme). Because of the prohibitive conditions imposed by the radiation surrounding the particle beam paths, it is necessary to rely on the development of ASICs resistant to TID above 1MGy and mixed-field fluxes. Such components involve a complex design flow, a detailed verification of the embedded features and standardised post-production testing procedures.

In particular, the DART28 device is being developed in view of the future particle accelerators and it represents a pioneer 28nm CMOS based integrated circuit, delivering a 100G class data transfer over 4 lanes, which operate at 25.6Gb/s each. In the foreseen system, the DART28 will eventually be paired with a radiation-hard optical transmitter based on silicon photonics technology, which will adopt a CWDM technique for the aggregation of the links. This can be easily matched to commercial solutions based on QSFP modules for receiving data in the readout crates.

To enable an effective verification of the logical functionality of the device, a detailed emulation activity, based on modern Xilinx Ultrascale Plus series FPGAs, was initiated prior to submission to the foundry. Such a methodology has involved many challenges concerning the migration of the original customised primitives to FPGA ones and has represented a valuable complement to the development of this category of digital ASICs. In particular, it proved effective for the analysis of the system-level characteristics. In addition, such a platform enabled a realistic reproduction of the device's behaviour before its actual submission, facilitating: the upcoming validation planning, the resolution of potential difficulties that may be encountered in the testing environments and the design of the laboratory testbed. Finally, it paved the way for the engineering of the DART28 back-end counterpart, which represents the core of the validation system and one of the key deployable products for the eventual project commissioning. At this stage, programmable logic devices of the same family were employed for such a component, the architecture of which has been optimised to allow further automation of the device qualification procedures and the scalability of data links under test. The architecture of both the hardware setup and the developed firmware will be described in the present work.

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