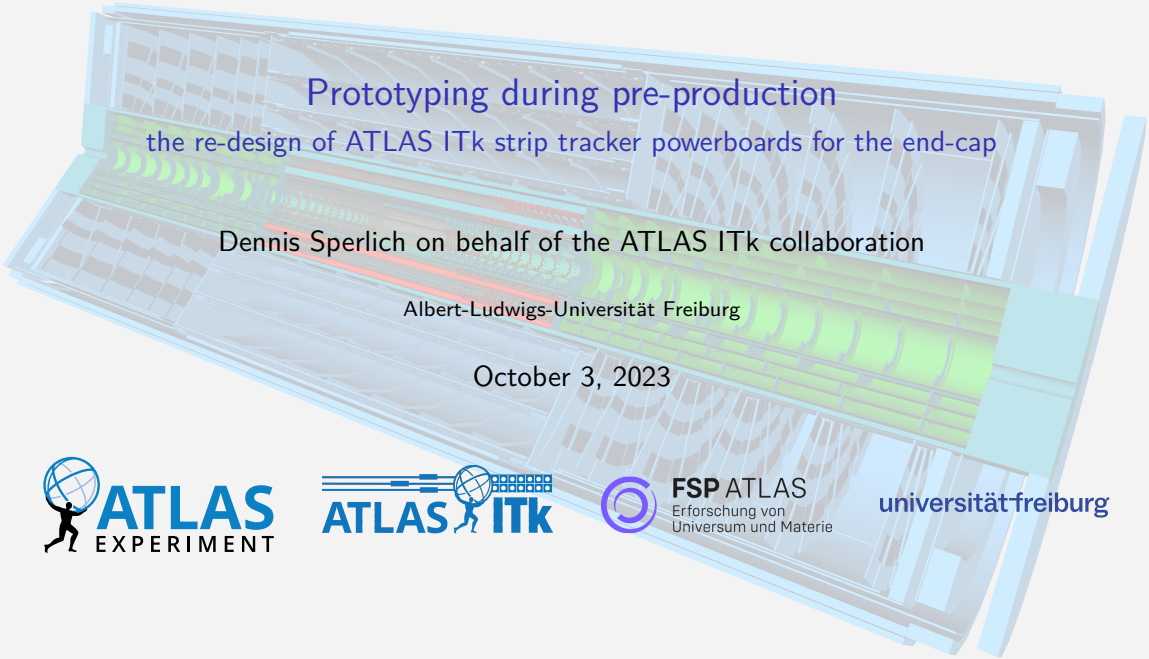

Prototyping during pre-production

the re-design of ATLAS ITk strip tracker powerboards for the end-cap

Dennis Sperlich on behalf of the ATLAS ITk collaboration

Albert-Ludwigs-Universität Freiburg

October 3, 2023

ATLAS EXPERIMENT

ATLAS ITk

FSP ATLAS
Erforschung von
Universum und Materie

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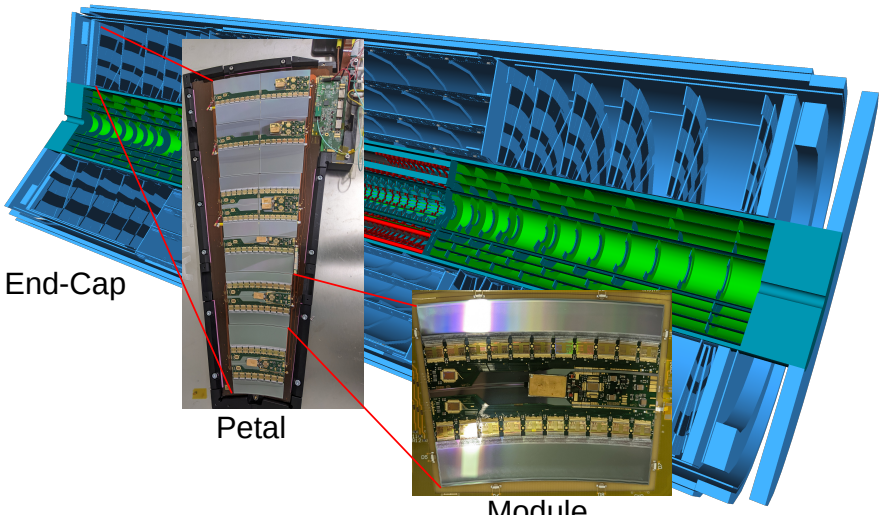
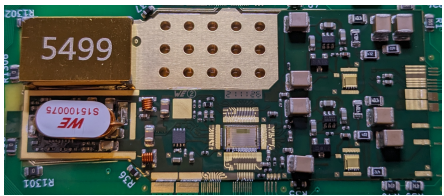
Endcap to Module

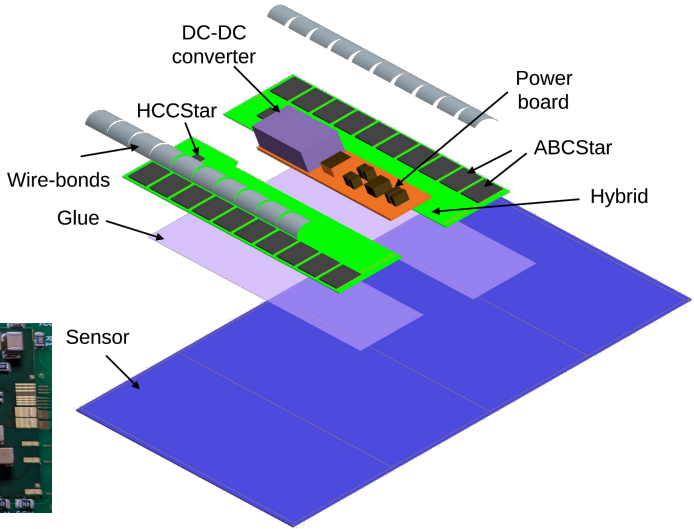
- 6 module types in Endcap



Module

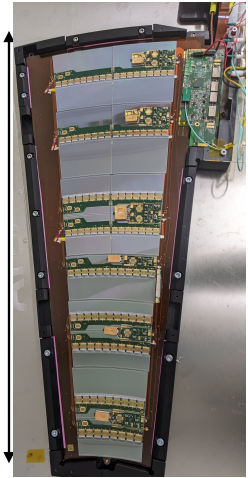
- Readout flex:
  - Frond-end chip ABCStar
  - Data aggregator chip HCCStar
- Powerboard:
  - DCDC (bPOL12V6)
  - Autonomous Monitoring And Control (AMACStar)
  - HV filter and switch





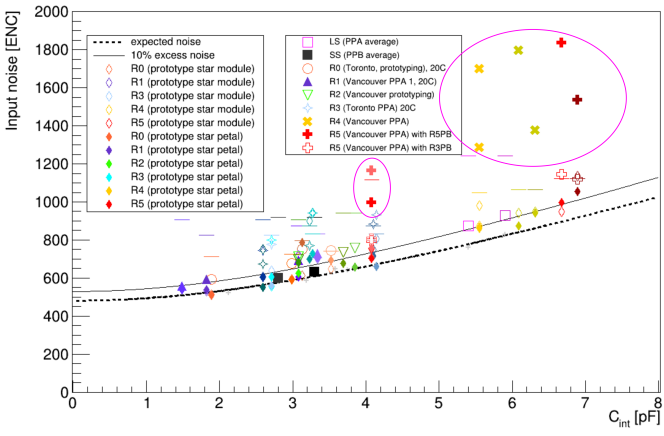
Powerboard design constrains

- Follow barrel design as much as possible
  - Branched off at prototyping version
  - Most changes ported over
- Adjust geometry for on 6 different modules, keep critical routing
  - Needed to be shorter + bent, but could be wider
- Keep components same / very similar, especially custom ones like coil, HV transistor, shieldbox
- Support more power (R3) and multiple sensors (R3,R4,R5)
- Limited availability of parts resulted limited testing opportunity



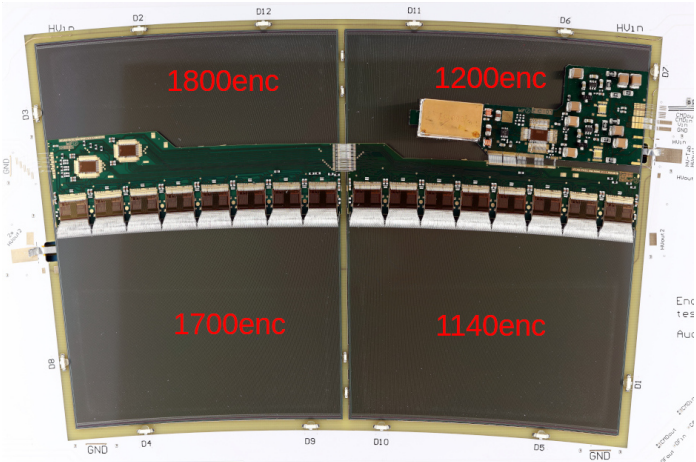
- Same requirements in terms of noise / electrical performance as in barrel
  - Only R0 tested properly during prototyping
  - R1, R2 and R3 made during prototyping but could not properly be tested
  - R45 was intended to be a cut down R3 powerboard (lower power requirement)
  - R45 was tested last, as early modules were build with partially populated R3

Noise problem with first prototype modules



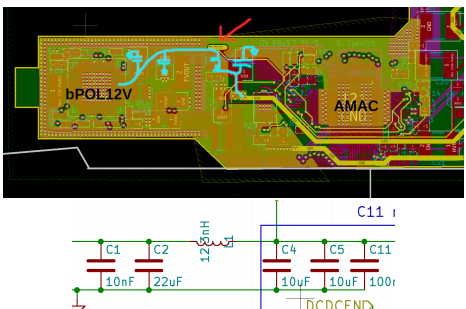
- Noise of R0-R3 was a little high, but most segments were technically still in our S/N requirement of 1:10
  - First one or two modules of these types in existence built without tools
  - Did expect small improvements due to better build quality
- R4 and R5 started with R3 powerboards which showed acceptable noise performance
  - Another reason why R3 was suspected a fluke
- After adding R4 and R5 with their own powerboard to the plot we have seen a real noise problem we couldn't ignore
  - Didn't initially make sense as R45 was just R3 powerboard with unused PCB removed

What did we see?

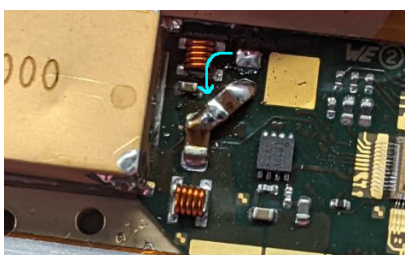


- Expected noise from capacitor loaded single chips: ~ 900 ENC, got 1200 on one sensor and 1700 on other
- the higher noise was on sensor not housing the powerboard
- Started a taskforce to solve this issue

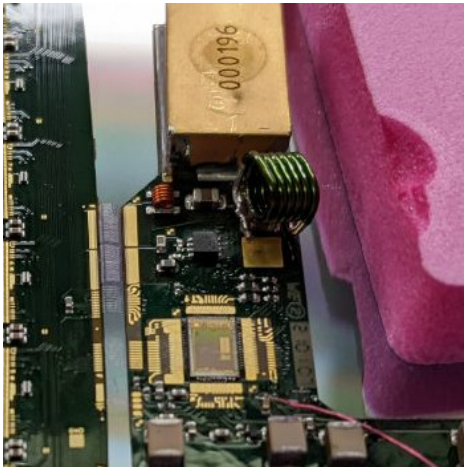
What was the source?



- Restriction in GND plane (red arrow)
- Impedance in GND path of input pi filter too high
- AMAC on same GND island as input pi filter cap
  - Stacking different capacitor values helped
  - Connecting the cap to the DCDC GND island reduced noise a couple 100 ENC

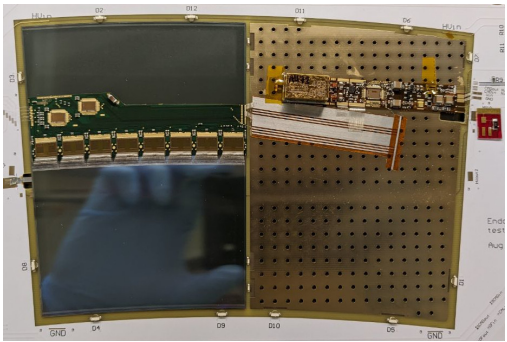


What was the source?

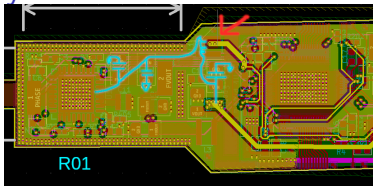


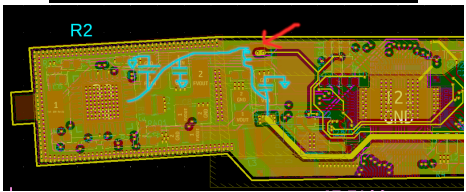
Test modules with modified power-board and only left sensor

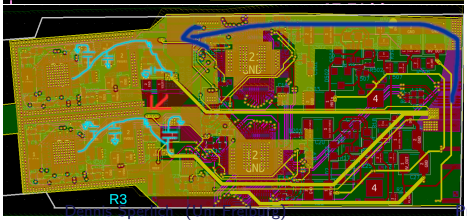
- Original 12nH coil actually borderline sufficient
  - Fitting a 47nH coil on old R45 flex achieved 1100/1400 ENC
  - Fitting a 90nH coil on old R45 flex achieved 1100/1200 ENC
  - Barrel PB on non covered sensor: 1300 ENC



Why were other modules not as badly affected?



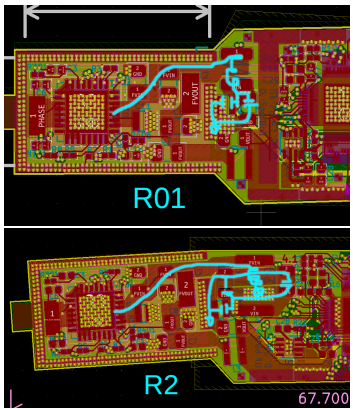




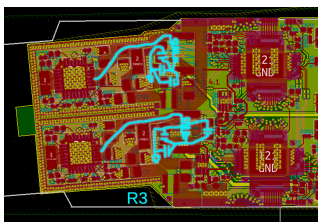
- R01 and R2 have cap on other side of restriction
  - Moving the capacitor GND connetion improved the R45 noise significantly as well
  - Single sensor modules less affected
- R3 has same restriction as R45 to AMAC
  - But much lower impedance to input pads (blue arrow)

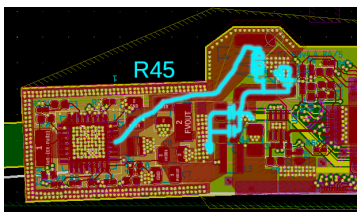
- After finding the issues with R45, the other flavours where found to have similar weaknesses $\rightarrow$ change them as well

Changes!

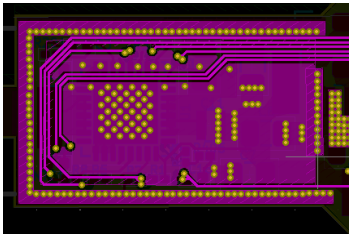


- Increase inductance in pi filter from 12nH to 90nH (R2,R3,R45) / 42nH R01 (space)
- Make sure both sides of pi filter are in big DCDC GND polygon
- Change 10nF 0402 to 100nF 0306 on input side of pi filter
- Add 1µF 0805 to 22µF 0805 on input side (R2, R3, R45)
- Decrease restriction in ground plane as much as possible
- Add PCB area to R45 for bigger coil + more capacitors

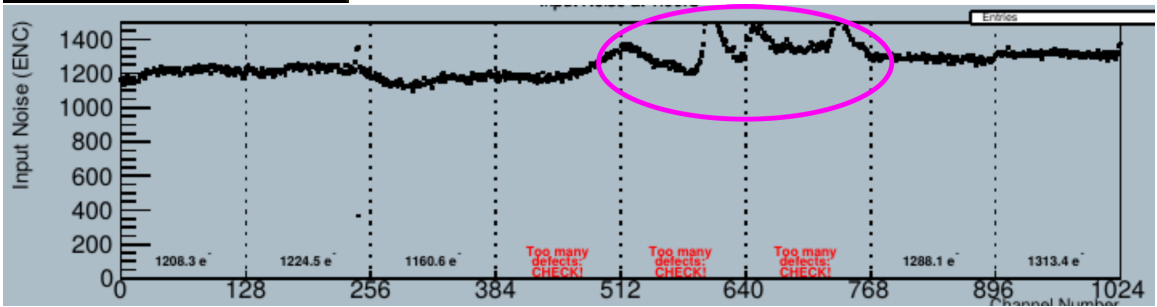




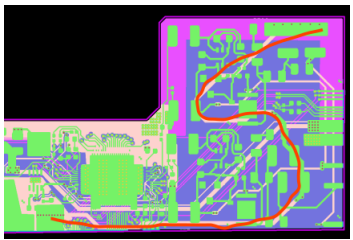
Other changes



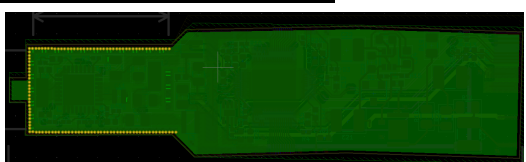
- Changed from stacked vias to staggered vias
  - Required by manufacturer to improve reliability long term
- Added more GND vias in pi filter region
  - Further strengthen the area which caused trouble
- Add more GND copper in second inner layer
  - attempt to reduce the noise peaks under the coil



Other changes to follow barrel pre-production design



- Have dedicated trace between HV filter GND and hybrid GND, no AMAC / DCDC current
- Move bottom layer vias from shieldbox edge to Input GND + AMAC + linPOL12V + input capacitor of pi filter + hybrid GND
  - Make bottom layer electrostatic shield in DCDC block
  - Use it to carry current up to linPOL12V and input capacitor



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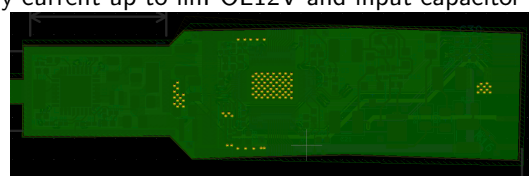
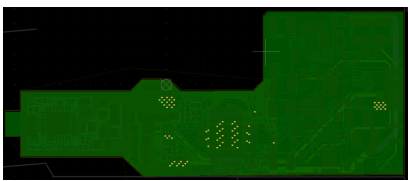


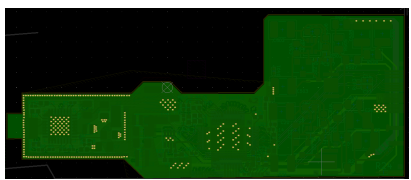
Design variants

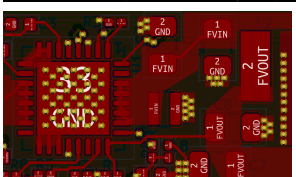
- In order to maximise the chance of success, we produced 3 design variants
  1. Implement all the changes I described so far
  2. Use bottom layer not as electrostatic shield, but rather to reduce the impedence of GND
     - only produced for R45
  3. change the low inductance capacitor next to DCDC to new CERN recommendation

No difference in noise seen between variants $\rightarrow$ chose variant 1 (most barrel like)

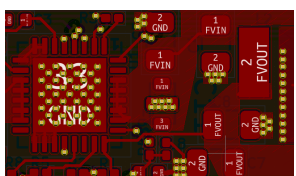


$1 \rightarrow 2$

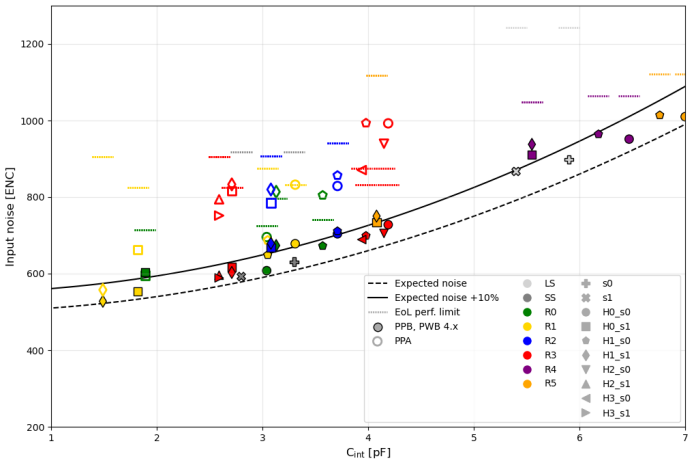




$1 \rightarrow 3$



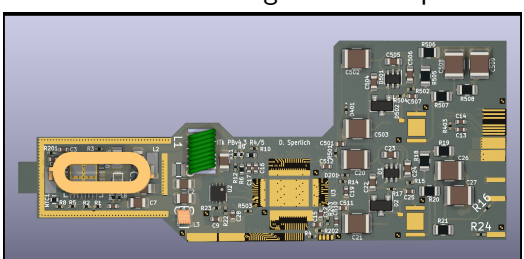
Noise performance



- Noise slightly higher than expected, but mostly within 10%
  - New PPB in solid markers
  - Old powerboards unfilled markers
- All noise levels well below our threshold of 10:1 S/N for end of life signal amplitudes

Design Change to concave R45

- During insertion trials of petals, a near collision of R5 shieldbox and carbon fiber rim was found
- Was overlooked in the 3D model due to a lost powerboard in the simplification of the petal model
- Found just after the submission of the R45 design variants
- Change outline of R45 to avoid collision with end-cap structure in R5
- No electrical change in this step – submission only after decision for variant 1 was made



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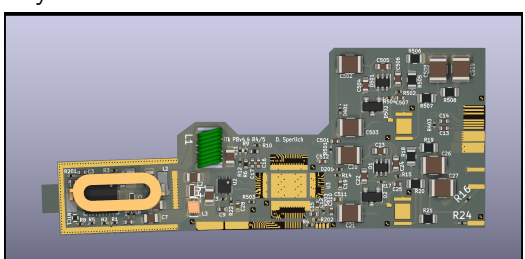

Summary

- EC powerbaord started as a relatively simple outline variants of the barrel powerboard
- Different positions of components thought to be less critical actually affected performance significantly
- The 20cm long HV trace + HVret to the second sensor increased the sensitivity to conducted noise to a degree incompatible with the original powerboard design
- Split sensor geometries only became available in pre-production
  - late discovery of the fundamental problem
- Layout changes were necessary to fix flaws + increase filtering
- Unfortunate staggering of design changes
  1. Increase input filter effectiveness for module performance
  2. Change to staggered vias due to inefficient communication from manufacturer about design rule changes
  3. Geometric change of R45 required after discovery of interference with global supports
- Powerboards with all the changes mentioned (except geometry change of R45) have been successfully built into modules with good noise performance