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Prototyping during pre-production: the re-design of ATLAS ITk strip tracker powerboards for the end-cap

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For the construction of the future ATLAS strip tracker end-caps, six geometries of silicon strip detector modules were designed. Each module comprises one or two silicon strip sensors and several flexes holding the required readout electronics, designed to match the geometry of each module. Due to the large number of designs, two module geometries using two sensors per ring module were prototyped for the first time in 2022, and showed excessively high noise. This contribution presents an overview of the follow-up investigation to diagnose the issue, the subsequent powerboard re-design and results from the first prototypes in 2023.

Summary (500 words)

Modules for the ATLAS ITk strip tracker are designed to meet several strict design criteria: a noise occupancy of $< 1\%$ and efficiency of at least 99% and a signal-to-noise ratio of at least 10:1 at the expected end-of-life fluence and dose. For the assembly of ITk strip tracker end-caps, six different module geometries were developed in order to provide sufficient coverage for tracking. The three module types located on smaller radii comprise one sensor (diced to maximise usable area of a 6"wafer) each, the module geometries located on outer radii require the combination of two sensors each.
Due to the high cost of prototyping especially sensor geometries, out of the six sensor shapes, only the innermost one was prototyped during the R&D phase. Dual sensor modules could only be prototyped as an approximate version using the existing sensor shape and an early development version of the powerboard. Using these combinations of prototype geometries, there was no strong evidence for excess noise during the R&D phase.

When the first prototype modules of all module geometries were assembled in 2022, the module types located at the outermost radii (R4 and R5) showed a noise excess far above the design specifications (up to twice the allowed maximum), making the approved design unusable for the production phase scheduled to begin within 12 months. Over the course of three months, an extensive investigation into the source of the excess noise was conducted by systematically modifying the test setup and module geometry. This process was made more complicated by the limited quantities of available parts: only two modules of each geometry (R4 and R5) were available world-wide to perform all necessary tests and modifications during this investigation. The tests included additional shielding, modified grounding and referencing and SMD component replacements.

Eventually, the powerboard, a kapton flex designed to control and monitor voltage and current for the module, was identified as the source of the noise. With the identification of the input filter as the noise source, a systematic weakness in all four powerboard designs was discovered. Improving the filtering was found to recover the module noise performance close to expectations.

With a pressing need for a re-design to produce a module within required specifications, several powerboard variations of the same geometry were designed and produced in parallel and became available for assembly into modules in 2023. Each design variant was assembled into at least two modules and their noise performance tested for comparison, leading to a design selection and first R4 and R5 module prototypes within specification, as well as a good understanding of the underlying issue.

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