TWEPP 2023

Topical Workshop on Electronics for Particle Physics

CMS Outer Tracker Phase-2 Upgrade: On-module Powering

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04/10/2023

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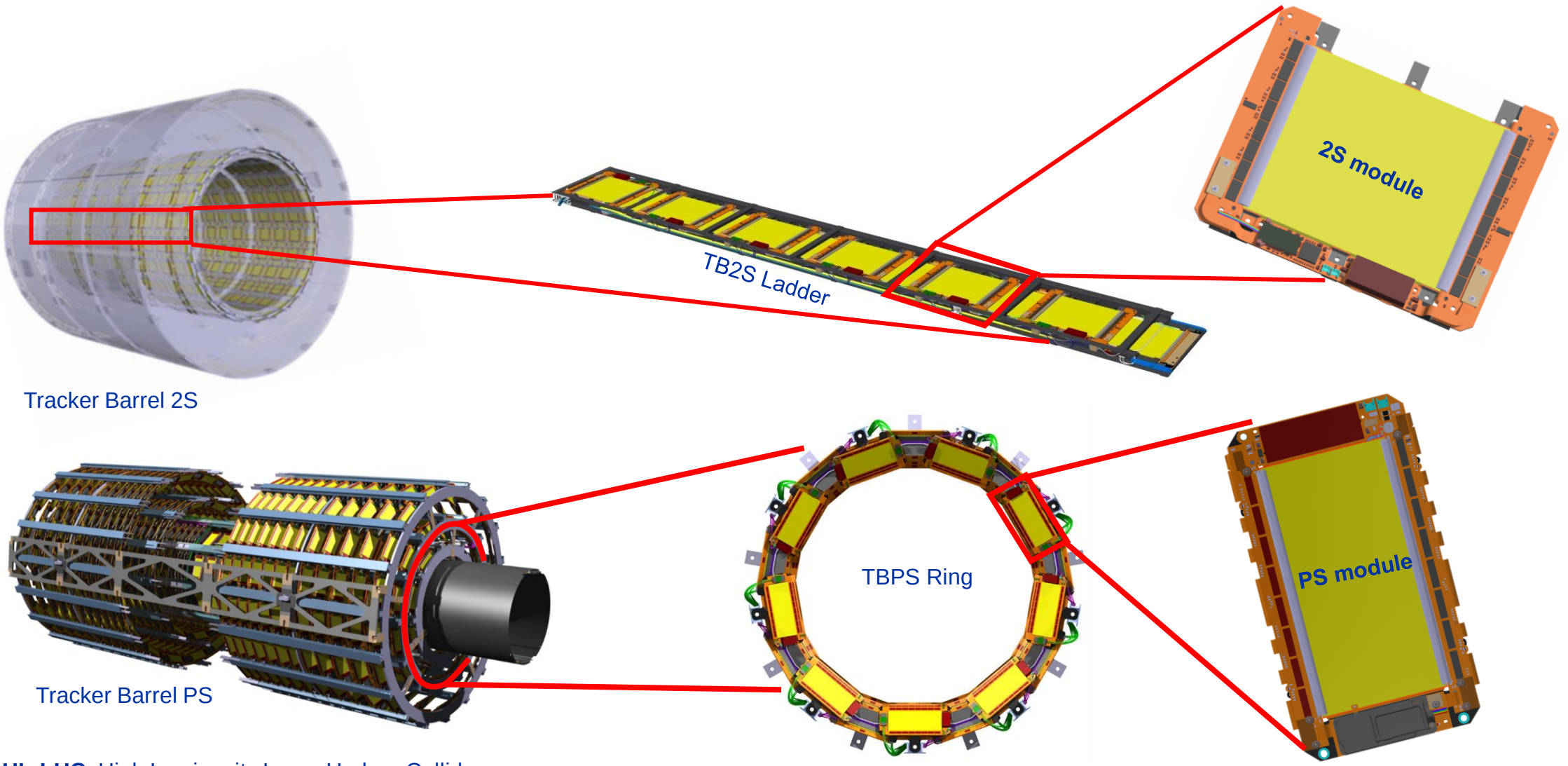
The CMS Outer Tracker Phase-2 Upgrade for the HL-LHC



HL-LHC: High Luminosity Large Hadron Collider;

On-module powering requirements

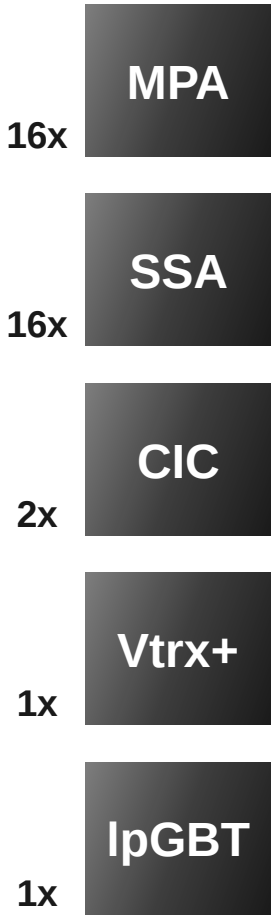
Powering context

Purpose of the powering implementation is to guarantee optimal operation for all the ASICs:

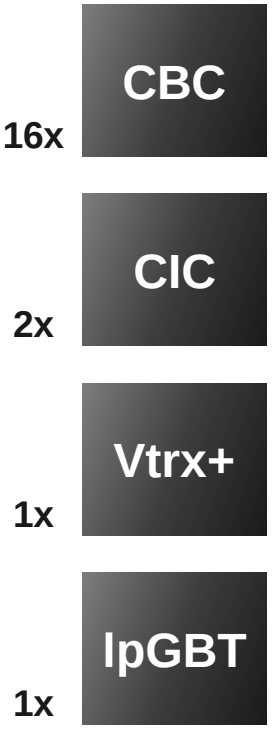
- For the **different consumption conditions**
- For all the **modules built (>13000)**
- For the **detector lifetime** (~10 years)

While minimizing power consumption

PS module ~6.5 W



2S module ~4 W

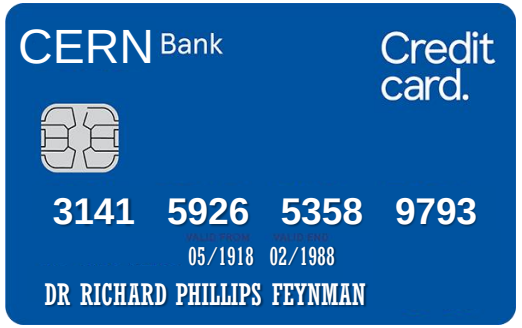


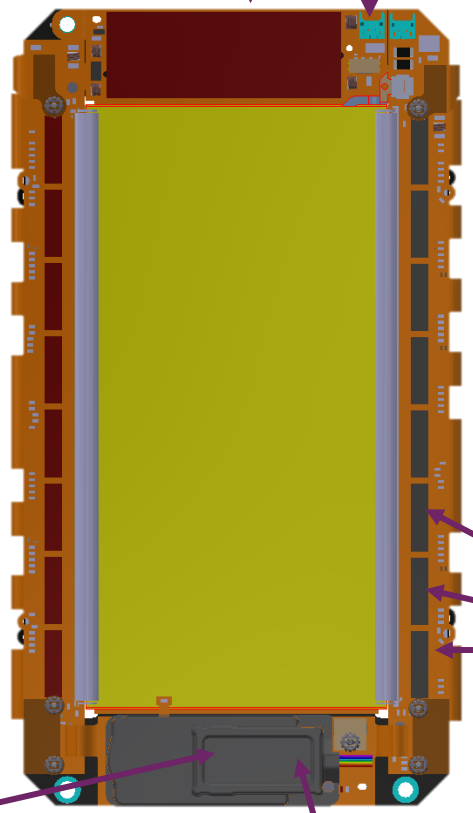
Vtrx+: electro-optical transceiver module
SSA,MPA,CBC: Front-end ASICs
CIC: Data aggregator ASIC

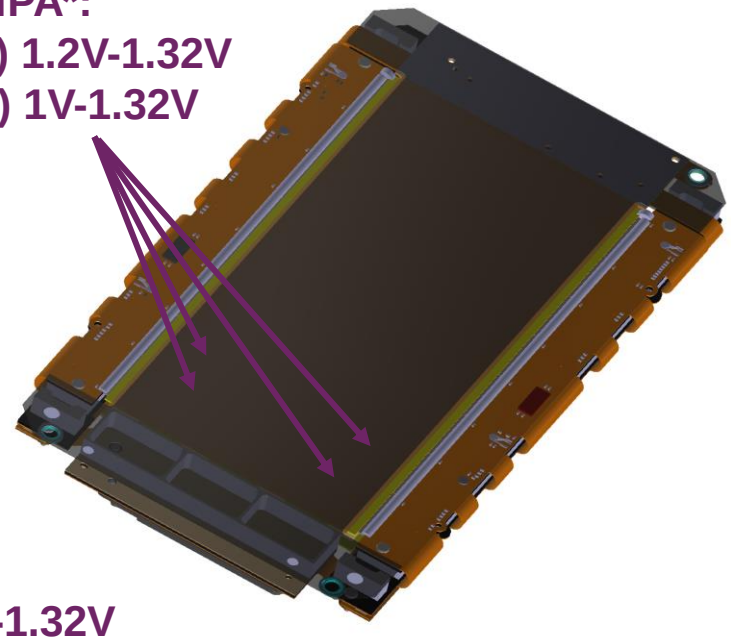
PS module example

- Circuits must be flexible and require very small tracks/copper separation → **small number of thin copper layers**
- ASICs have **tiny operating voltage range** (down to 120mV)

Credit card for scale



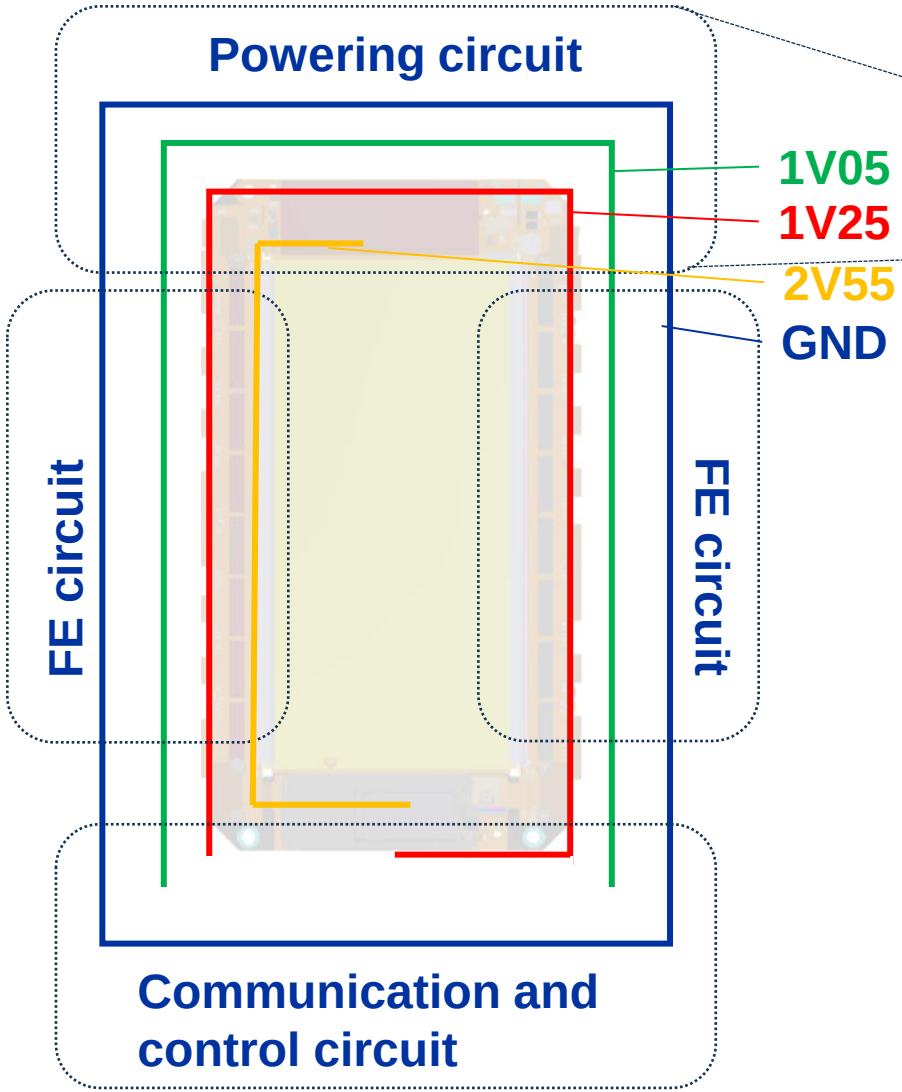


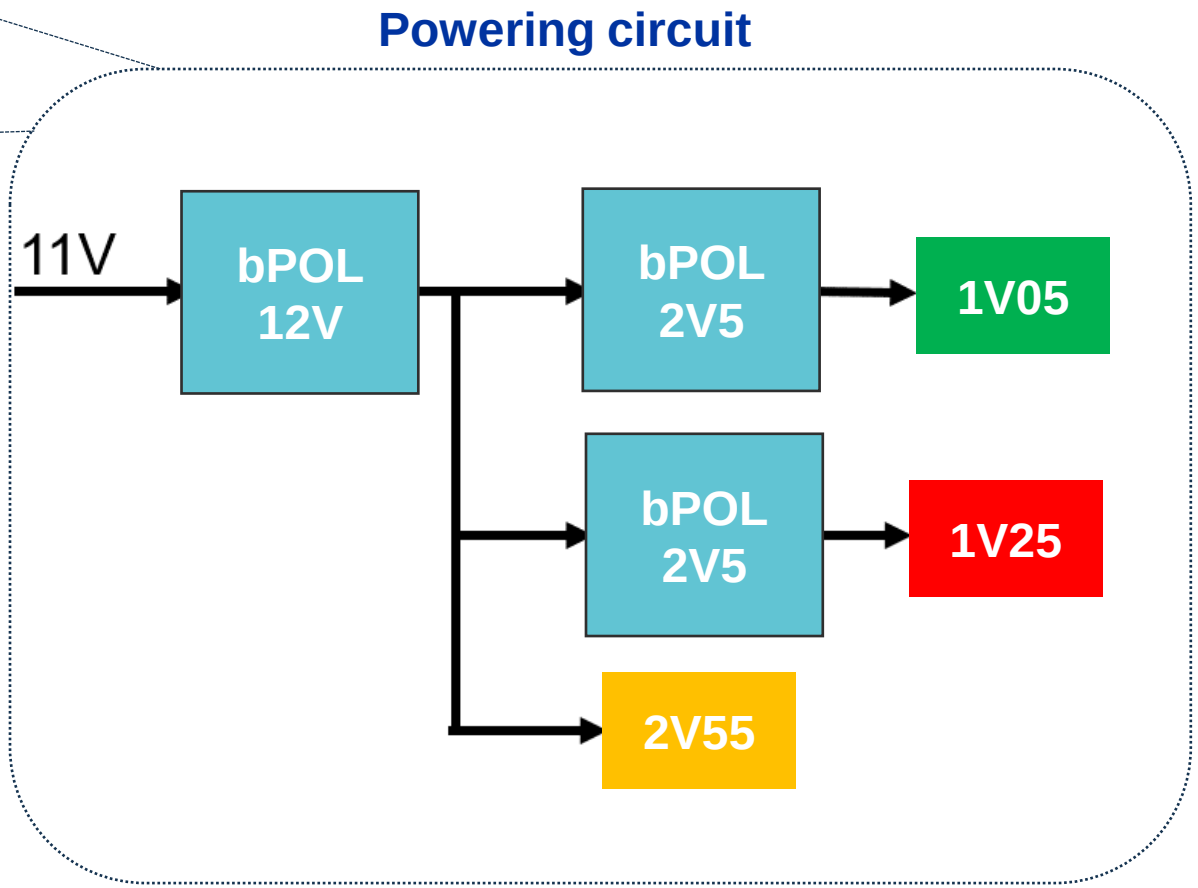


**MPA connected and powered through wire bonds*

Design and evolution

1st Design

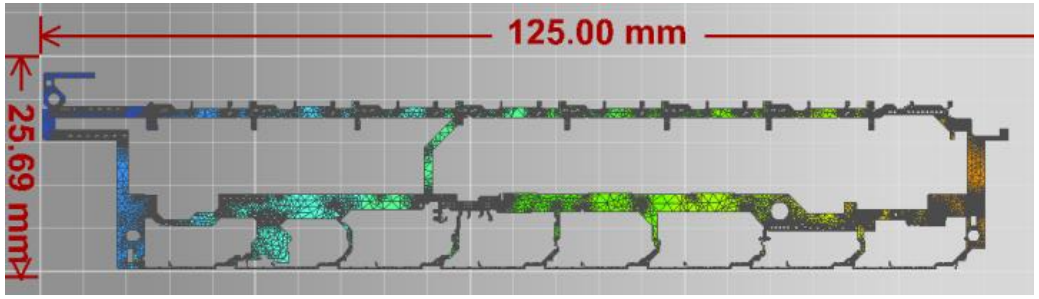




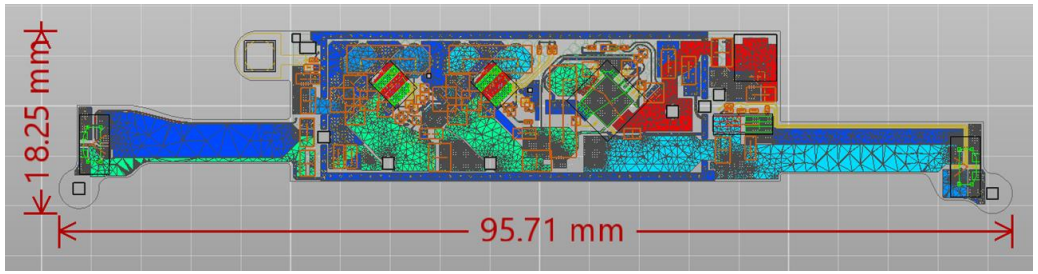
bPOL12: buck converter switching @2.5MHz in QFN32
bPOL2V5: buck converter switching @4MHz bare die

Early prototyping & design evolution

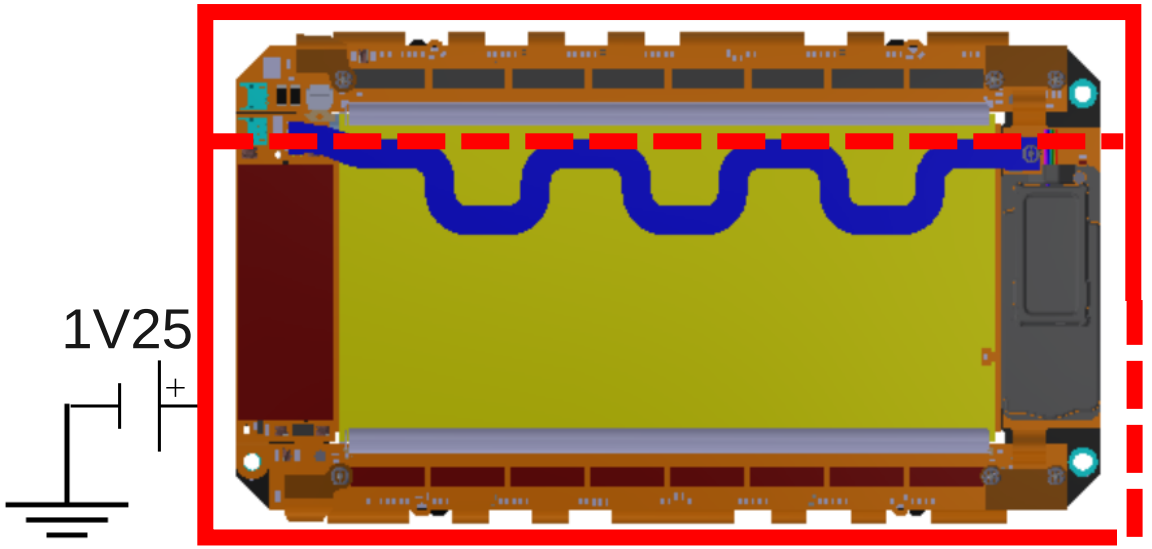
- **Simulations** guide the individual circuit designs (IR drop, current density)
- 1st PS powering circuit prototype → insufficient performance → **re-design** and "**remote sensing**"
- 1V25 seems critical → add **more paths for the currents** to flow



Simulation of the 1V25 rail of an early PS-FEH



Simulation of the IR drops on the TOP copper layer on the final PS-POH

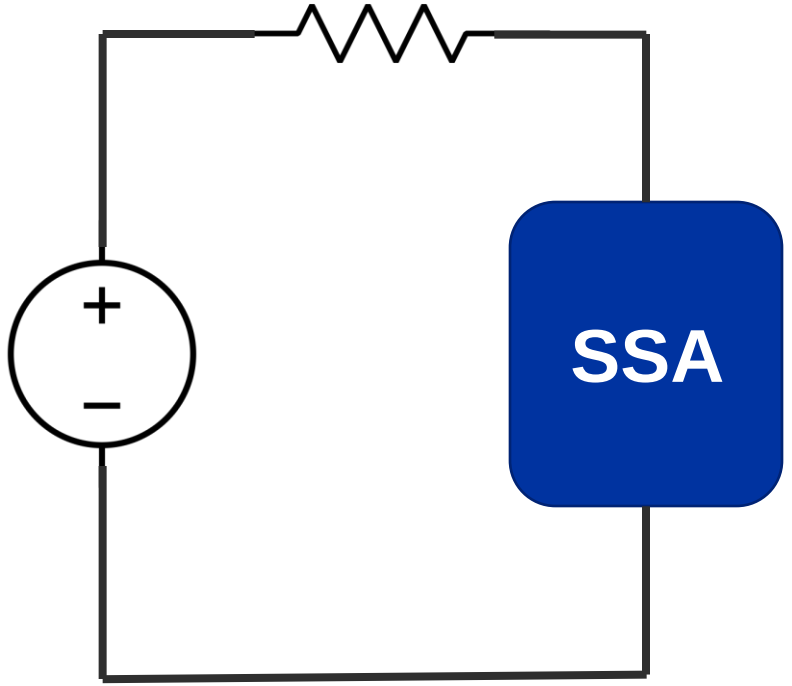


The 1V25 rail in the last prototype PS modules. The dashed lines represent addition of 1V25 distribution compared to original design

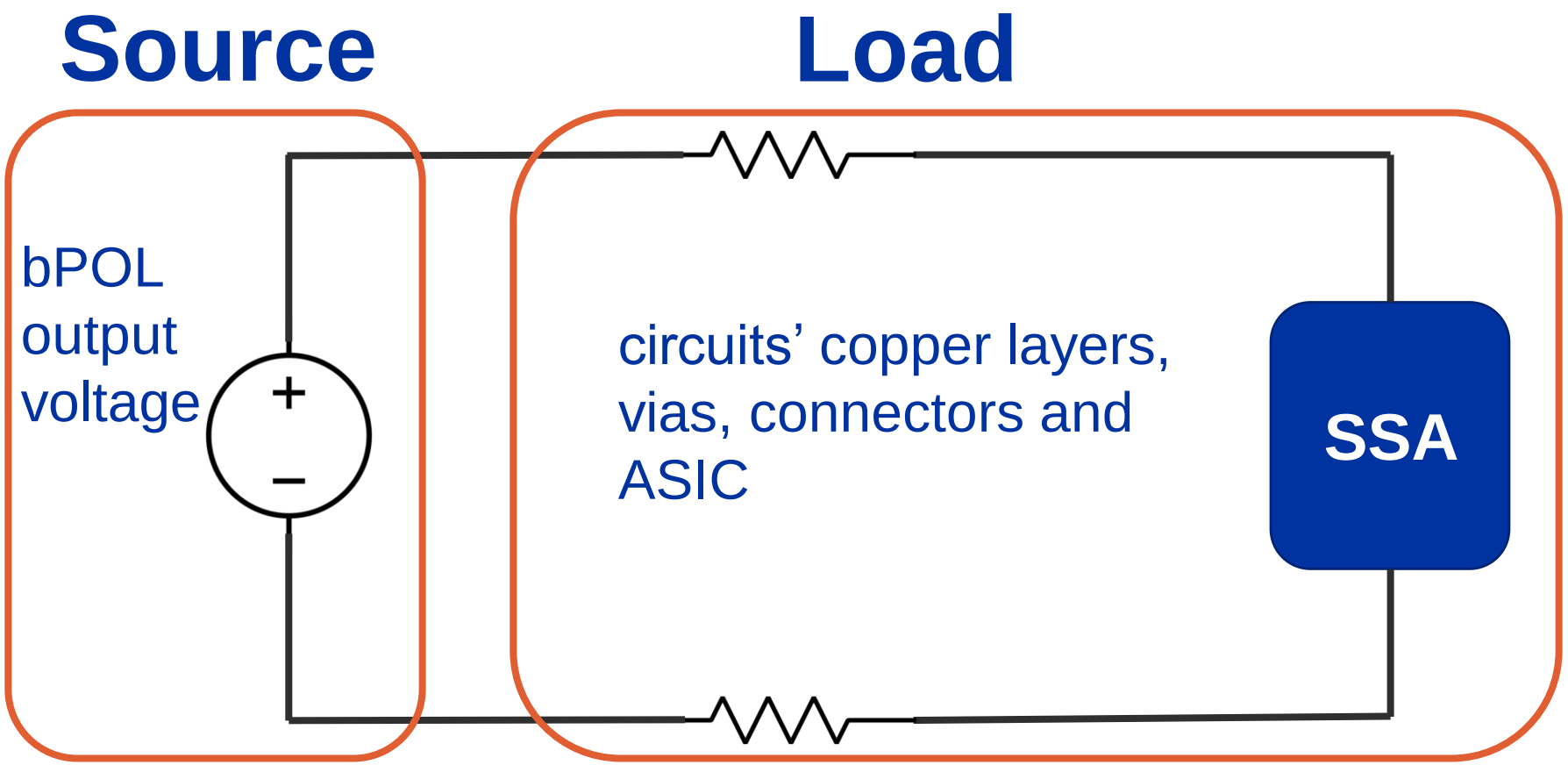
Validation and final powering strategy

Simulated voltage drop $\boldsymbol{V_{drop}}$ @ nominal SSA power

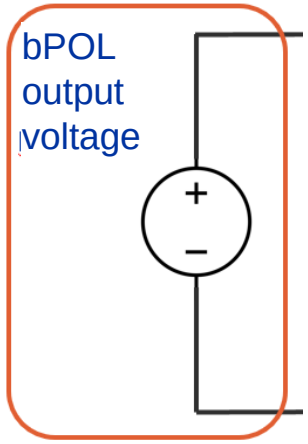
bPOL output voltage $\boldsymbol{V_{OUT}}$



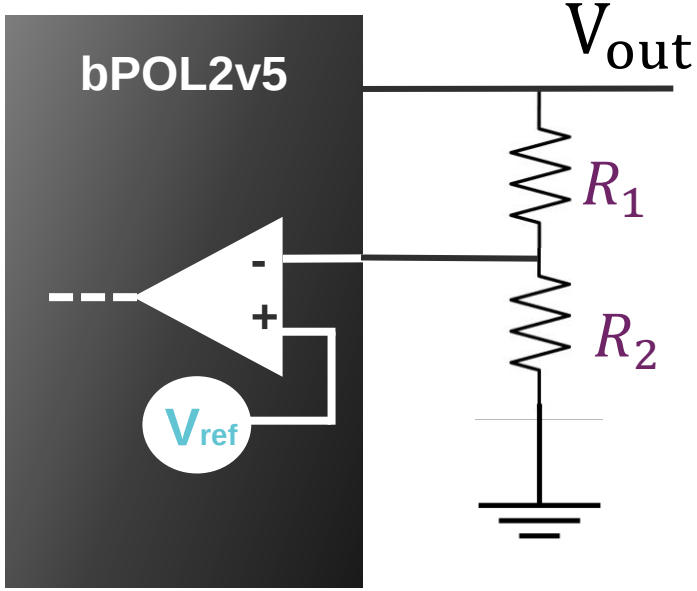
$$V_{out} = minimum\,\text{SSA oper. voltage} + \boldsymbol{V_{drop}} + \boldsymbol{safety}$$


Source
Load
bPOL
output
voltage
+
–
circuits’ copper layers,
vias, connectors and
ASIC
SSA

Effects on the source



$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right)$$



- **Resistor divider**

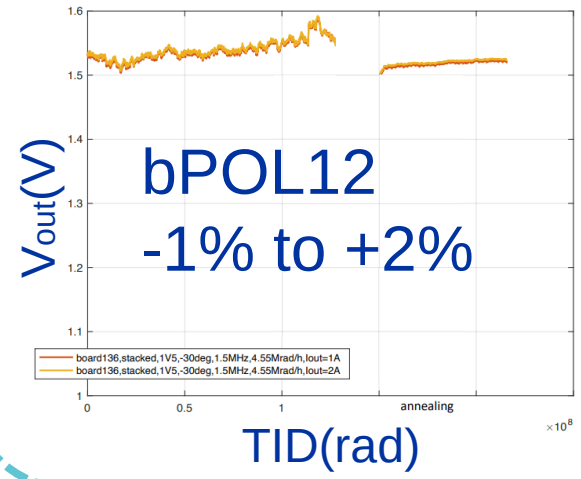
Theoretical computation of effects

$R_{1,2} = R_{1,2}$ (Temperature, irradiation, aging, process variation)

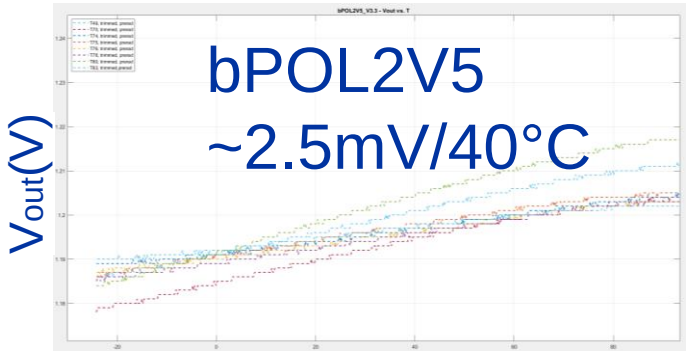
Assuming R1,R2 are from the same resistor family →

$\mathbf{R = R\ (process\ variation)}$

bPOL V_{ref} :TID



bPOL V_{ref} :Temp



bPOL V_{ref} : Process variation/trimming accuracy

bPOL12: $\mathrm{Vref} \sim N(630mV, (7mV)^2)$

bPOL2V5: $Vref = 300mV \pm 1mV$

- **bPOL V_{ref} : aging**

Assumed insignificant

Example source: bPOL2V5

Some effects on output voltage have a rather **complicated form** and have time, location in detector and other dependencies**. Others, not even known** apart from their limits (e.g. resistors)

→ How to deal with this?

<u>First possible solution</u>: “worst” case for everything: e.g. minimum/maximum expected output voltage will occur when we have:

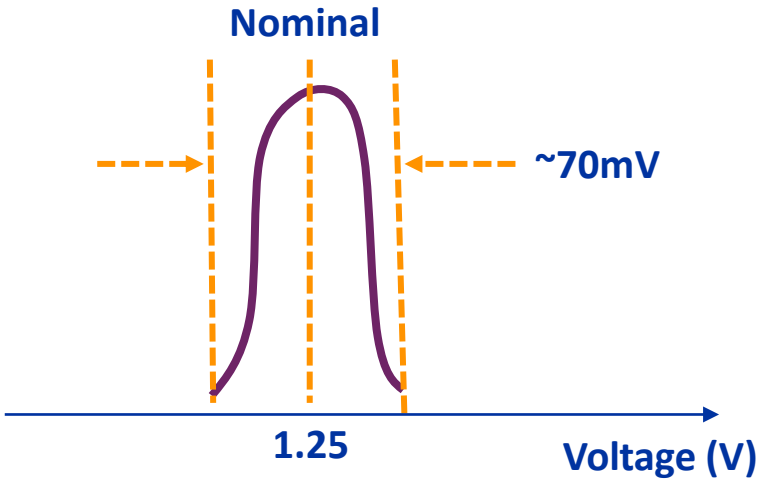
→ worst case TID effect

→ worst case bPOL2V5 trimming

→ worst case resistors

→ worst case temperature

bPOL2V5 V_{out} Distribution (P.D.F.):



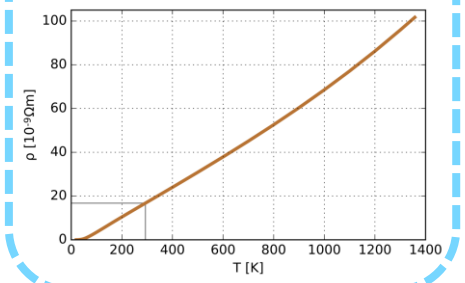
P.D.F: Probability density function

Effects on the load

circuits' copper layers, vias, connectors and ASIC

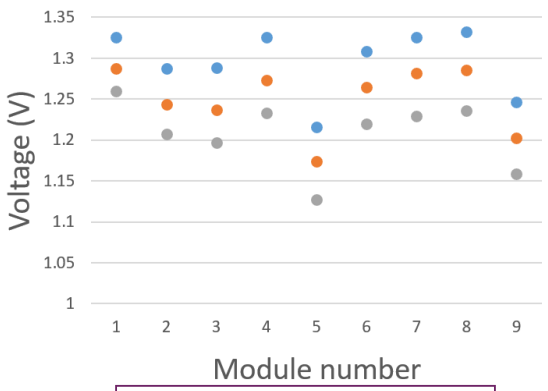
SSA

Copper
~ -20% at 50 degrees colder

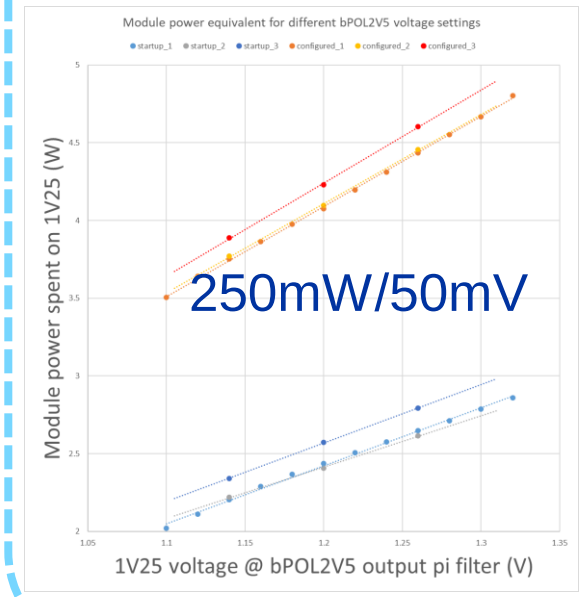


Prototype module data

2S modules: 2S-SEH unloaded and worst location voltage in a module

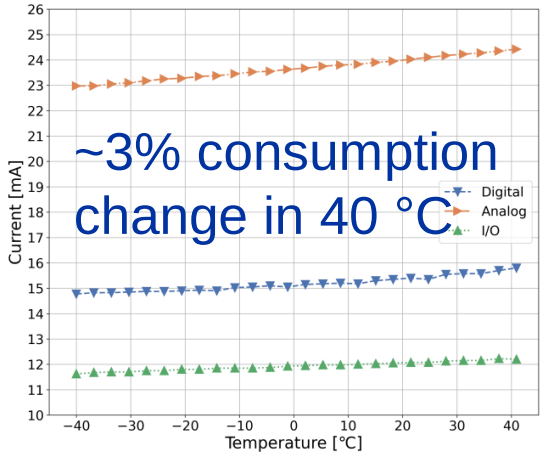


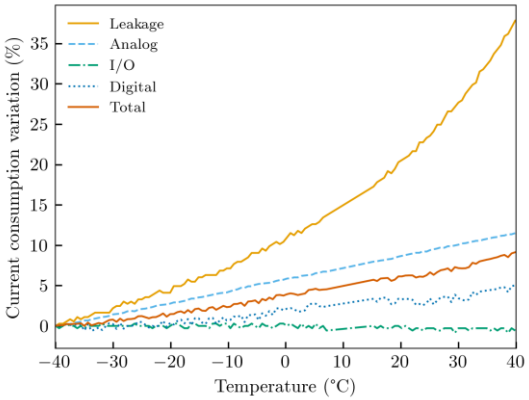
Dedicated powering measurement setups



Single chip tests

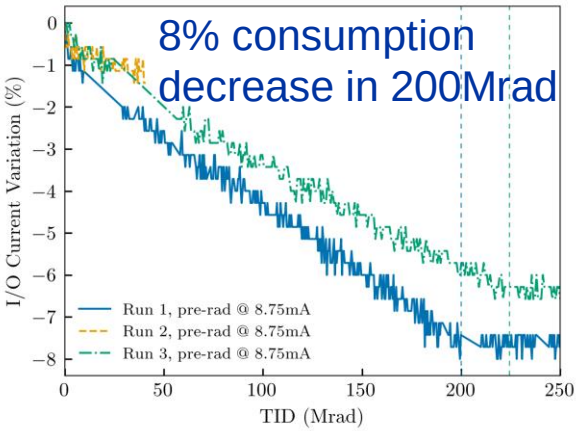
CMS PH2 OT ASICs

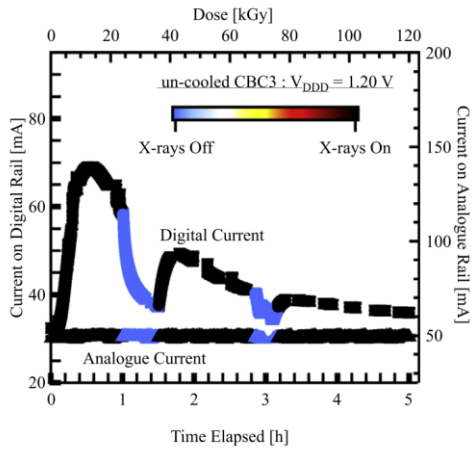




Single chip tests

CMS PH2 OT ASICs





Effects on the load: an example

- **Prototype module data:** drop between powering circuit output and furthest SSA at <u>standardized conditions</u>

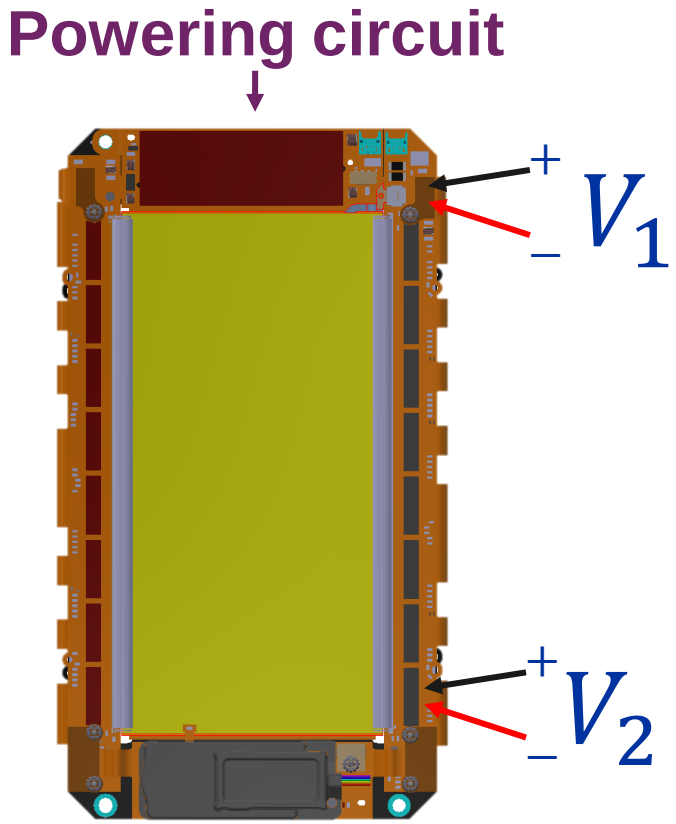
$$\sim N(\mu, (\sigma)^2)$$

With sufficient data points from different prototype modules, the standard deviation **includes effects of**:

- PCB and ASIC process variation varying connector contact resistances etc.
- uncertainty from the measurement itself.

$$\alpha * (\mu - 3 * \sigma) < Vdrop_{SSA} < \beta * (\mu + 3 * \sigma)$$

α,β: ***adjustments*** *for effects of TID, temperature, ASIC version, consumption conditions etc. as* expected from **single chip test results**



$$V_1 - V_2 = Vdrop_{SSA}$$

Verifying powering strategy and V_{OUT} choice

Choose powering circuit nominal V_{OUT} such that:

Min expected Max expected

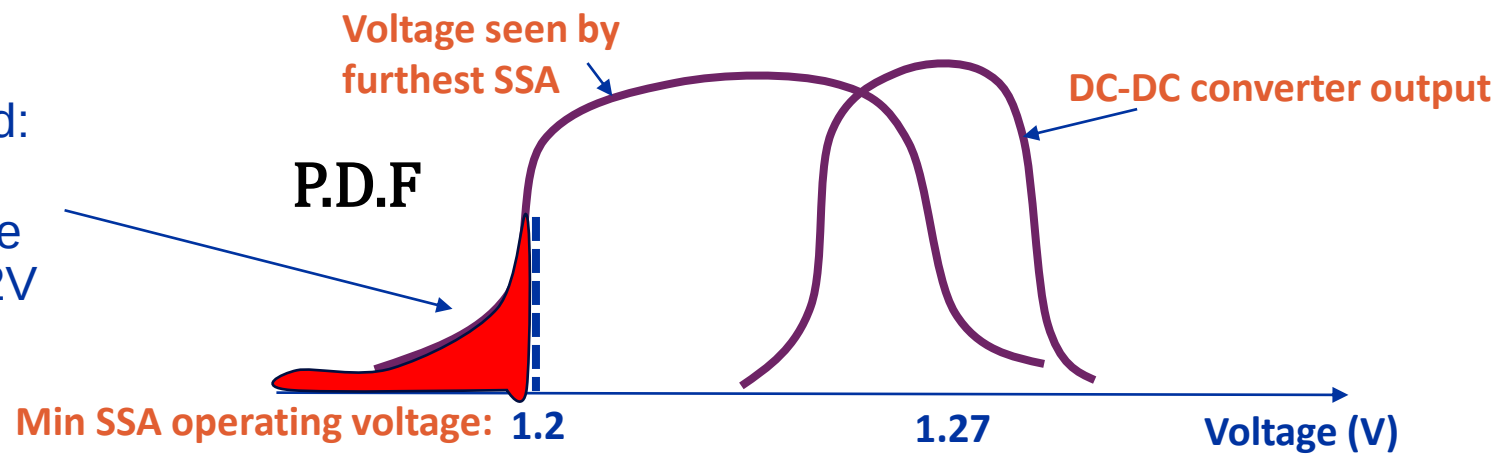
$$V_{OUT} - Vdrop_{SSA} > \text{minimum SSA oper. voltage}$$

Max expected

$$V_{OUT} < \text{maximum SSA oper. voltage}$$

If red area ≠0 no matter the possible nominal V_{OUT} then numerical estimation is required:

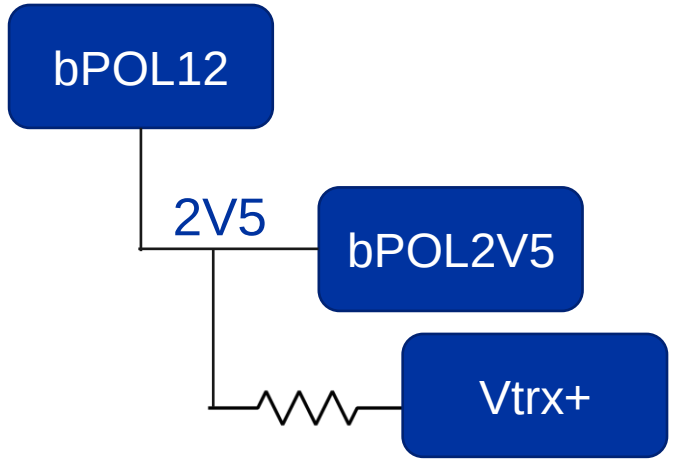
e.g. small chance that 1% of the modules will see lower than 1.2V at some point during operation can be deemed acceptable…

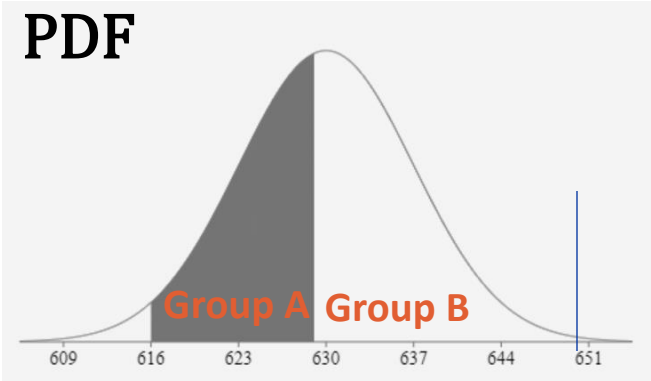


Results of these studies for the CMS OT modules

This study was completed for each supply rail and each ASIC on the two modules:

- We **chose output voltages** that guarantee operation with **minimal power losses**.
- The PS module *definitively* **does <u>not</u> need the zig-zag tail**.
- It's worth to procure **0.1% resistors** for the PS and 2S modules' output voltage setting.
- Finally, noticed an issue with the 2.5V which required further actions :
  - **simulate bpol2v5 operation** on our circuits with **2.7V input** (higher than the specified 2.5V max)
  - bin bpol12: **Split the bPOL12 ASICs** we will use into two groups **based on their Vref**, in order to reduce their expected output spread
  - Consider potential impact on VTRx+ operation below 2.5V





bPOL12 Vref distribution of the prototype bPOL12_V6

Conclusion

Current technology of ASICs and circuits along with other **exotic requirements** for our detectors mean complications in terms of achieving power integrity now and **even more so in the future**.

→ Study the powering early in the (system) design process to avoid surprises

→ Greatly benefit from studying other powering schemes (e.g. serial powering)

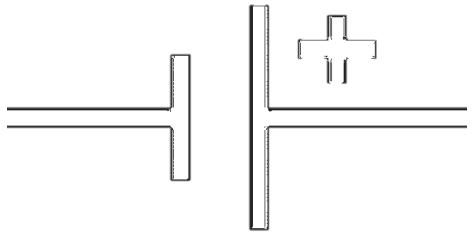
Often, we develop circuits/systems in parallel with ASICs.

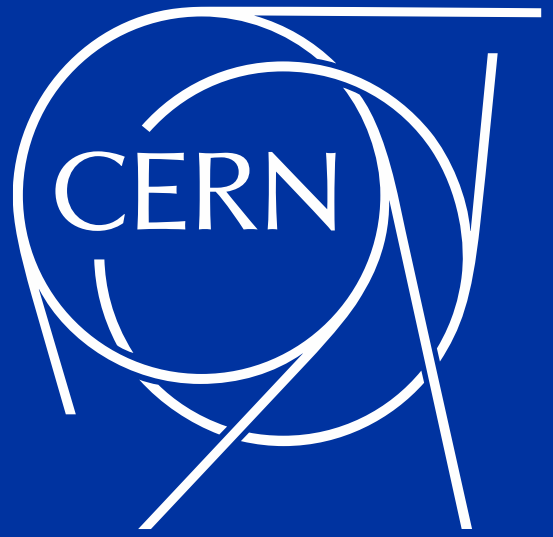
→ Thorough electrical measurements and verification in prototype systems is key (tricky when the usual priority for prototypes is getting data out of them)

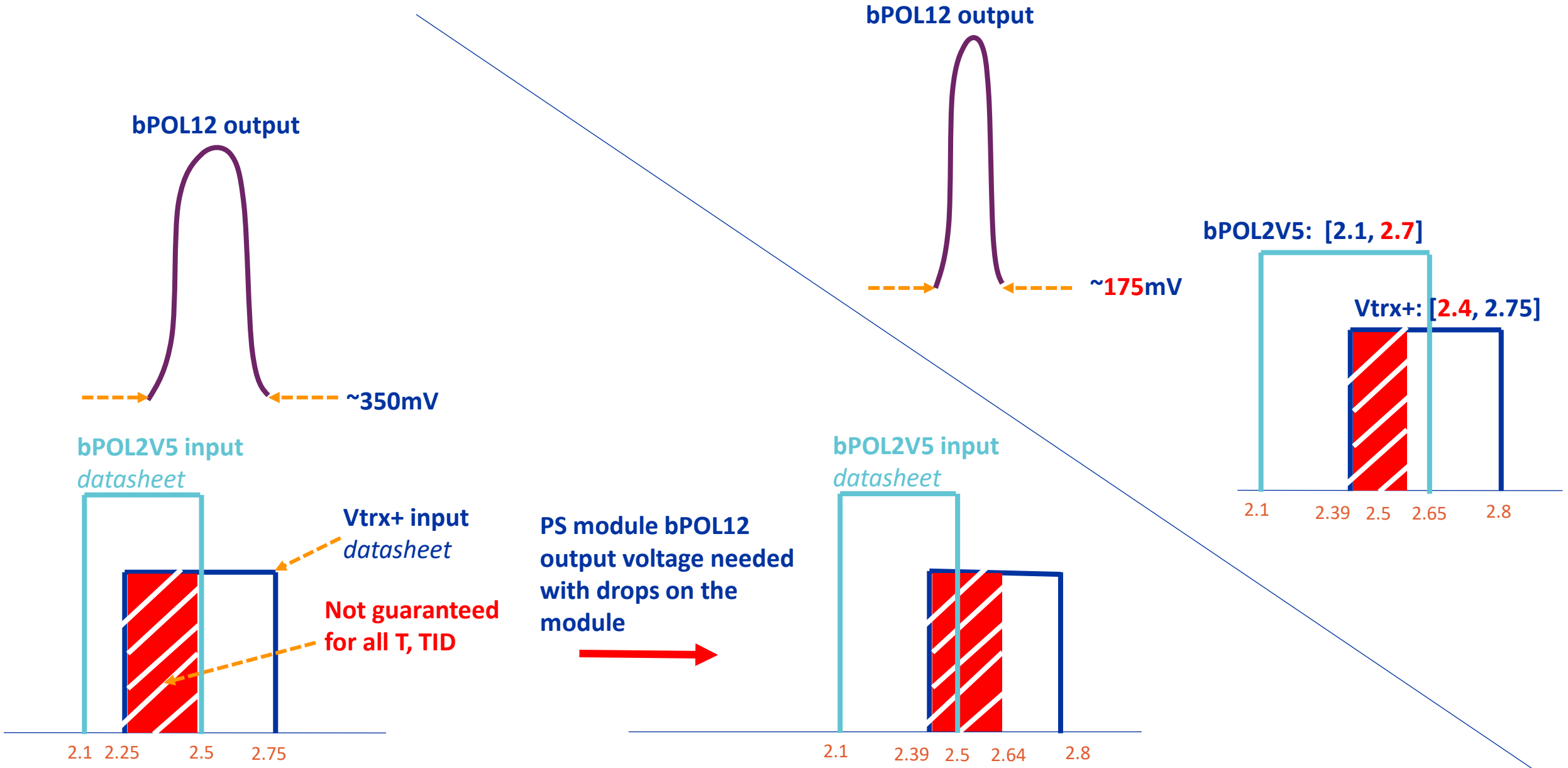
→ASIC qualification (consumption vs TID, temperature..) is crucial. In our case this information existed and was available when it was required

CMS OT circuits now in production. Powering strategy is fixed. ☺

Thank you for your attention
Any questions/comments?




CERN


bPOL12 output
~350mV
bPOL2V5 input
datasheet
Vtrx+ input
datasheet
Not guaranteed
for all T, TID
2.1
2.25
2.5
2.75
PS module bPOL12
output voltage needed
with drops on the
module
bPOL12 output
~175mV
bPOL2V5 input
datasheet
2.1
2.39
2.5
2.64
2.8
bPOL2V5: [2.1, 2.7]
Vtrx+: [2.4, 2.75]
2.1
2.39
2.5
2.65
2.8