Hybrid designs and kick-off production experience for the CMS Phase-2 Upgrade

A PS-FEH-L16 kick-off hybrid

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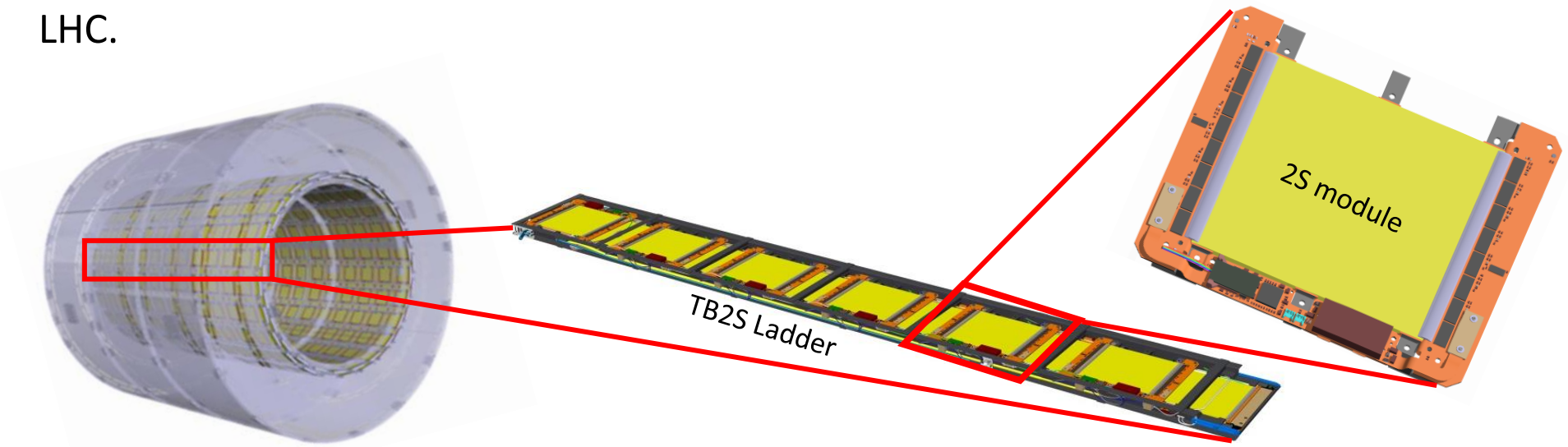
Outline:

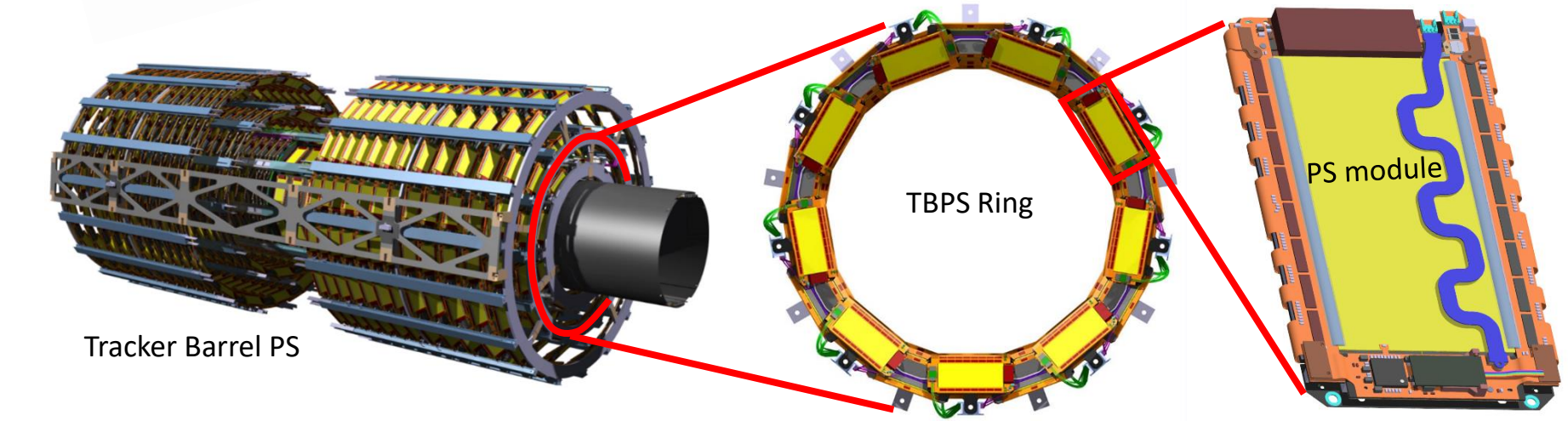
1. Introduction of CMS Phase-2 upgrade and the procurement of hybrids
2. Introduction of the front-end hybrid concepts, architecture and design practices
3. Kick-off hybrid designs and test results
4. Quality issues, lessons learnt and yield
5. Conclusion

Hybrid circuit: Unpackaged dies are mounted on a substrate with passive components.

CMS: Compact Muon Solenoid; **PS**: Pixel-Strip type module; **PS-FEH-L16**: PS Front End Hybrid, left 1.6 mm spacing

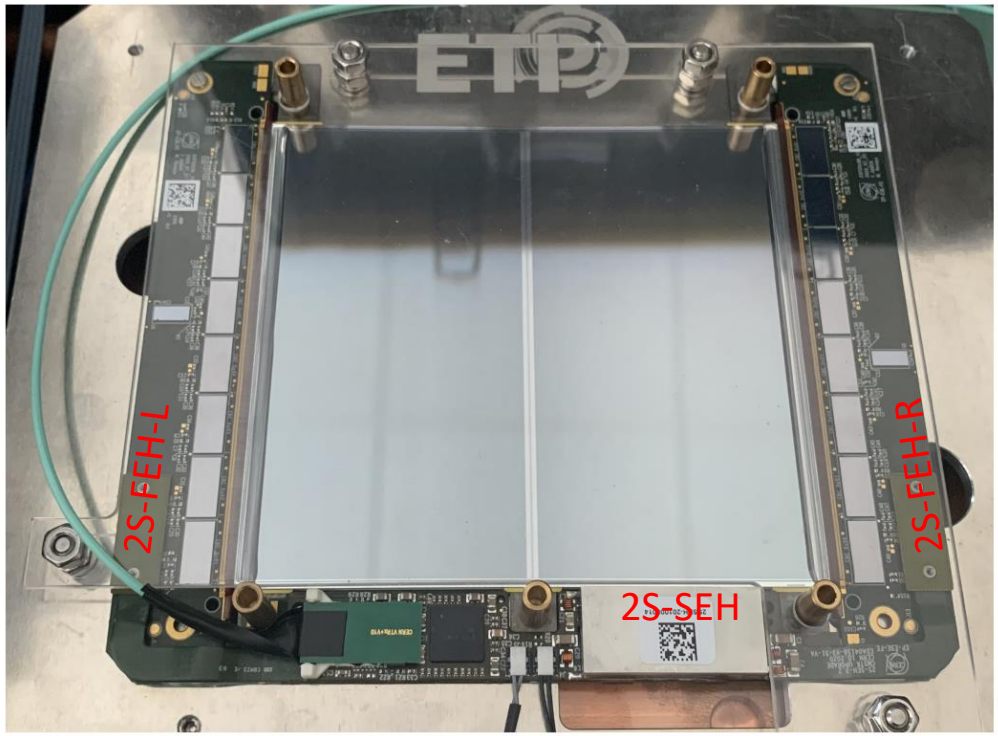
The CMS Tracker Phase-2 Upgrade is required to adapt the CMS detector to the 3000 fb^{-1} total integrated luminosity and 14 TeV centre-of-mass energy of the HL-LHC.



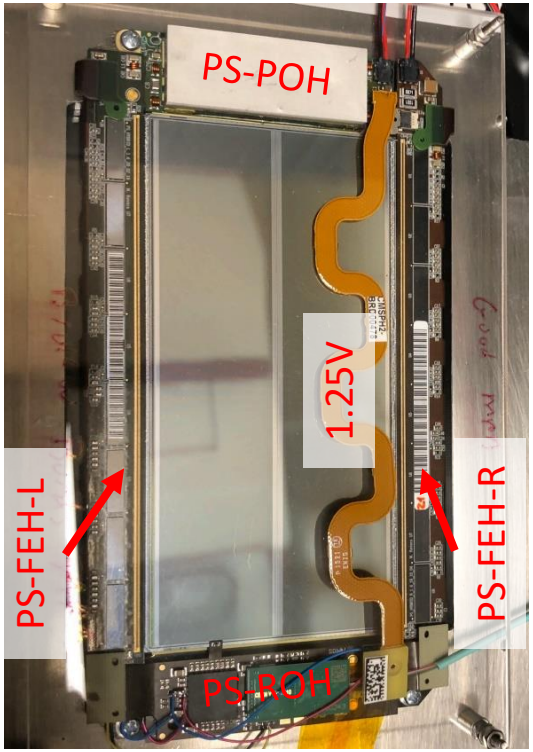


HL-LHC: High Luminosity Large Hadron Collider; **TB** – Tracker Barrel; **2S** – Strip-strip module; **PS** – Pixel-Strip module

Sensor module prototypes are assembled from multiple pieces, including hybrids, sensors, spacers and stiffeners. Modules from kick-off hybrids are currently under construction.



A Strip-Strip (2S) module prototype constructed from the latest hybrid prototypes.

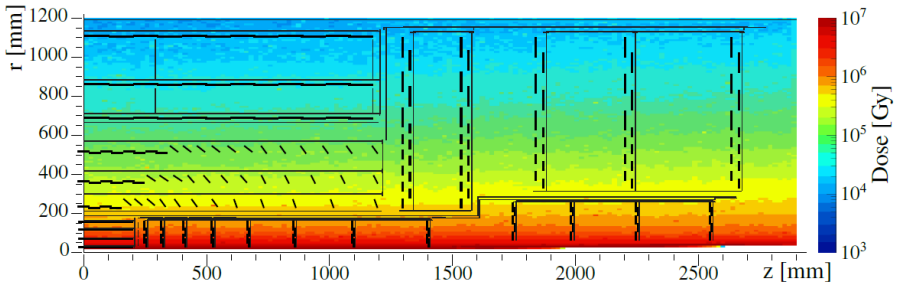


A Pixel-Strip (PS) module prototype constructed from the latest hybrid prototypes.

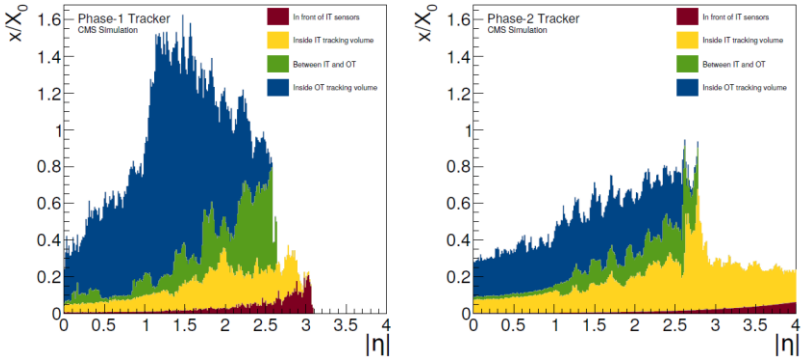
SEH: Service Hybrid; **ROH** – Read-Out Hybrid; **POH** – Power Hybrid; **FEH** – Front-End Hybrid

The requirements for the electronics are the following:

- Tolerate radiation (max. 56 and 9 Mrad expected for PS and 2S respectively [1]).
- Reduce mass and size as much as possible.
- Operation in cold, minimize heat transfer to sensors.
- Reliable operation for 15 years.
- Low power consumption (~5.4W per 2S module; 7.8W per PS module[1]).
- Total number of modules planned: 2S: 9140; PS: 6730;



Expected radiation levels in the CMS Ph-2 tracker [1]



Estimated material in the upgraded CMS tracker [1]

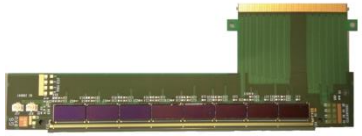
[1]: The Phase-2 Upgrade of the CMS Tracker Technical Design Report CMS-TDR-17-001

The hybrid development is a long story:

2013 — **Market survey preparation**

2CBC2 hybrid with rigid 6 layers substrate

2013 - 2016 — **Prototype development**



8CBC2 hybrid with CF stiffener glued with double-sided adhesive

2017 - 2020 — **Hybrid Industrialization**

8CBC3 hybrid + CIC mezzanine with CF stiffened 4 layers flex and compensator

2020 - 2022 — **Invitation to tender**

2S-FEH-L with CF stiffened 4 layers flex and compensator, final geometry

2023 - 2024 — **Ramp-up production**

2S-FEH-L with CF stiffened 4 layers flex and improved alignment for series production

Verification of design modifications, pilot manufacturing
Lots delivered in 2023

Kick-off

Today we are here

Verification of manufacturing processes, fine tuning.
Lots will be delivered in 2024
~500 pcs/month

Pre-series

High rate production, continuous observation of quality.
Starts by end of 2024
~2000 pcs/month

Mass production

PS family kick-off hybrids

2 x 15 pcs of PS power hybrid (PS-POH)

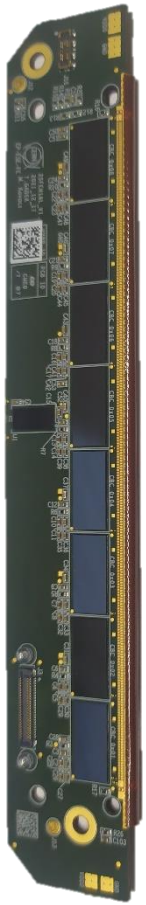
30 pcs of PS readout hybrid (PS-ROH)

30 pcs of PS front-end hybrid left (PS-FEH-L)

30 pcs of PS front-end hybrid right (PS-FEH-R)

2S family kick-off hybrids

2 x 15 pcs of 2S service hybrid (2S-SEH)

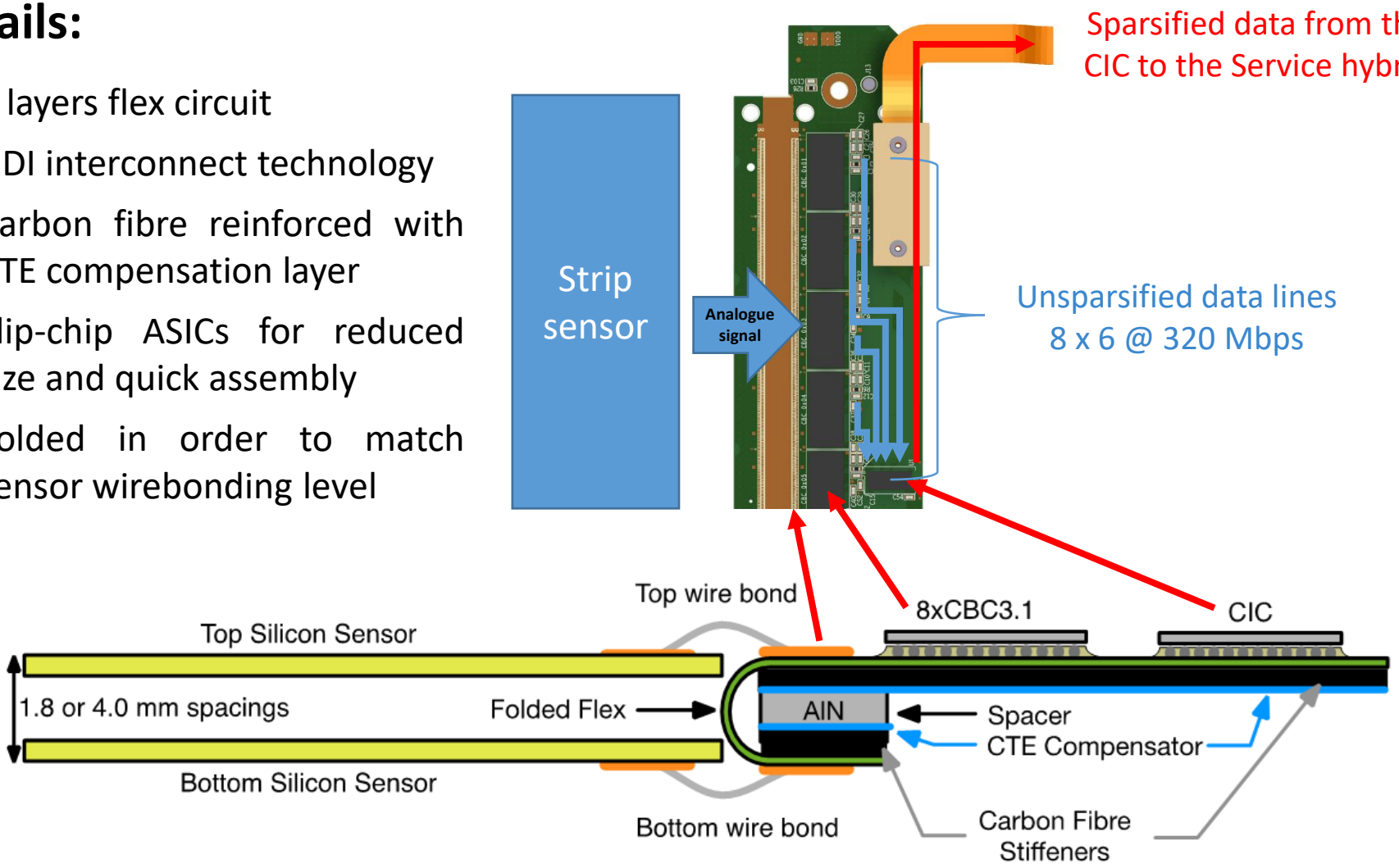


30 pcs of 2S front-end hybrids left (2S-FEH-L)

30 pcs of 2S front-end hybrids right (2S-FEH-R)

Details:

- 4 layers flex circuit
- HDI interconnect technology
- Carbon fibre reinforced with CTE compensation layer
- Flip-chip ASICs for reduced size and quick assembly
- Folded in order to match sensor wirebonding level

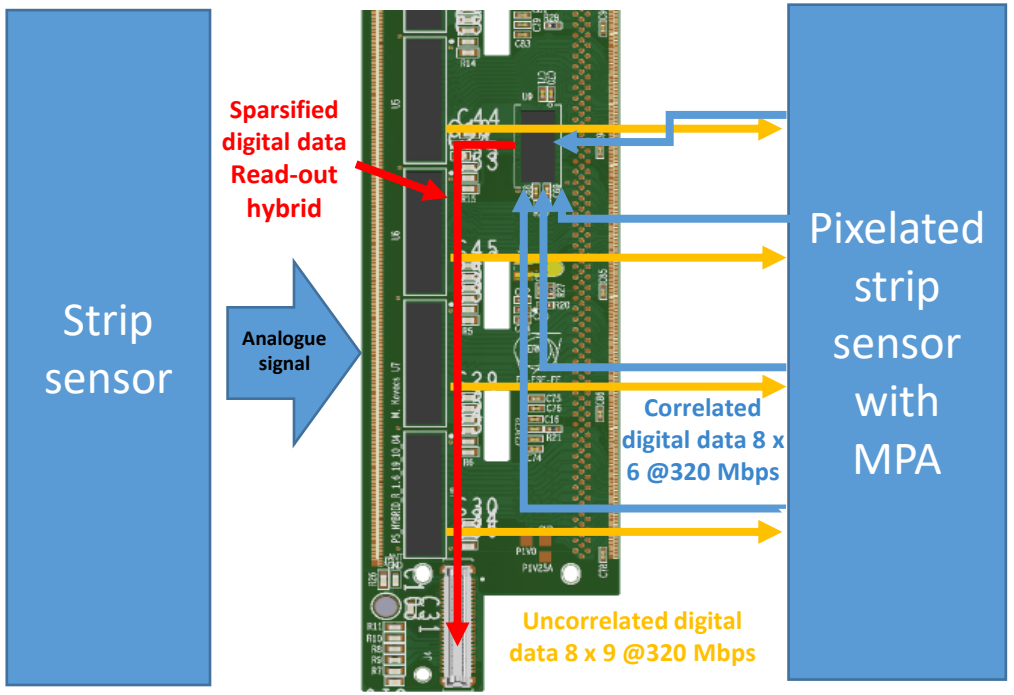


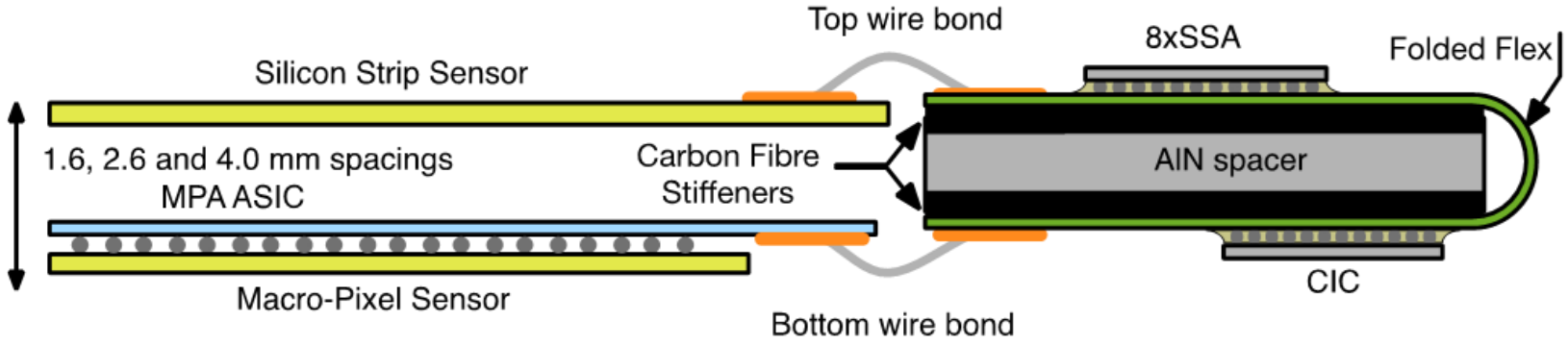
Cross section view of the 2S front-end hybrid construction in a module

HDI – High Density Interconnect; **CTE** – Thermal Expansion Coefficient; **CIC** – Concentrator ASIC;

Details:

- 5 layers HDI flex
- Circuit area is smaller than for the 2S hybrids
- No compensator is needed as the circuit is symmetric
- Smallest line and spacing is 45/45 µm respectively
- Very thin build-up, 125 µm total



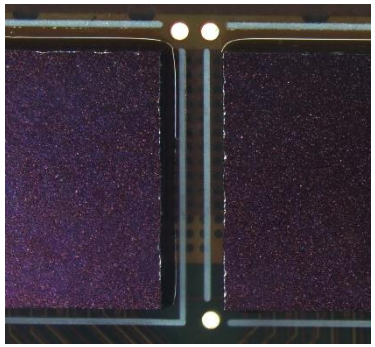


Cross section view of the PS front-end hybrids construction in a module

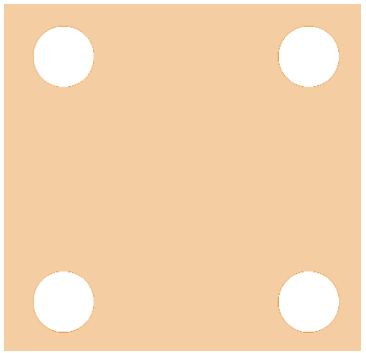
ALN – Aluminium-Nitride a ceramic compound; **MPA** – Macro Pixel ASIC; **SSA** – Short Strip ASIC;

Few important HDI design practices for flex circuits:

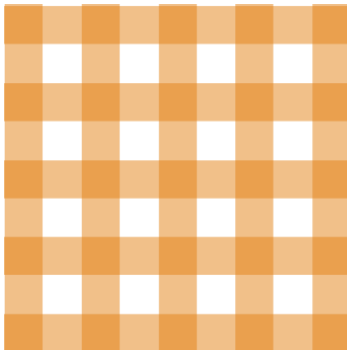
- Use crosshatched copper pattern to improve flexibility.
- Use “teardrops” at trace to pad connections to increase reliability.
- Avoid stacked µvias to further increase reliability.
- Balance copper area to achieve a flat surface, fill unused areas.
- Use “vent holes” to speed-up circuit drying process.
- Use silkscreen or solder mask barriers to control underfill flow.
- Use simulation tools with small size conductors to estimate impedance.



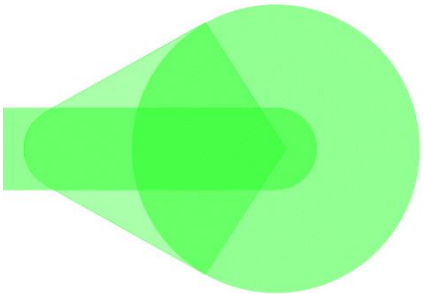
Underfill “barrier”



“vent holes” placed every mm



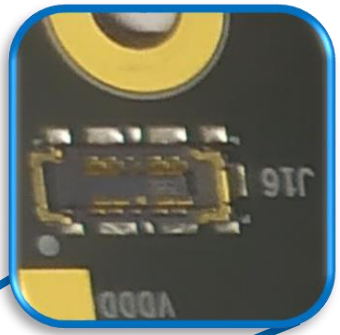
X-hatch can improve flexibility



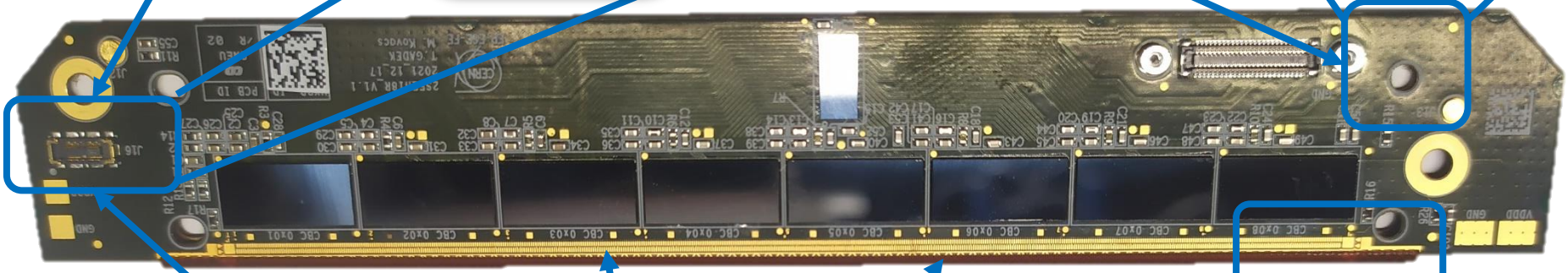
Teardrop will decrease stress

3. 2S-FEH kick-off design - test results

Additional GND interconnection connector for noise reduction ✓



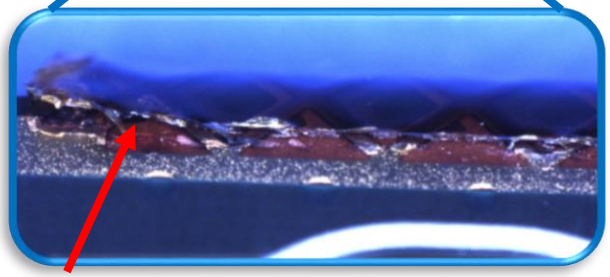
Additional lamination tooling hole to improve assembly tooling holes cleanliness ✓



This additional GND interconnection circuit can improve noise performance by 10 – 15 %

Circuit size is compensated by 0.1% before manufacturing to meet final size criterion

In this circuit, the coverlay protects a GND mesh that is not critical in case of damage

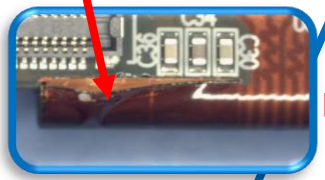


Minor delamination, flaking at milling line

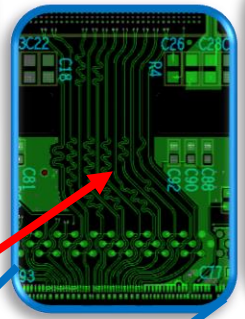
4. PS-FEH kick-off design - test results

Risk of damage

Coverlay coverage was increased to prevent delamination.

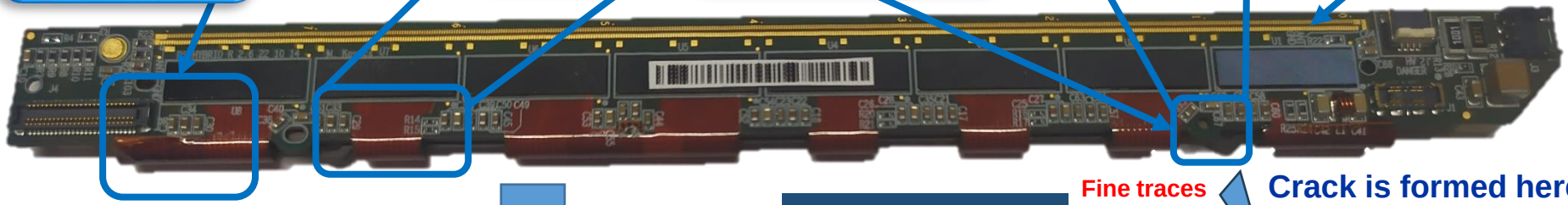


Fine traces protected by coverlay



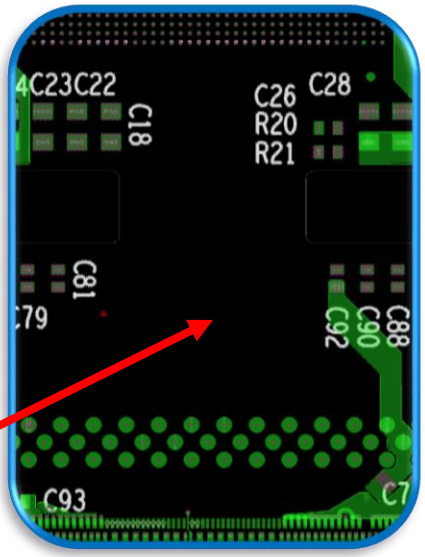
New alignment procedure was developed for improved tooling hole cleanliness and stiffener alignment. Dedicated tools for lamination. ✓

Circuit size is compensated by 0.1% before manufacturing to meet final size criterion

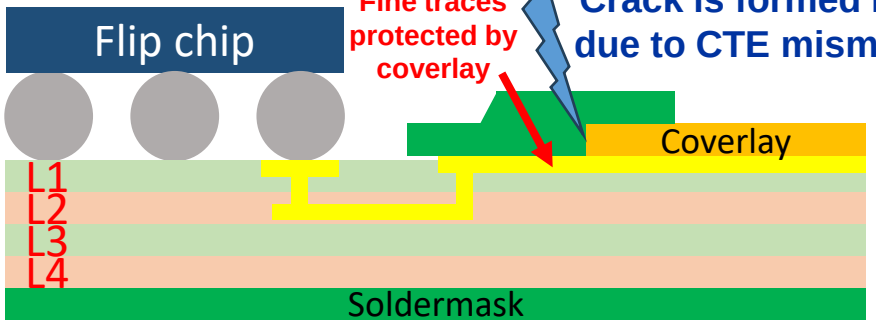


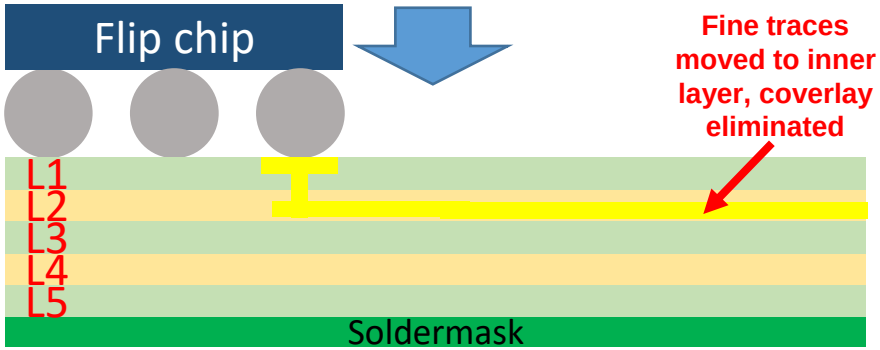
New design solution was needed urgently

Add one more layer to the circuits and eliminate fine traces from the top layer in fold region.



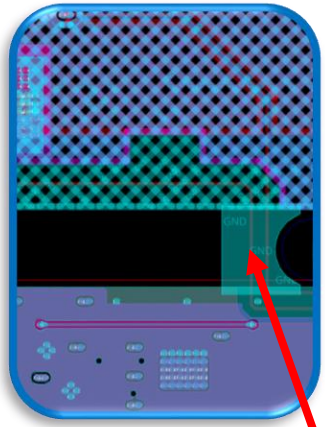
Fine traces are in inner layer

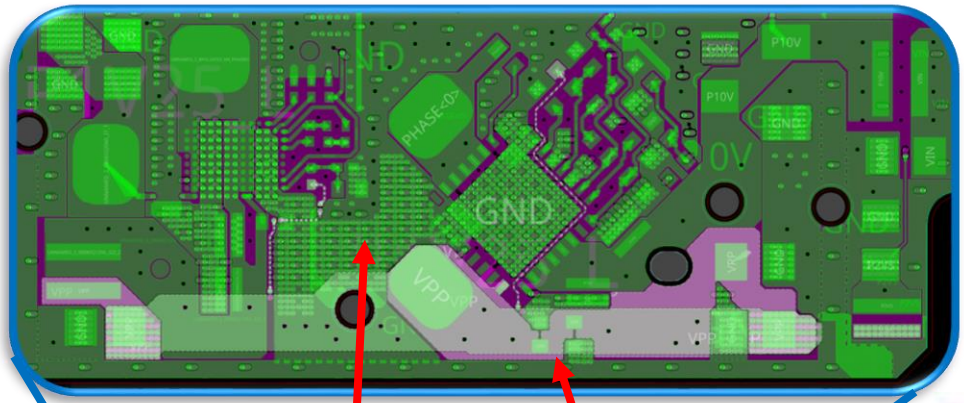




4. 2S-SEH kick-off design - test results

Module tests revealed that the baseline noise is slightly higher than desired. Various layout improvements were made and two GND schemes: split plane and regular.

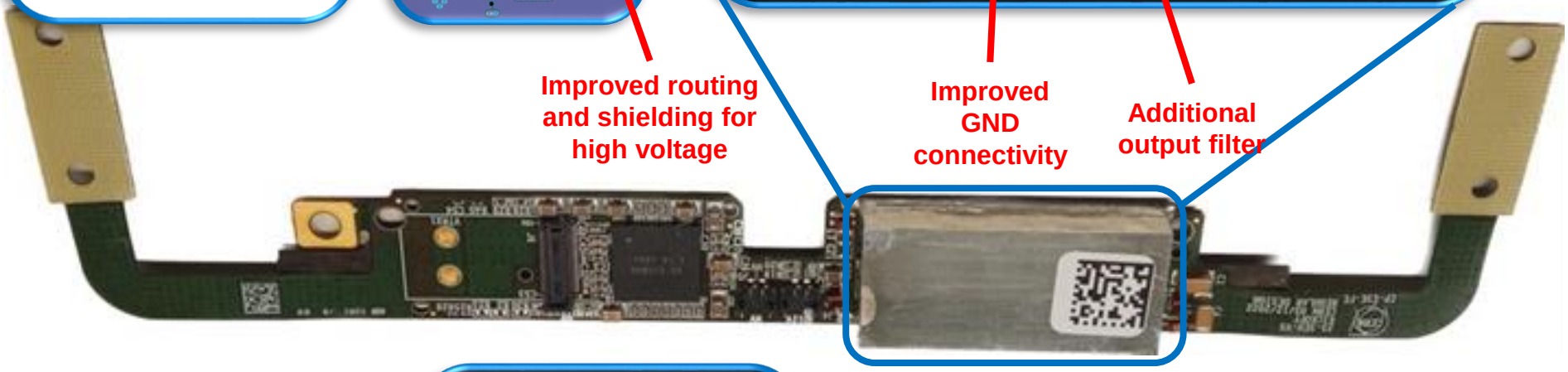




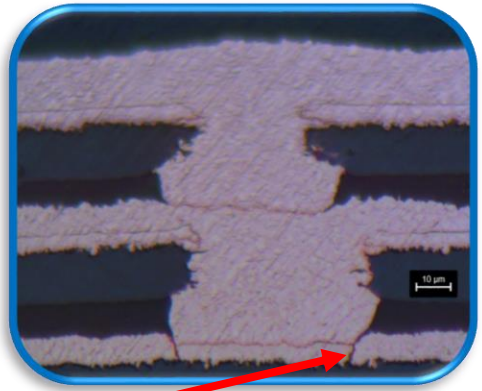
Improved routing and shielding for high voltage

Improved GND connectivity

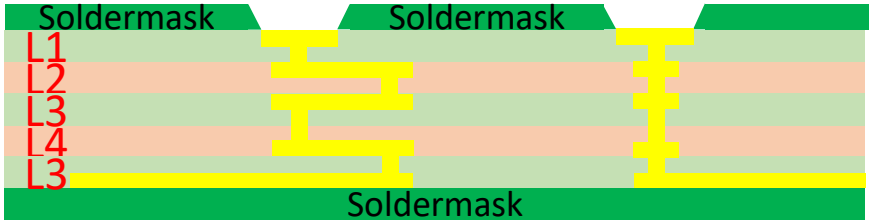
Additional output filter



Previous design had reliability issues related to stacked vias. The 2S-SEH was redesigned with staggered vias to improve reliability.



Via corner crack in SEH

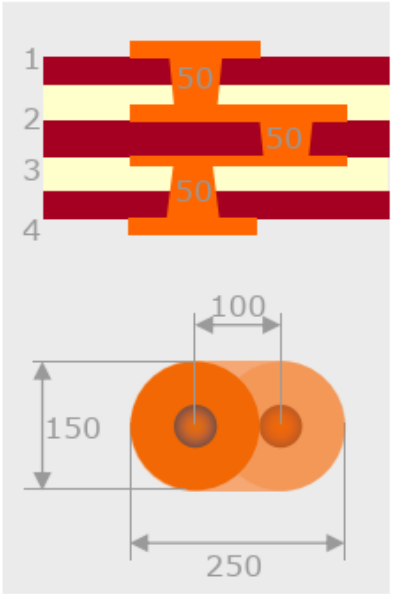
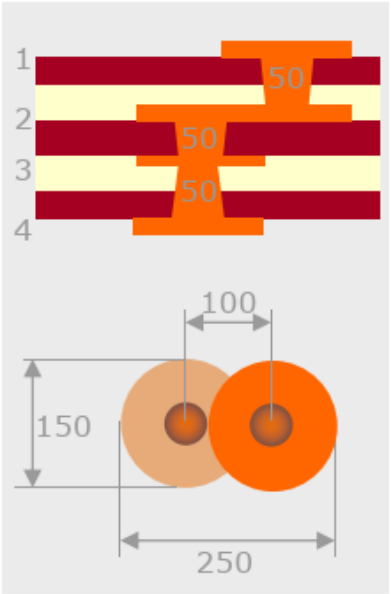
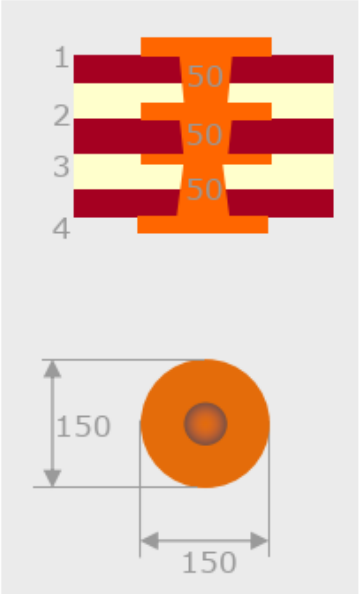


Staggered via structure

Stacked via structure

Via barrel thermal expansion is significantly reduced in staggered structure.

4. Reliability of stacked vs staggered microvias

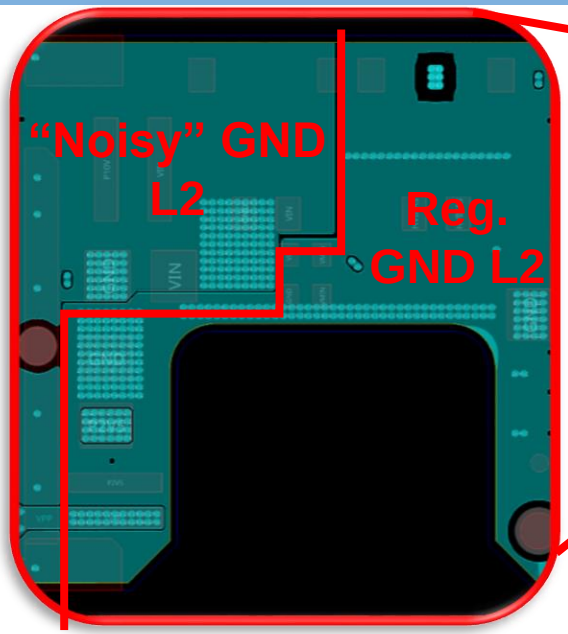
Description	Flex stacked BV +100 µm de-stacking	Flex stacked BV +100 µm de-stacking	Flex stacked BV
Picture			
Pad size layer 1	150	150	150
BV 1-2	50	50	50
Pad size layer 2	150x250 oval	150x250 oval	150
BV 2-3	50	50	50
Pad size layer 3	150x250 oval	150	150
BV 3-4	50	50	50
Pad size layer 4	150	150	150
De-stacking	100	100	100
IST cycles average	**>1000 cycles**	**~130 cycles**	**~40 cycles**

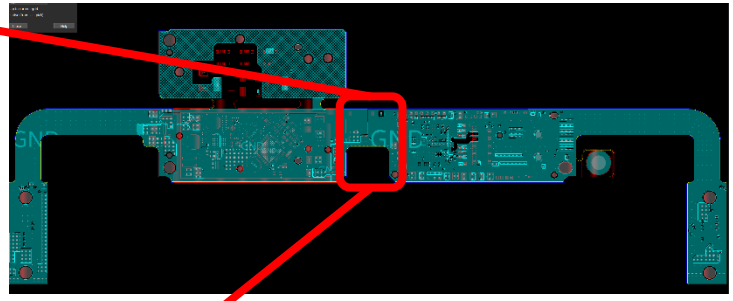
IST: Interconnect Stress Test

Source: Design guidelines – Dyconex AG. IST cycles according to IPC-TM-650 2.6.26 @ maximum temperature of 210 °C

4. 2S-SEH and PS-POH split-plane and regular designs comparison

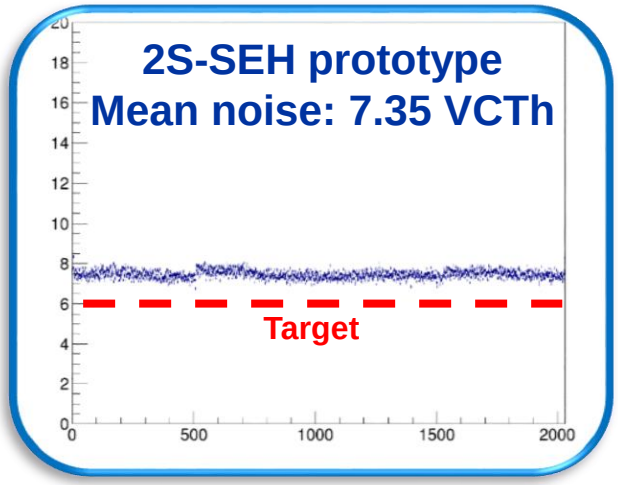
On top of the standard design improvements two design variants were made for the PS-POH and 2S-SEH: Split-plane and regular. Preliminary test results show significantly more noise with the split plane design.

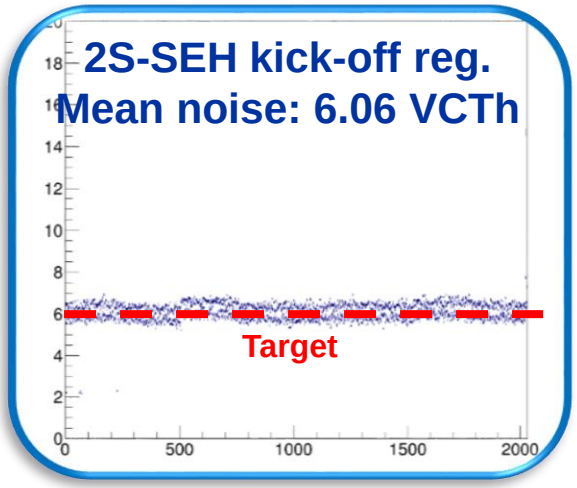


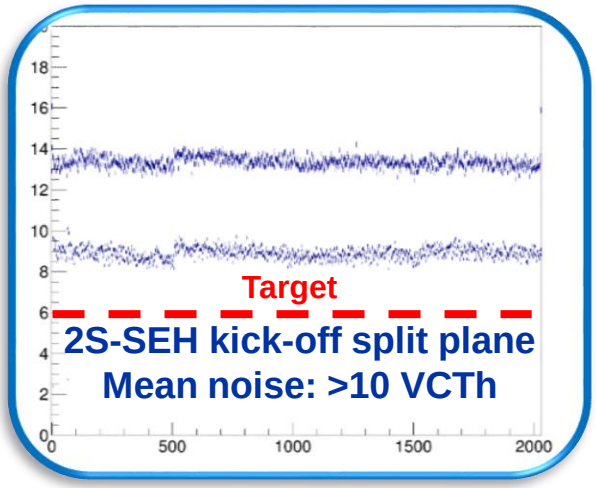


2S-SEH split-plane design

Preliminary results are similar with the PS-POH



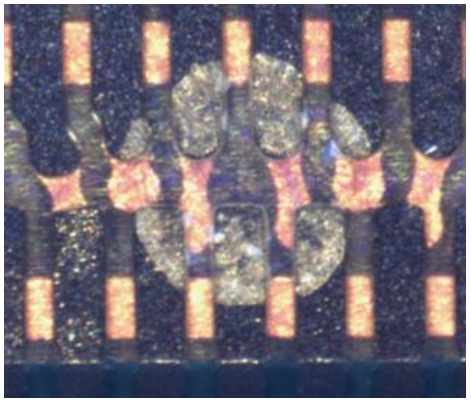




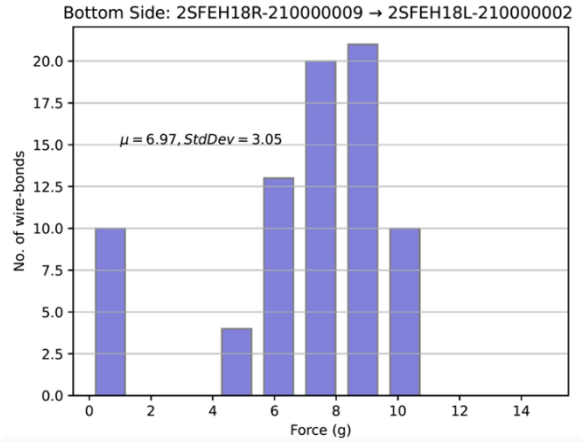
More info on noise studies: https://iopscience.iop.org/article/10.1088/1748-0221/17/12/C12008

Noise target: 1000e approx. equivalent to 6 VCTh (preamp threshold) units. 1 VCTh ~ 167e

Cleanliness

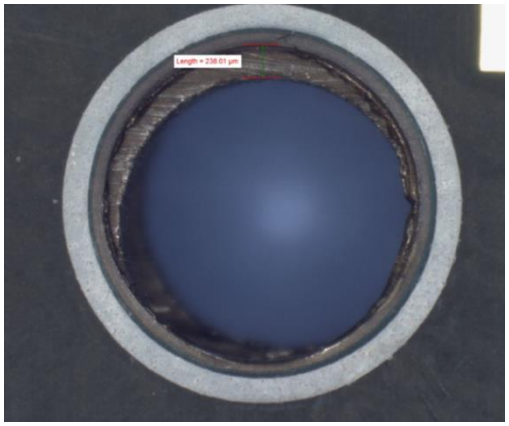


Some circuits arrive with contaminated wire bond pads.

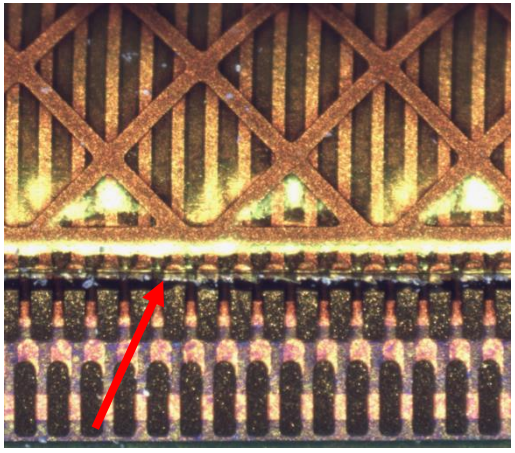


Contaminations are leading to poor wire bonding pull force (below 8g mean).

Misalignment

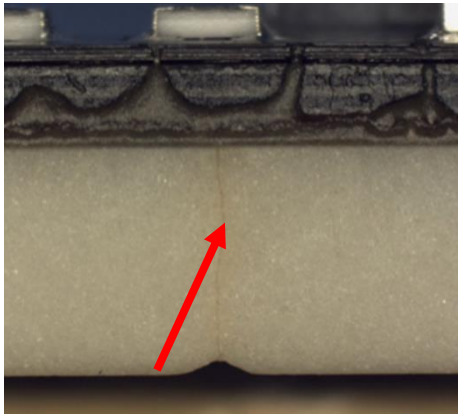


Alignment of fold-over is out of tolerance and the hole diameter is reduced.

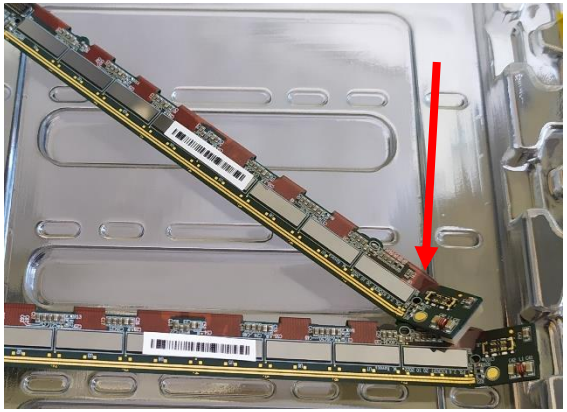


Misaligned coverlay is covering wirebond pads.

Mechanical damage



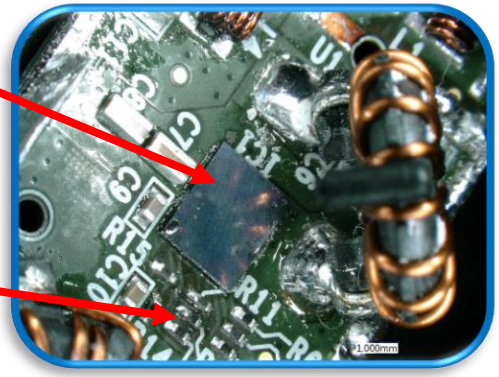
A cracked aluminium nitride spacer in the PS-ROH circuits.



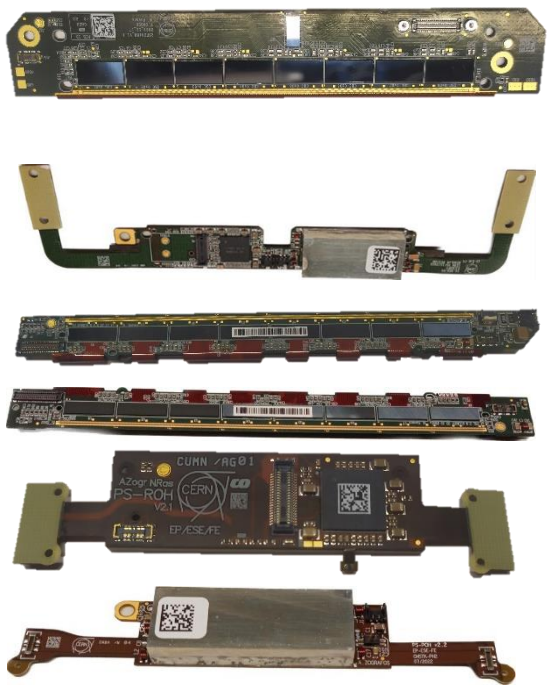
Circuits broken due to wrong orientation in packaging.

Problems with lead time:

- Flex lead time 60 -> 100 working days (WD)
- Assembly lead time 30 -> 50 WD



PCB yield is 50 - 70 %



Hybrid type	No. ordered	received	Tested good	Yield
2S-FEH 1.8 R	30	29	24	83%
2S-FEH 1.8 L	30	26	22	85%
2S-SEH split	15	23	12	52%*
2S-SEH reg.	15	17	9	53%*
PS-FEH 2.6 R	30	32	NO DATA	-
PS-FEH 2.6 L	30	33	NO DATA	-
PS-ROH	30	34	NO DATA	-
PS-POH split	15	18	18	100%
PS-POH reg.	15	20	20	100%

* Preliminary data, numbers might improve slightly with further tests. Yield includes visual inspection results in all cases.

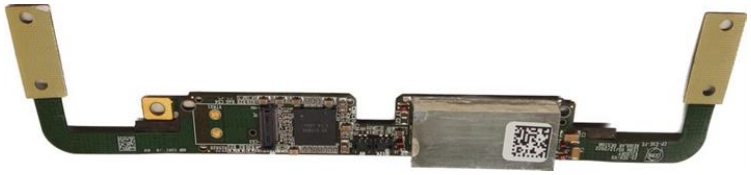
Hybrid designs

- All hybrid designs were successfully produced during the kick-off production.
- The 2S-FEH, PS-POH and PS-ROH hybrids were produced without major issues.
- The PS-FEH had to be redesigned to 5 layers in order to eliminate coverlay use.
- The 2S-SEH was redesigned before the kick-off production to avoid stacked vias. Two design variants were produced, preliminary test results show better noise performance in the case of the regular design.
- Two versions were made of the PS-POH circuits as well. Preliminary results are showing better performance in the case of regular design.
- Most of pre-series circuits are launched, in some cases further tests are needed.

Production:

- Lead times are much longer than expected and range up to half year.
- Yield is good in some cases, but improvement is needed for a few hybrid types.
- Cleanliness of wire-bond pads and precision need to be improved.

- Small details can be very important and can cause big problems if not mitigated in time. A good example is the coverlay issue.
- It might not be a good idea to change a design that is close to the specified performance. A good example is the split-plane POH and SEH design.
- Trying to hurry can lead to more mistakes from the suppliers, which can cause further delays. A good example is the resistor divider issue in the 2S-SEH.
- Open communication with the suppliers is extremely important to resolve issues or misunderstandings.



Thank you for your attention!

Please follow the next presentations of our working group:

- **Angelos Zografos** – CMS Outer Tracker Phase-2 Upgrade on-module powering: today 11:40 Sirocco room
- **Patryk Szydlik** – Commissioning of the Test System for the Phase-2 Upgrade of the CMS Outer Tracker: Thursday 17:40 poster session