Single Event Effects characterization of a commercial 28 nm CMOS technology

TWEPP 2023

2023/10/07 - Geremeas

EP-ESE-ME
G. Borghello, D. Ceresa, R. Pejašinović, F. Piernas Diaz, G. Bergamin and K. Kloukinas
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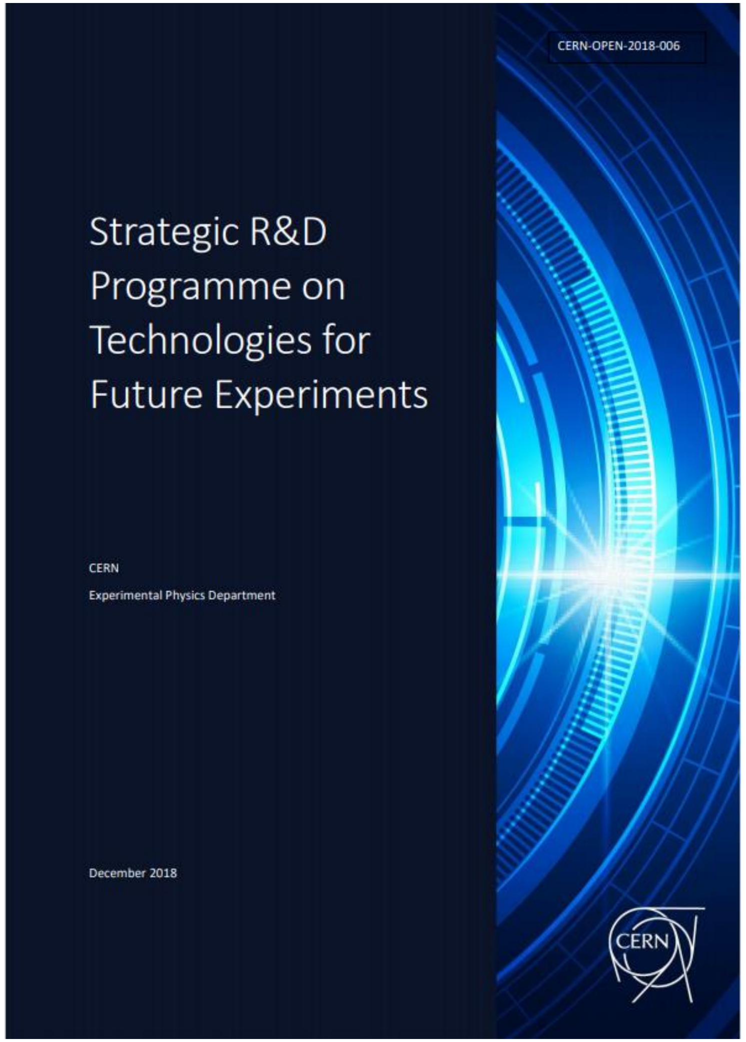
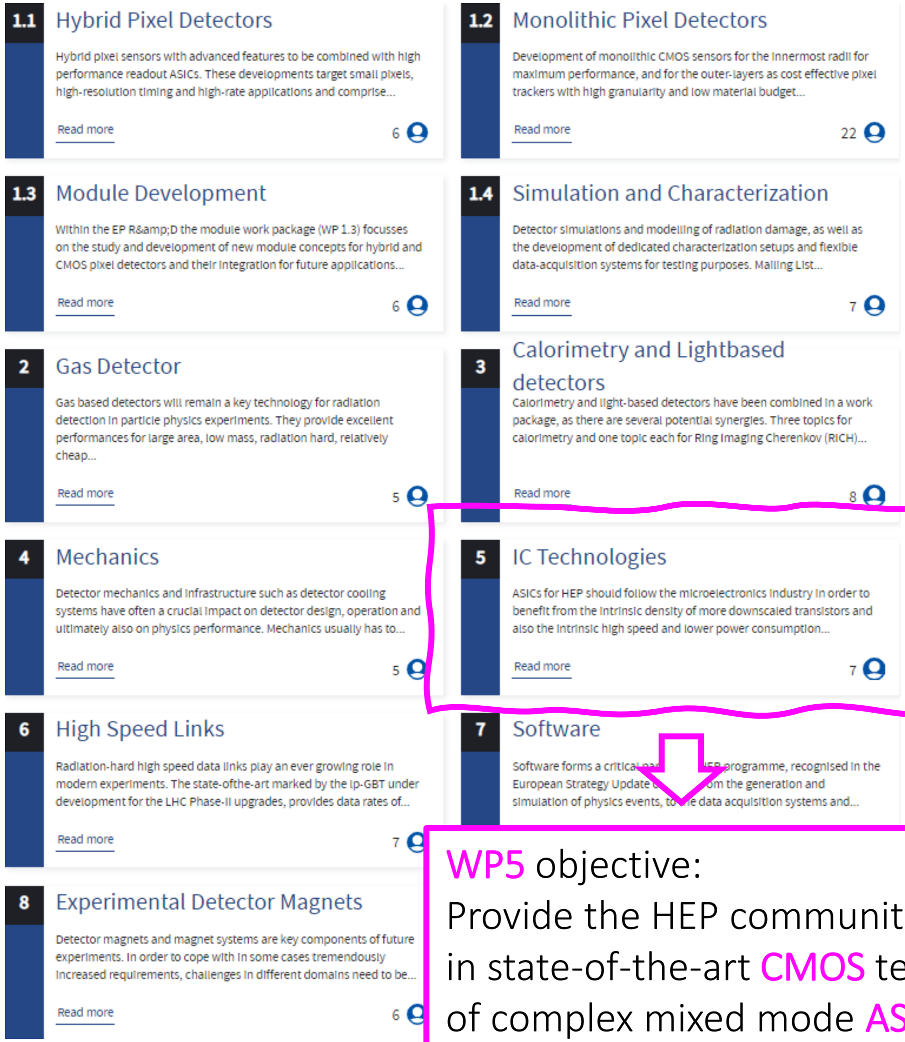
EP-R&D - WP5.1



https://ep-dep.web.cern.ch/sites/ep-dep.web.cern.ch/files/Report%20final_0.pdf

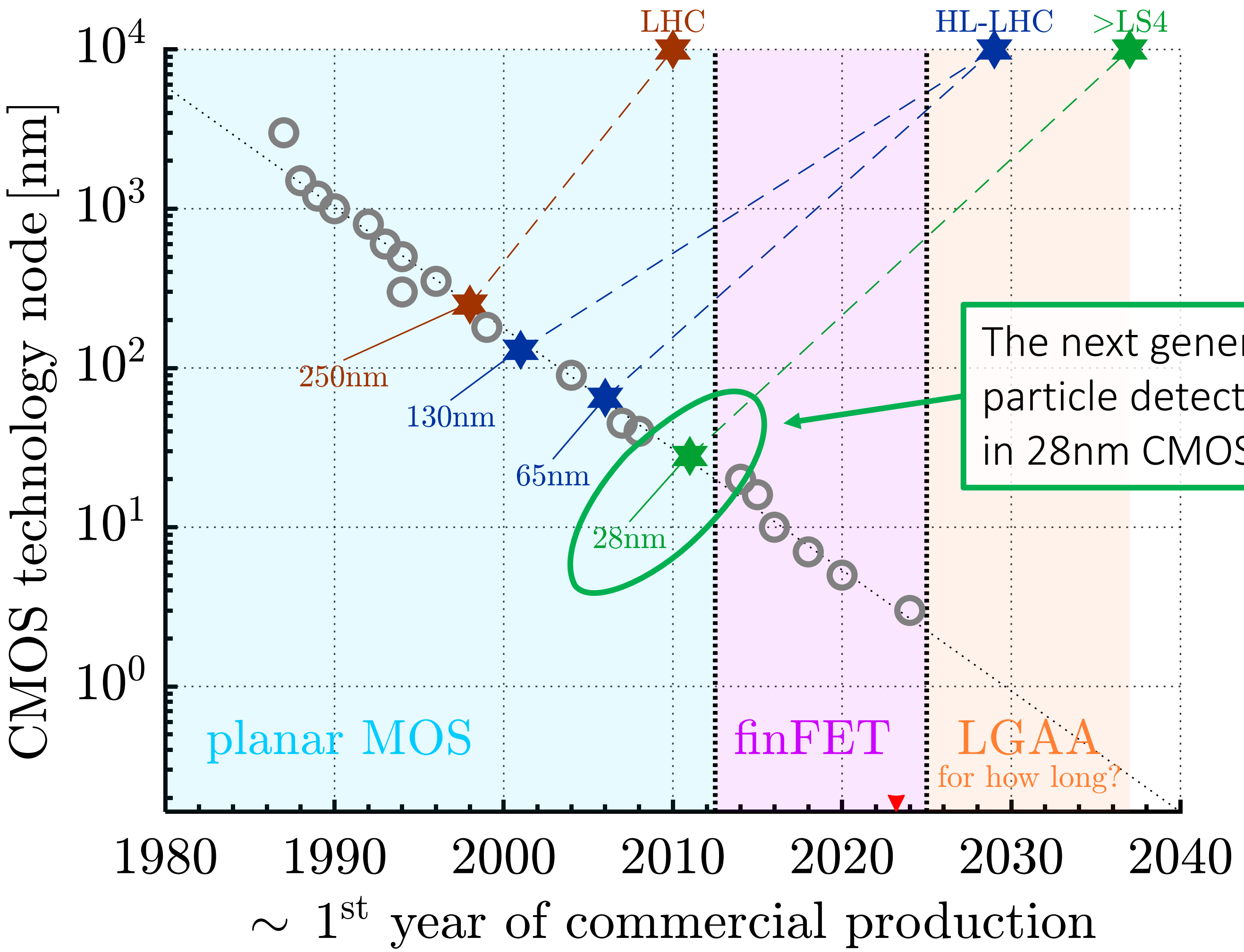


https://ep-rnd.web.cern.ch/

WP5 objective:
Provide the HEP community with solid infrastructure in state-of-the-art **CMOS** technologies for the design of complex mixed mode **ASICs**

https://indico.cern.ch/event/1042567/contributions/4419842/attachments/2272167/3859068/PresentationIPBlocksForumV3_noAdditionalSlides.pdf

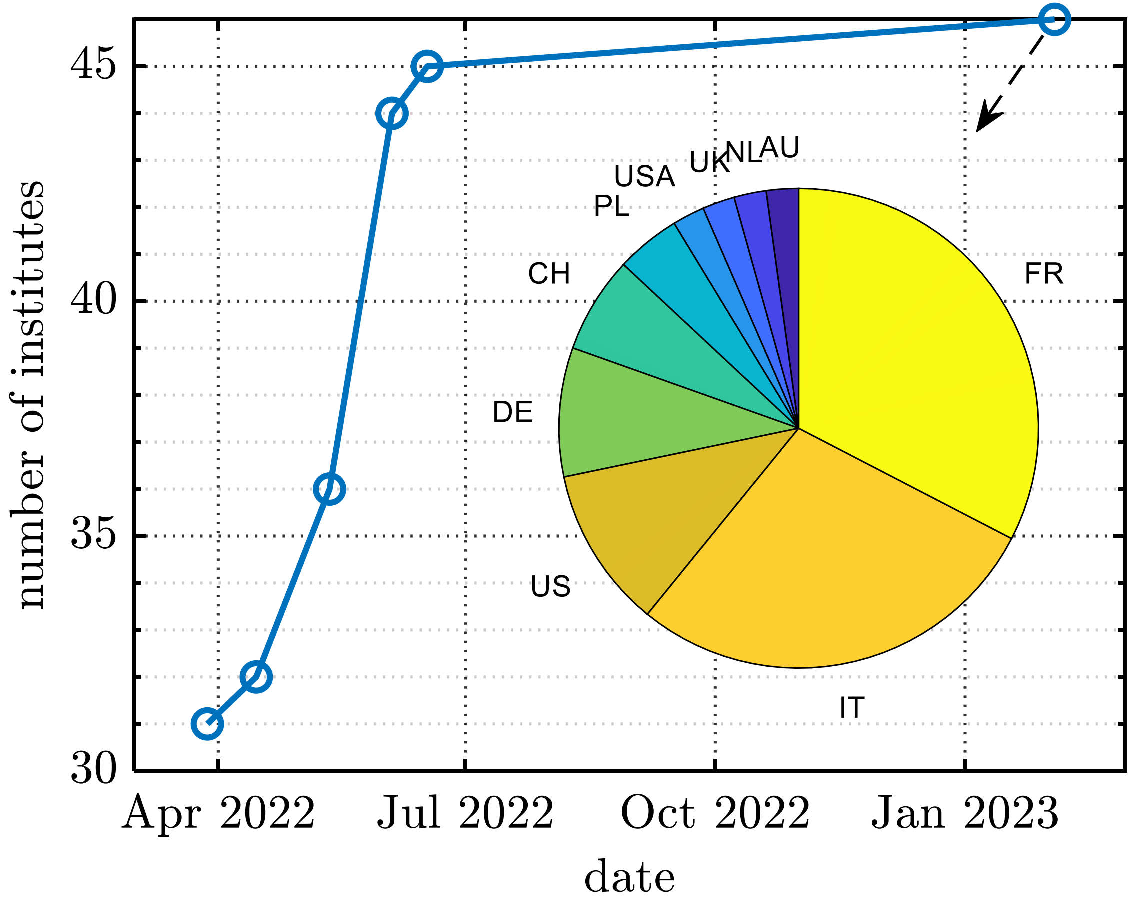
CERN & CMOS



The next generations of ASICs for particle detectors will be designed in 28nm CMOS technology

data from:
https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_3nm
https://irds.ieee.org/editions/2022/more-moore

ASICs in 28nm technology



list of Institutes that collaborate in 28nm-ASIC development projects with CERN

https://asic-support-docs.web.cern.ch//nda/

TID effects in 28nm technology

investigation of **TID** effects in 28 nm technology is at an **advanced stage**

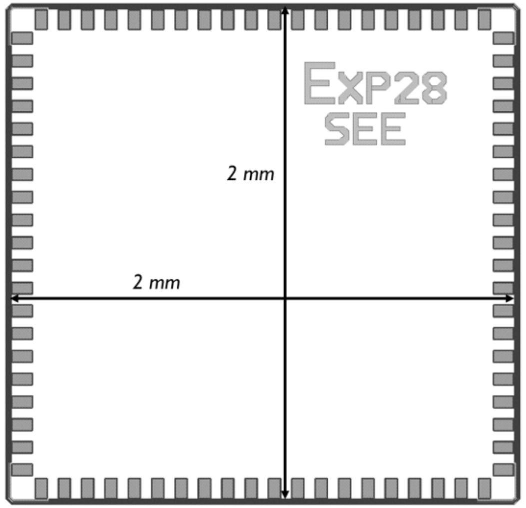
- Borghello, G., et al. "Total ionizing dose effects on ring-oscillators and SRAMs in a commercial 28 nm CMOS technology." *Journal of Instrumentation* 18.02 (2023): C02003.
- M. Piller *et al*., "Generic Analog 8 Bit DAC IP Block in 28nm CMOS for the High Energy Physics Community," *2022 Austrochip Workshop on Microelectronics (Austrochip)*, Villach, Austria, 2022, pp. 5-8, doi: 10.1109/Austrochip56145.2022.9940783.
- Bonaldo, Stefano, et al. "Influence of halo implantations on the total ionizing dose response of 28-nm pMOSFETs irradiated to ultrahigh doses." *IEEE Transactions on Nuclear Science* 66.1 (2018): 82-90.
- Zhang, Chun-Min, et al. "Characterization and modeling of Gigarad-TID-induced drain leakage current of 28-nm bulk MOSFETs." *IEEE Transactions on Nuclear Science* 66.1 (2018): 38-47.
- Zhang, Chun-Min, et al. "Characterization of gigarad total ionizing dose and annealing effects on 28-nm bulk MOSFETs." IEEE Transactions on Nuclear Science 64.10 (2017): 2639-2647.
- ....

What is the sensitivity to **Single Event Effects** (SEE) of **28nm** CMOS technology?

EXP28:SEE/ANA

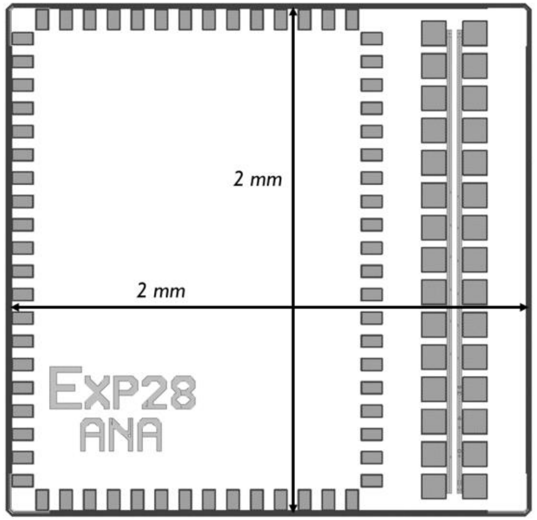
D. Ceresa, G. Borghello, G. Bergamin, F. Piernas Diaz, R. Pejašinović, K. Kloukinas

SINGLE EVENT EFFECT (SEE)



NON-DESTRUCTIVE EVENTS (SBU, MBU, SET)

ANALOG IP BLOCKS



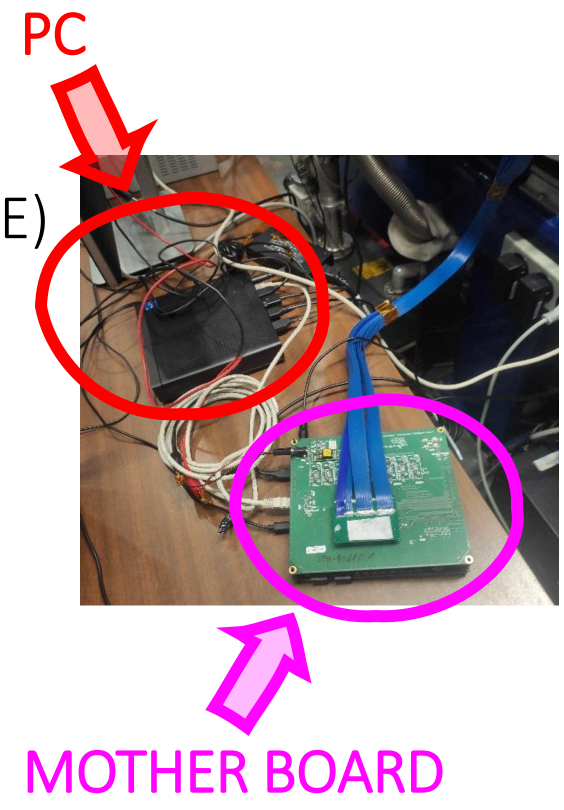
DESTRUCTIVE EVENTS (SEL)

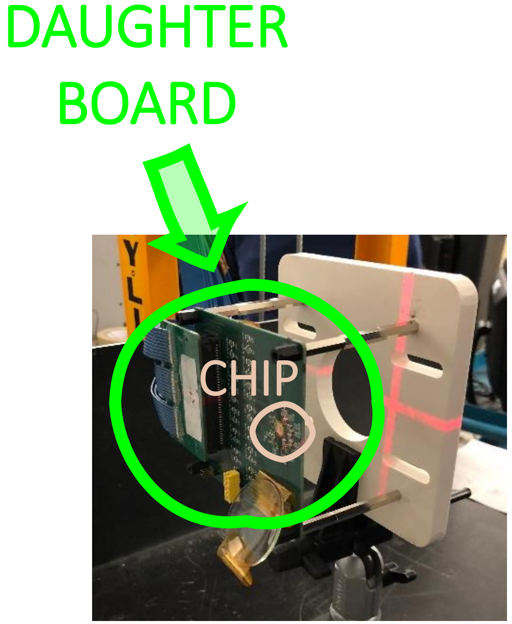
chips received **mid 2022**

EXP28:SEE/ANA – TESTs

- Heavy-ions test at HIF (Louvain-La-Neuve, BE)
  https://uclouvain.be/en/research-institutes/irmp/crc/heavy-ion-facility-hif.html
  - ➢ 2 days of test end of November 2022

- Proton test at TRIUMF (Vancouver, CA)
  https://www.triumf.ca/pif-nif/proton-irradiation
  - ➢ 1 (long) day beginning of December 2022
  - ➢ tested only EXP28-SEE





Test system developed by Risto Pejašinović and Francisco Piernas Diaz!

RADNEXT
(This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101008126.)

EXP28:SEE/ANA – TESTs

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EXP28:SEE/ANA – HI TEST

2 days of test in November 2022

ion cocktail

M/Q	Ion	DUT energy [MeV]	Range [µm Si]	LET [MeV/(mg/cm²)]
3.25	$^{13}C^{4+}$	131	269.3	1.3
3.14	$^{22}Ne^{7+}$	238	202.0	3.3
3.37	$^{27}Al^{8+}$	250	131.2	5.7
3.27	$^{36}Ar^{11+}$	353	114.0	9.9
3.31	$^{53}Cr^{16+}$	505	105.5	16.1
3.22	$^{58}Ni^{18+}$	582	100.5	20.4
3.35	$^{84}Kr^{25+}$	769	94.2	32.4
3.32	$^{103}Rh^{31+}$	957	87.3	46.1
3.54	$^{124}Xe^{35+}$	995	73.1	62.5

https://uclouvain.be/en/research-institutes/irmp/crc/parameters-and-available-particles.html

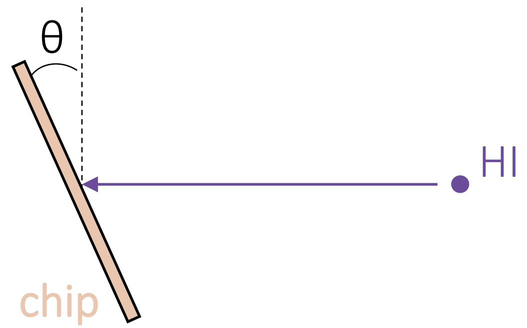
EXP28:SEE

→ tested for **all ions** at θ = 0° and 45°

→ fluence **~5x10⁶ ni/cm²** for each ion/angle

EXP28:ANA

→ several combination of ion/angle/voltage (more details later)



$$LET_{eff} = LET/\cos(\theta)$$

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  - tested only EXP28-SEE

Only EXP28:SEE chip
(non-destructive events)

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EXP28:SEE/ANA – PROTON TEST

1 (long) day beginning of December 2022

test n.	1	2	3	4	5	6	7
chip	A	A	A	A	B	B	B
energy [MeV]	480	480	480	480	480	480	480
fluence [$cm^{-2} \times 10^9$]	174	182	184	184	183	184	184
flux [$cm^{-2} \times 10^6/s$]	520	130	1300	1300	1300	1300	1300

- 2 chips (A, B)
- 2 energies (480, 350 MeV)

test n.	8	9	10	11	12	13	14	15	16	17	18
chip	B	B	B	B	B	B	A	A	A	A	A
energy [MeV]	350	350	350	350	350	350	350	350	350	350	350
fluence [$cm^{-2} \times 10^9$]	90	183	183	184	184	90	184	184	64	385	385
flux [$cm^{-2} \times 10^6/s$]	256	256	640	640	640	128	640	640	128	640	640

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EXP28:SEE/ANA

D. Ceresa, G. Borghello, G. Bergamin, F. Piernas Diaz, R. Pejašinović, K. Kloukinas

first comprehensive overview of the SEE sensitivity of 28nm CMOS technology

- ✓ minimum distance between D-flip-flop to avoid MBU
- ✓ cross section of DFF for HI and protons
- ✓ cross section of foundry SRAMs for HI and protons
- ✓ MBU evaluation in scrambled SRAMs
- ✓ evaluation of a method to predict SEEs rate in the accelerator environment using heavy-ion data
- ✓ cross section and pulse length for SET with HI and protons
- ✓ multi-SET
- ✓ sensitivity to Single-Event-Latch-UP

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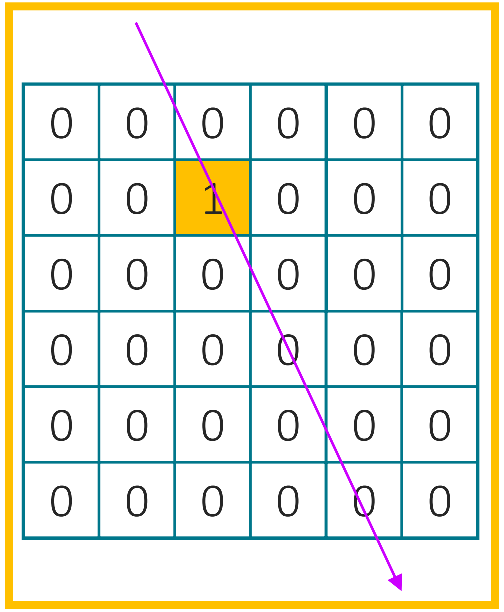
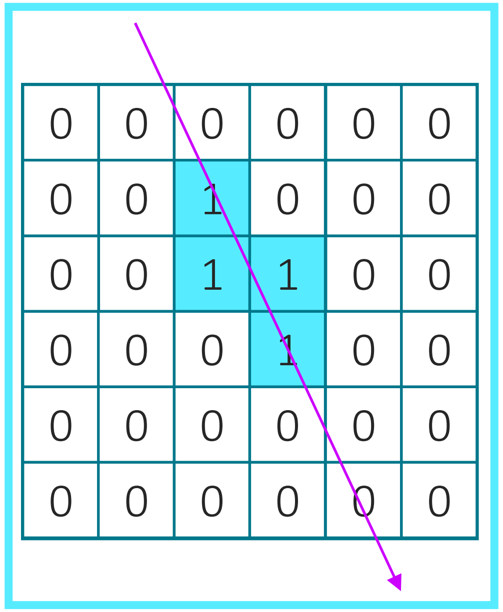
MULTI-BIT-UPSET

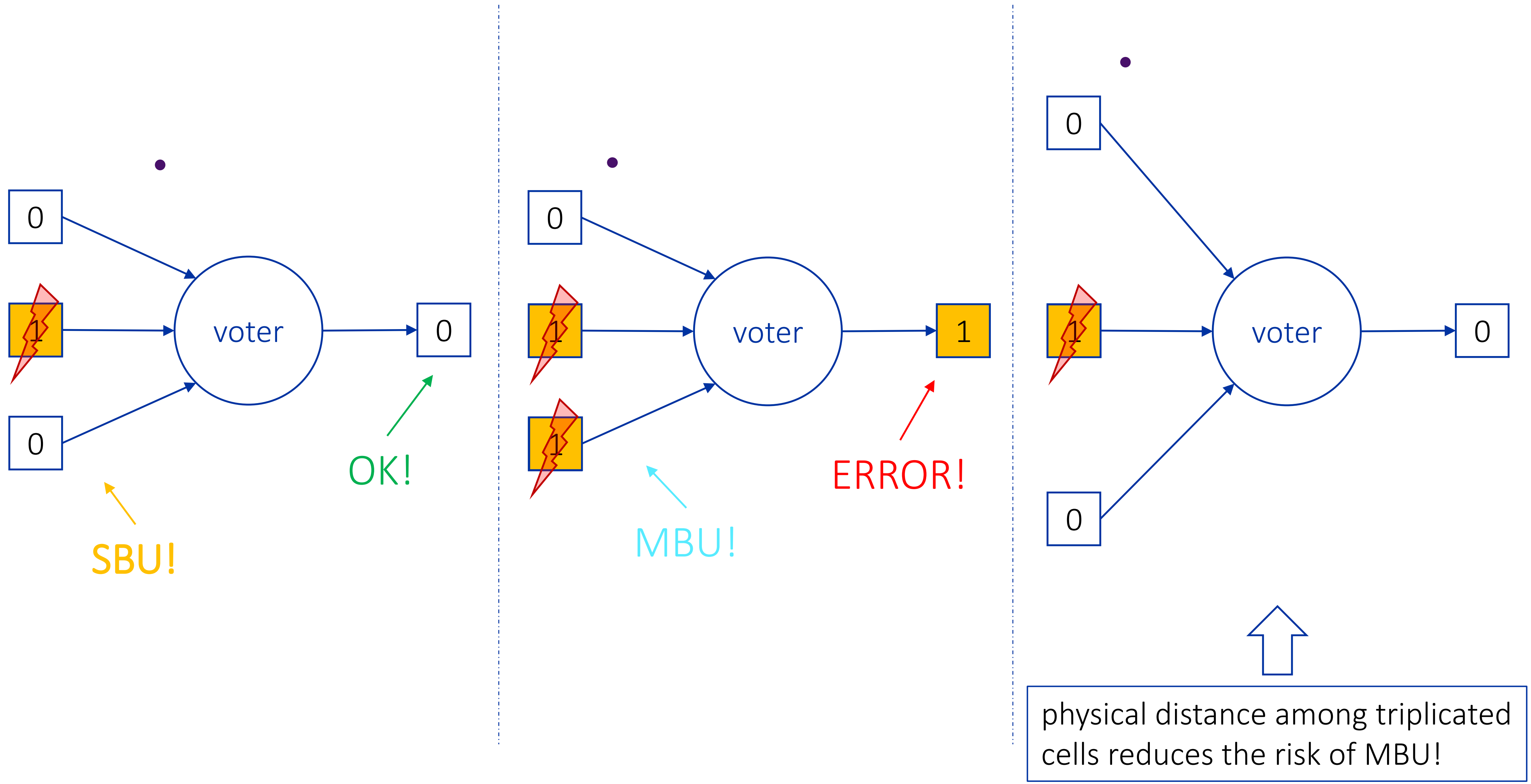
Single-bit-upset (SBU)



Multi-bit-upset (MBU)

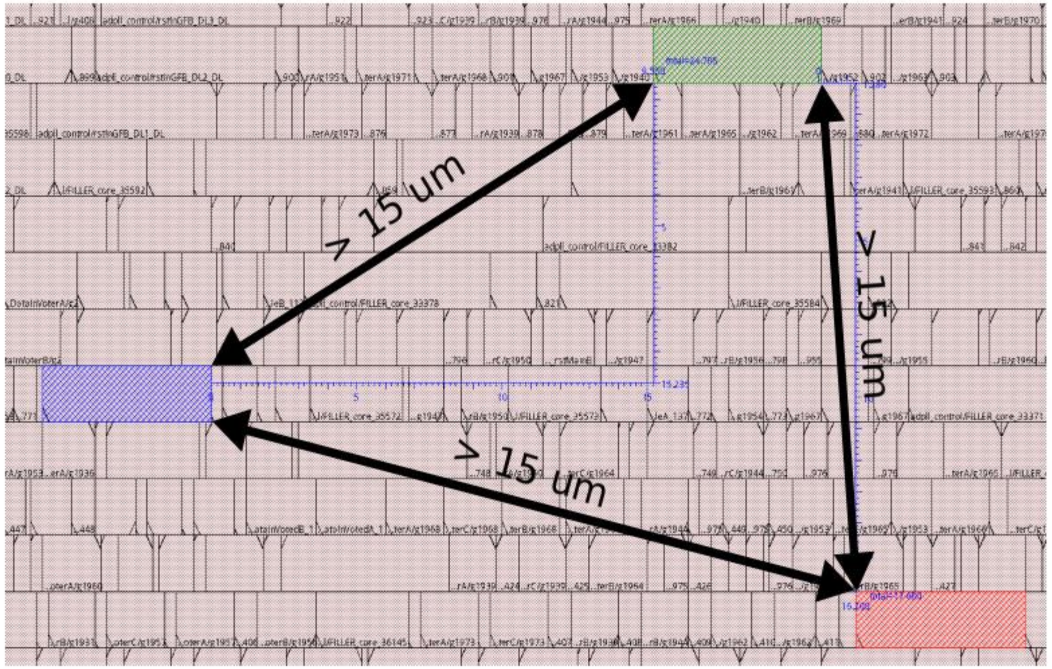


TRIPLICATION



TRIPLICATION

15 µm typically used in 65nm technology

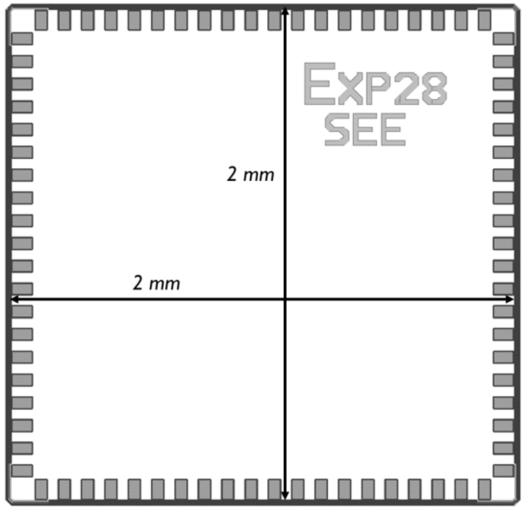


Stefan Biereigel: Investigations on Multi-Bit Upsets in 65nm CMOS (https://indico.cern.ch/event/959655)

What is the minimum distance between DFF to avoid MBU in 28nm technology?

EXP28:SEE

SINGLE EVENT EFFECT (SEE)



3 test structures:

- 7 matrices of D-flip-flops
- 4 foundry SRAMs

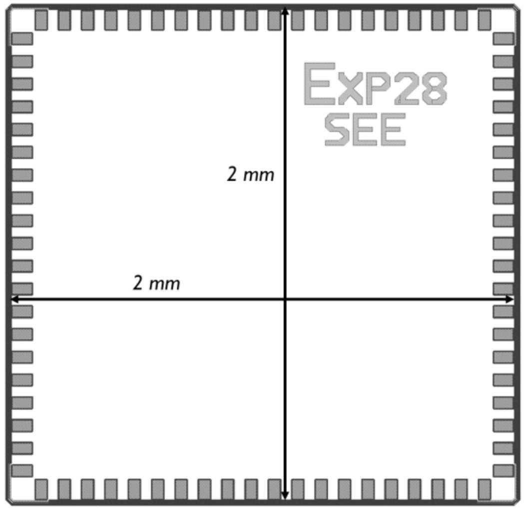
} single- and multi-bit-upsets (SBU, MBU)

- 16 chains of inverters + vernier detector

} single-event-transient (SET)

EXP28:SEE

SINGLE EVENT EFFECT (SEE)



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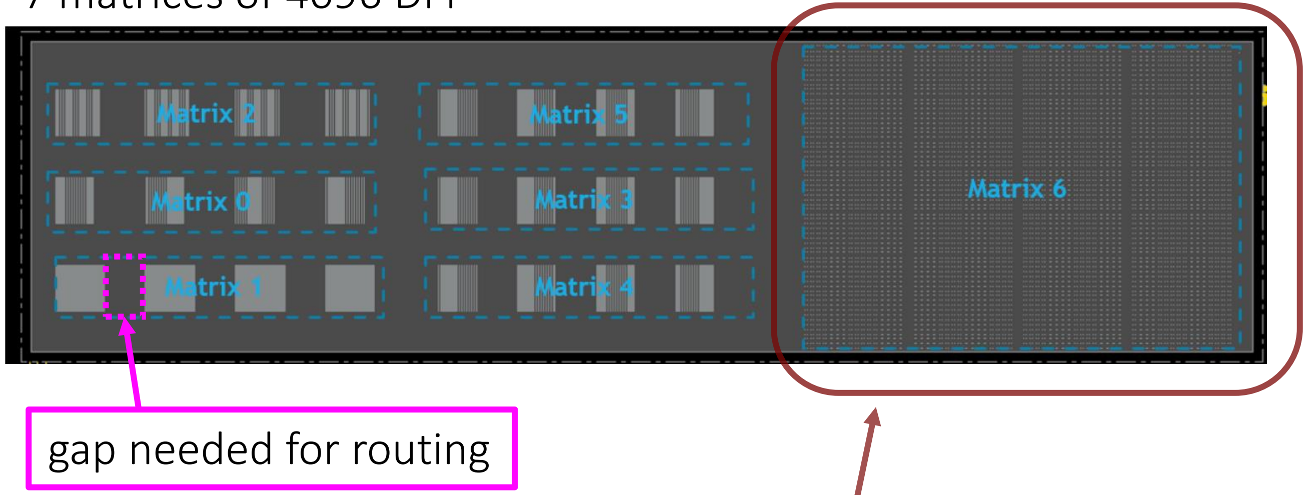
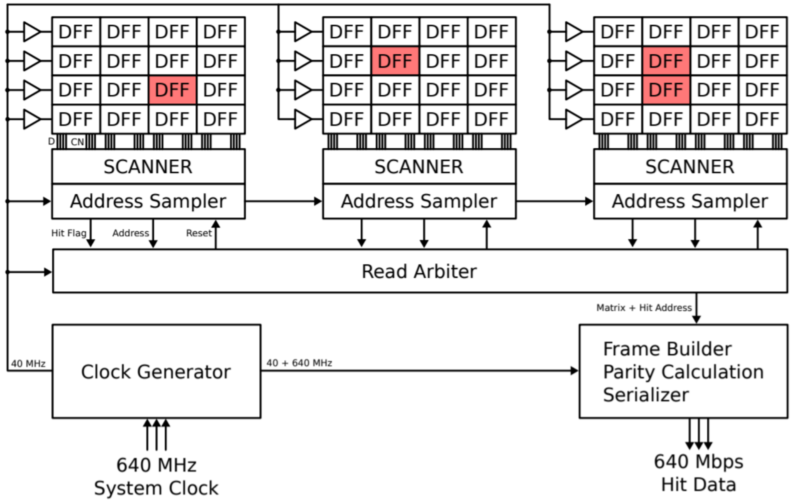
single-event-transient (SET)

EXP28:SEE – DFF

7 matrices of 4096 DFF

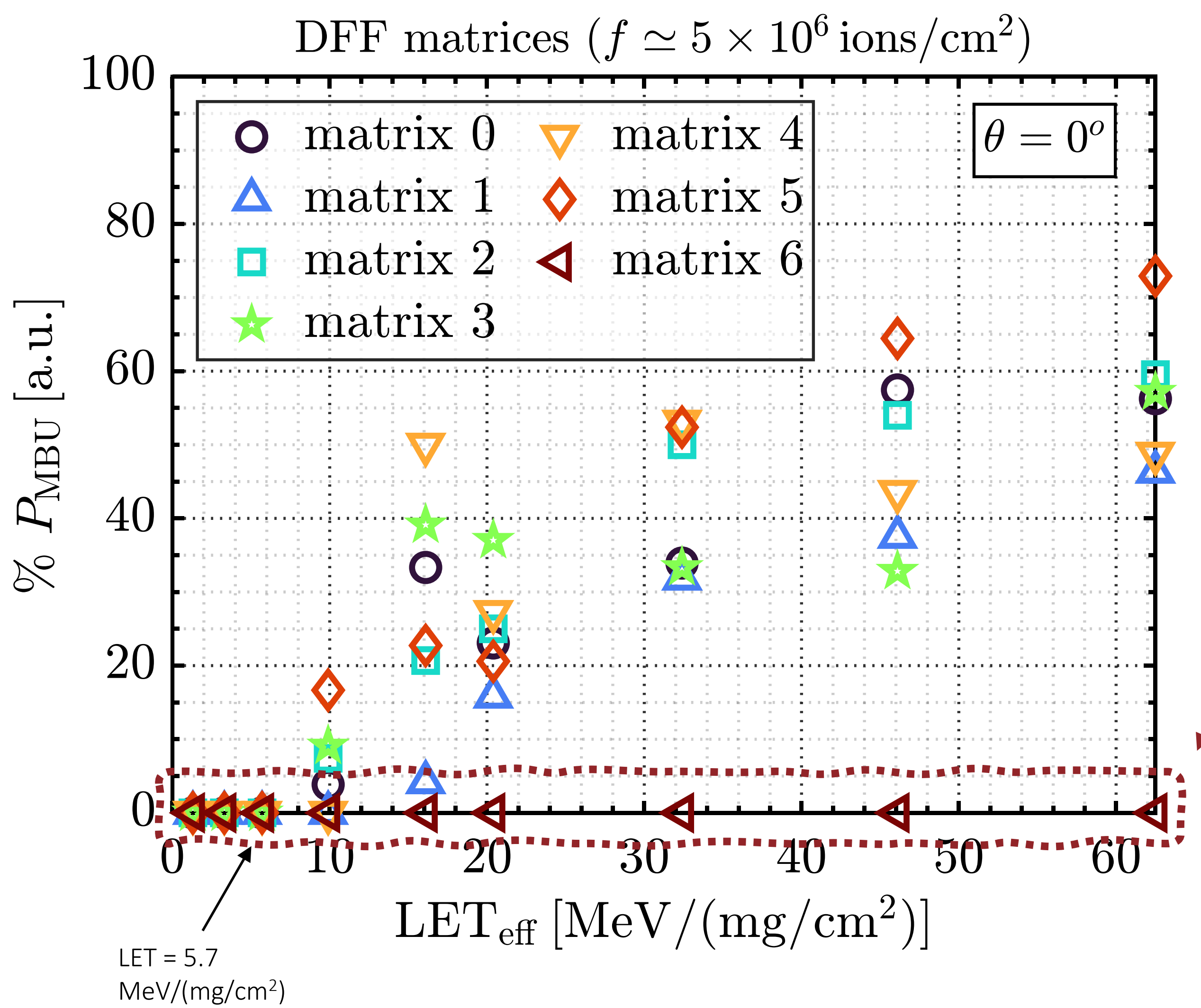




Stefan Biereigel: Investigations on Multi-Bit Upsets in 65nm CMOS (https://indico.cern.ch/event/959655)

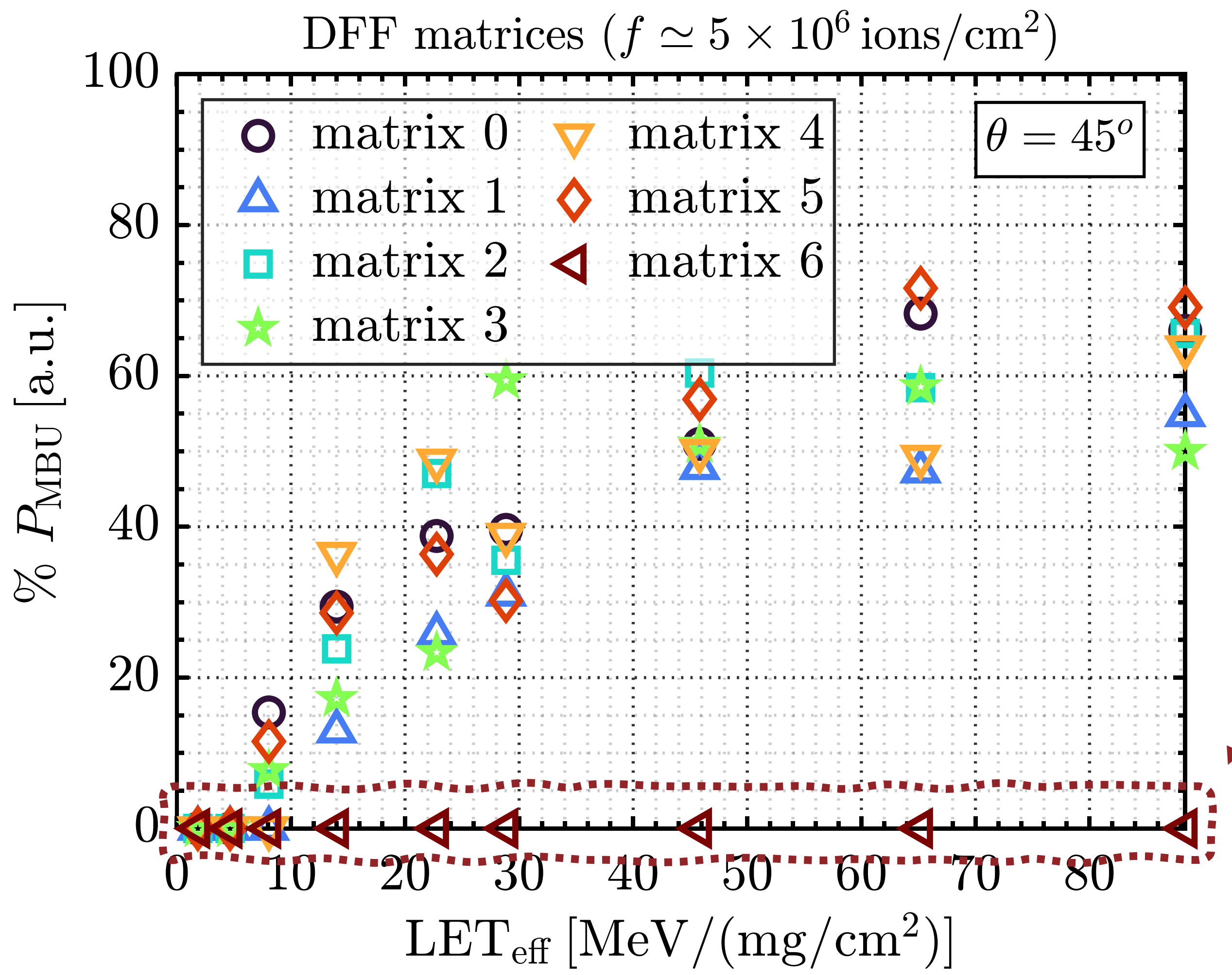
0	D_{FF}D1	(D Flip-Flop with Sync Clear)
1	D_{FF}D1+C_{KB}D1	(D Flip-Flop with Sync Clear + buffer in the D-Q path)
2	D_{FF}D4	(D Flip-Flop with D4 driving strength)
3	D_{FF}D1LVT	(Low-Vt flavor)
4	D_{FF}D1UHVT	(High-Vt flavor)
5	D_{FF}D1ULVT	(UltraLow-Vt flavor)
6	D_{FF}D1	(~5.5 µm spacing between DFF)

EXP28:SEE – DFF – MBU – HI



no MBU in matrix 6!

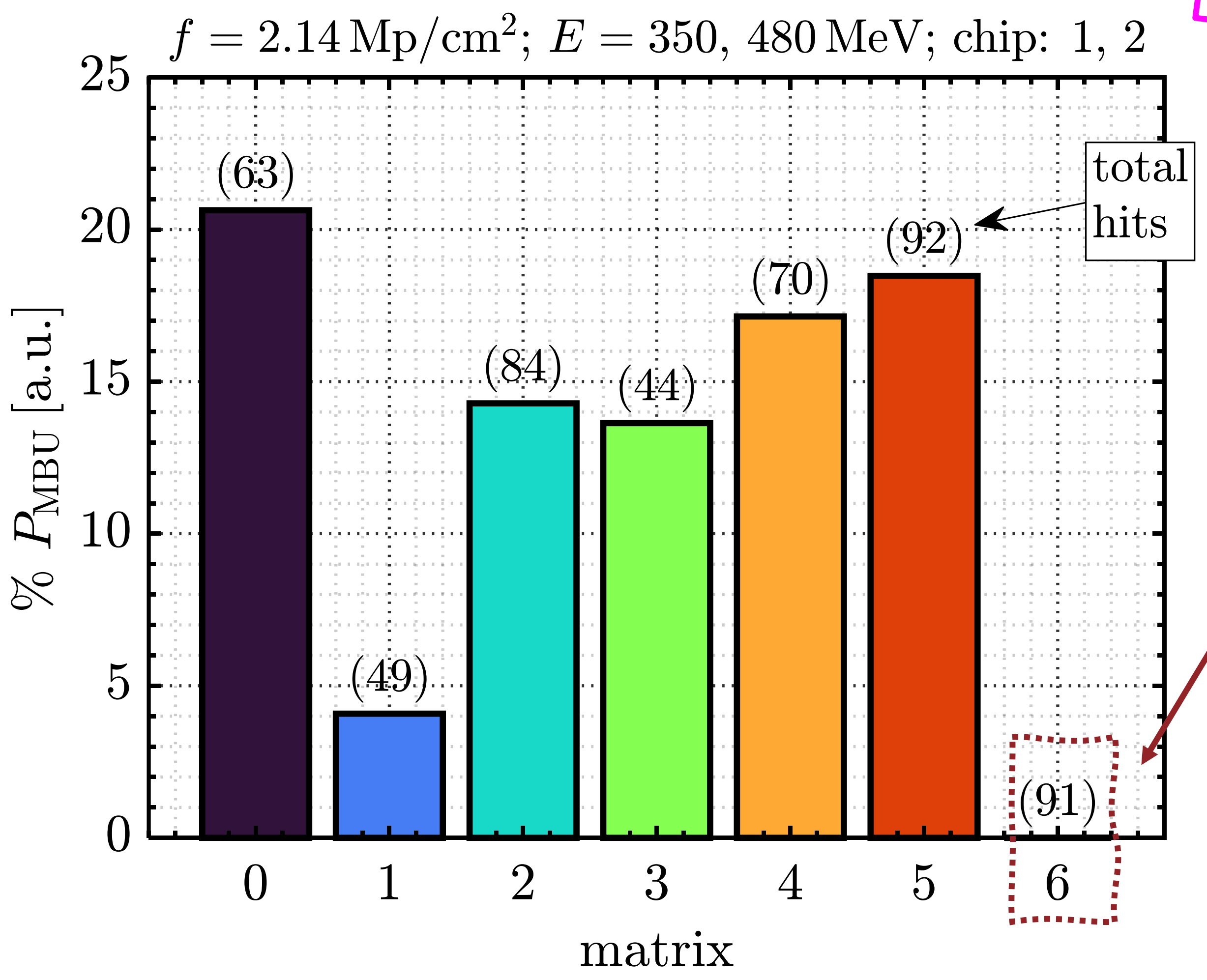
EXP28:SEE – DFF – MBU – HI



results confirmed at $\theta = 45°$!

no MBU in matrix 6!

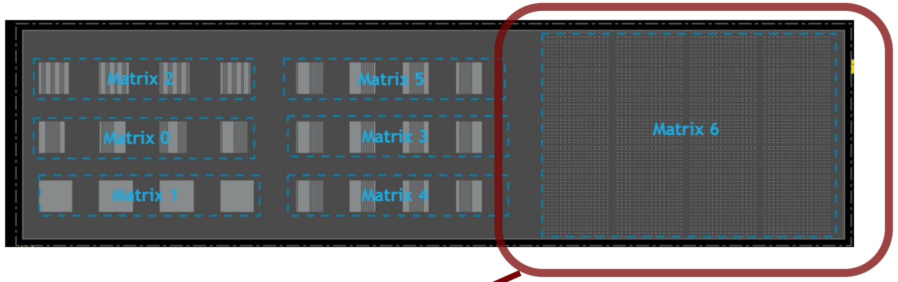
EXP28:SEE – DFF – MBU – protons

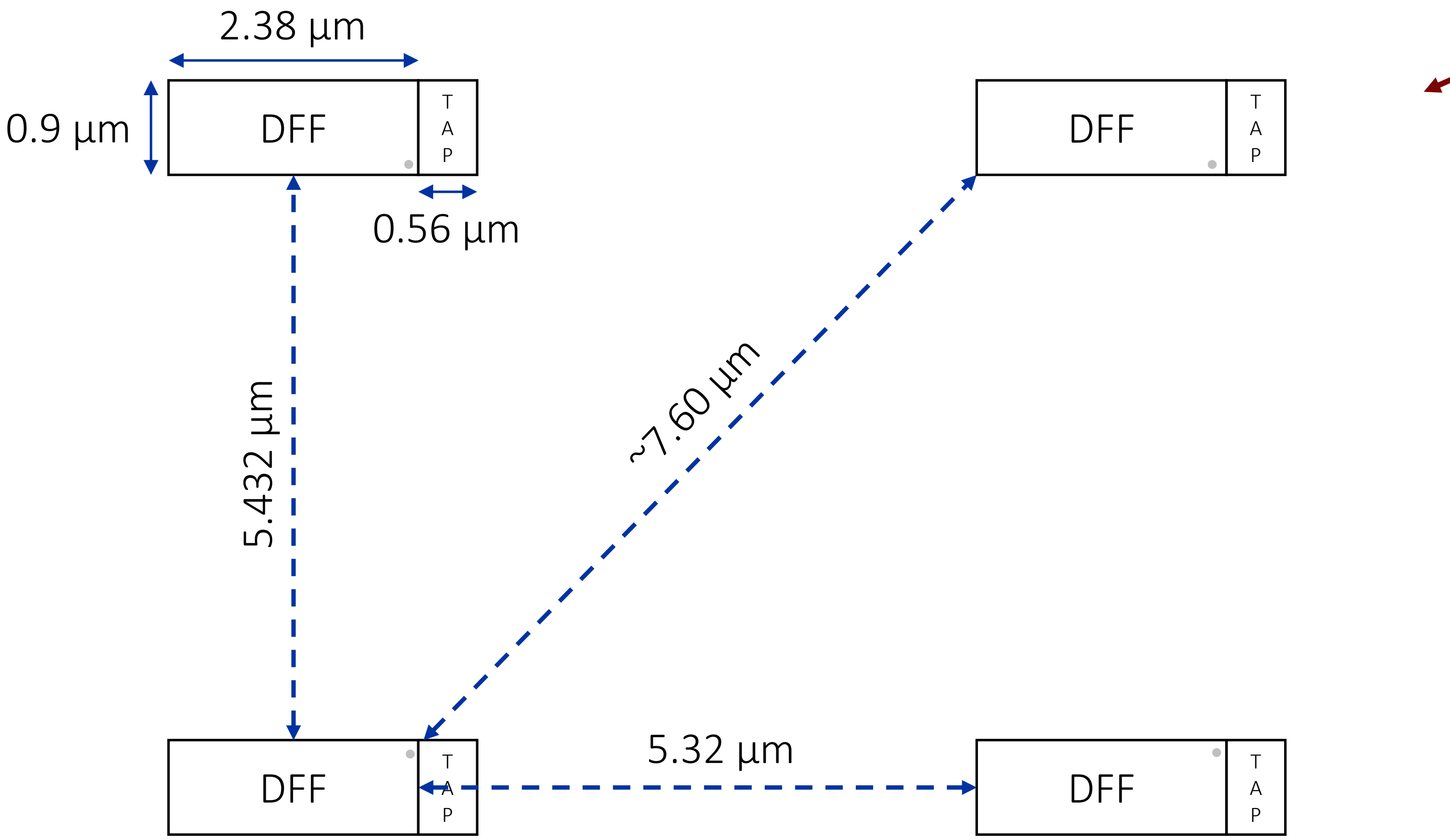


results confirmed by proton test!

no MBU in matrix 6!

EXP28:SEE – DFF – MATRIX 6





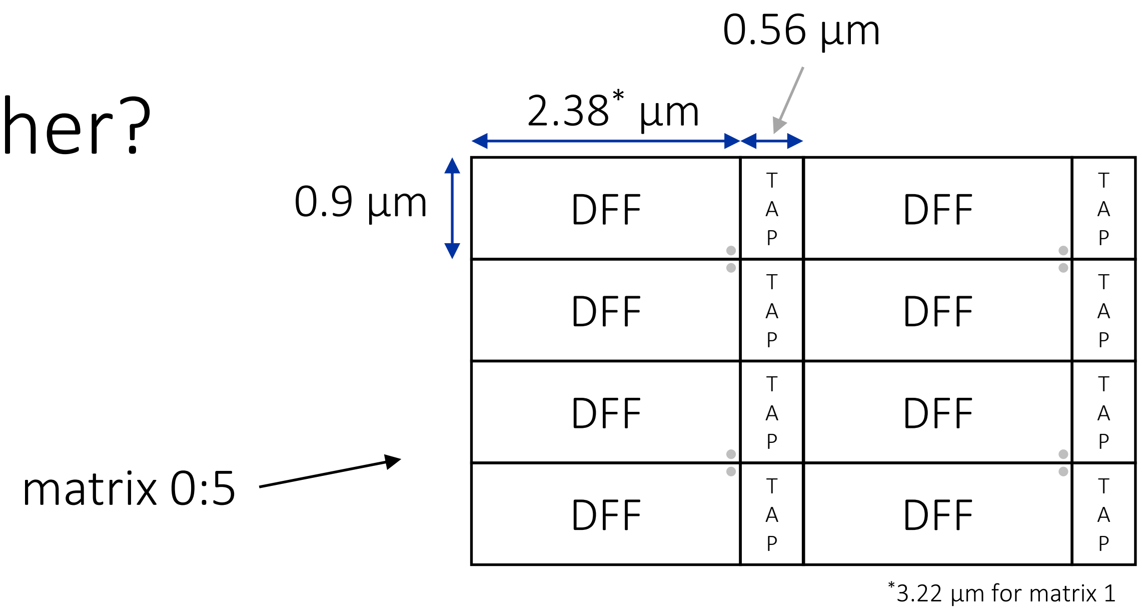
dimensions as drawn

EXP28:SEE – DFF

~6 µm spacing between DFFs drastically reduces probability of MBU!

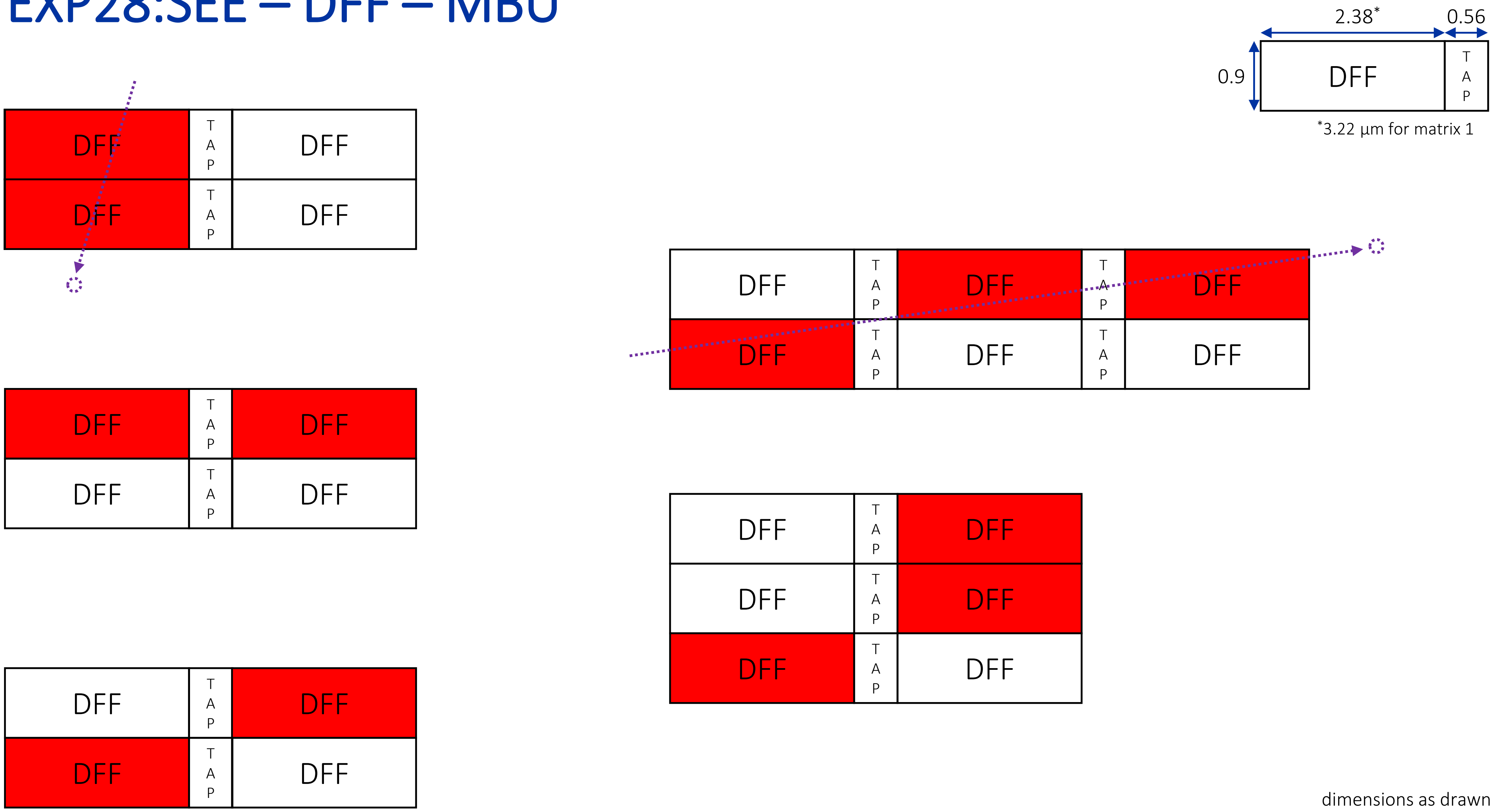
- key information for triplication strategy!
- ~2.5 times less than the 15 µm typically used in 65nm technology!

Can we reduce it further?



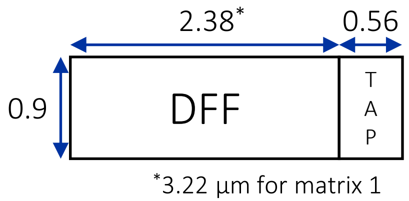
dimensions as drawn

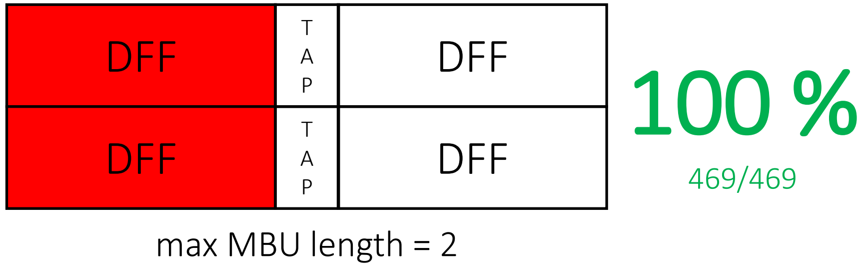
EXP28:SEE – DFF – MBU

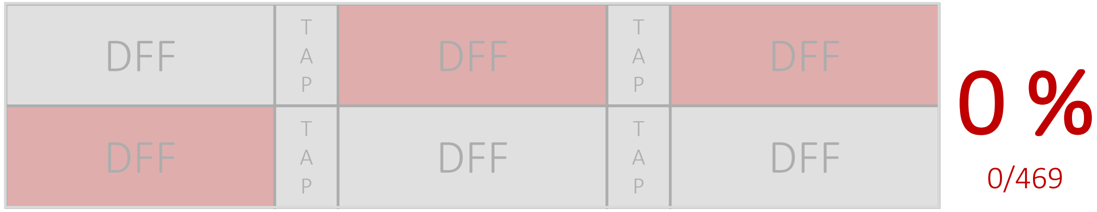


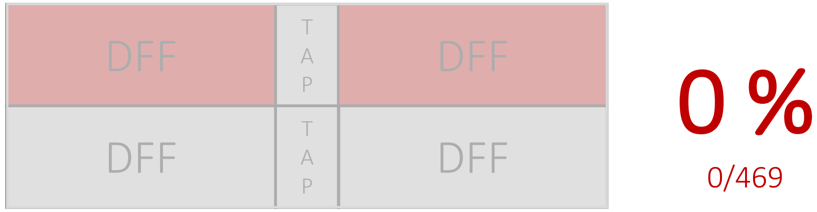
dimensions as drawn

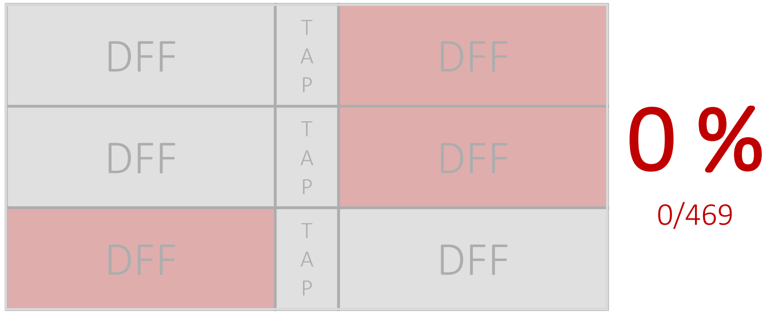
EXP28:SEE – DFF – MBU – HI

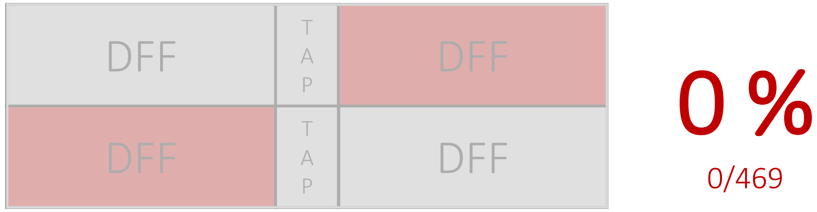






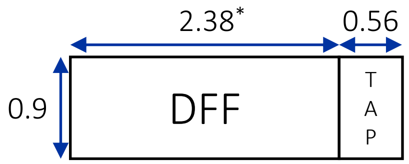




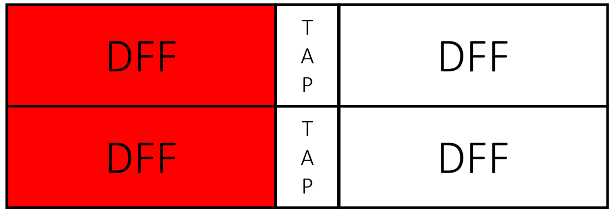


dimensions as drawn

EXP28:SEE – DFF – MBU – protons



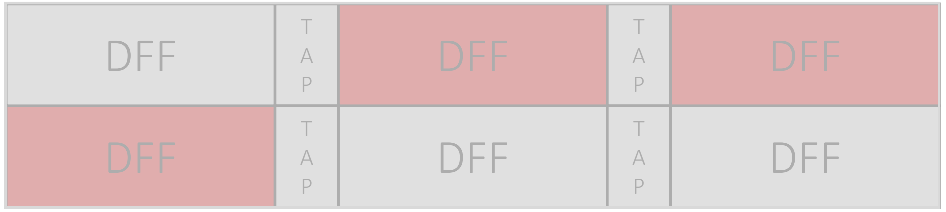
*3.22 μm for matrix 1



96.5 %

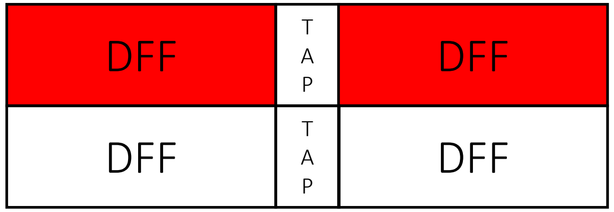
55/57

max MBU length = 2



0 %

0/57

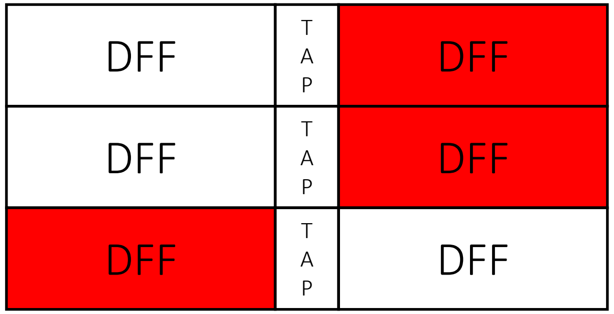


1.75 %

1/57

matrix 5, test 6

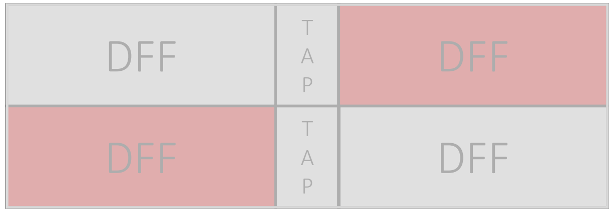
max MBU length = 2



1.75 %

1/57

matrix 2, test 6



0 %

0/57

dimensions as drawn

EXP28:SEE – DFF

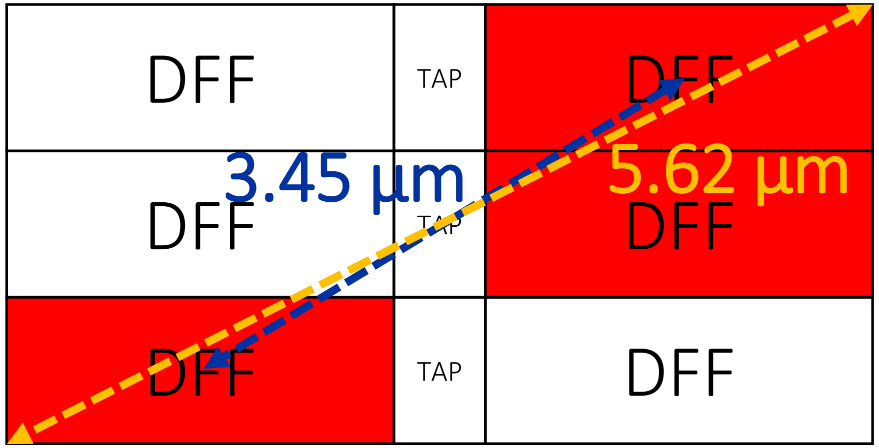
~6 µm spacing between DFFs drastically reduces probability of MBU!

- key information for triplication strategy!
- ~2.5 times less than the 15 µm typically used in 65nm technology!

Can we reduce it further?

maybe yes,
probably not by much

anyway, not with these data:
very small statistics, not fine enough matrix



dimensions as drawn

EXP28:SEE/ANA

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Huhtinen, M., and F. Faccio. "Computational method to estimate Single Event Upset rates in an accelerator environment." *NIMA* 450.1 (2000): 155-172.

- minimum distance between D-flip-flop to avo…
- evaluation of a method to **predict SEEs rate in the accelerator environment using heavy-ion data**
- pu…
- se…

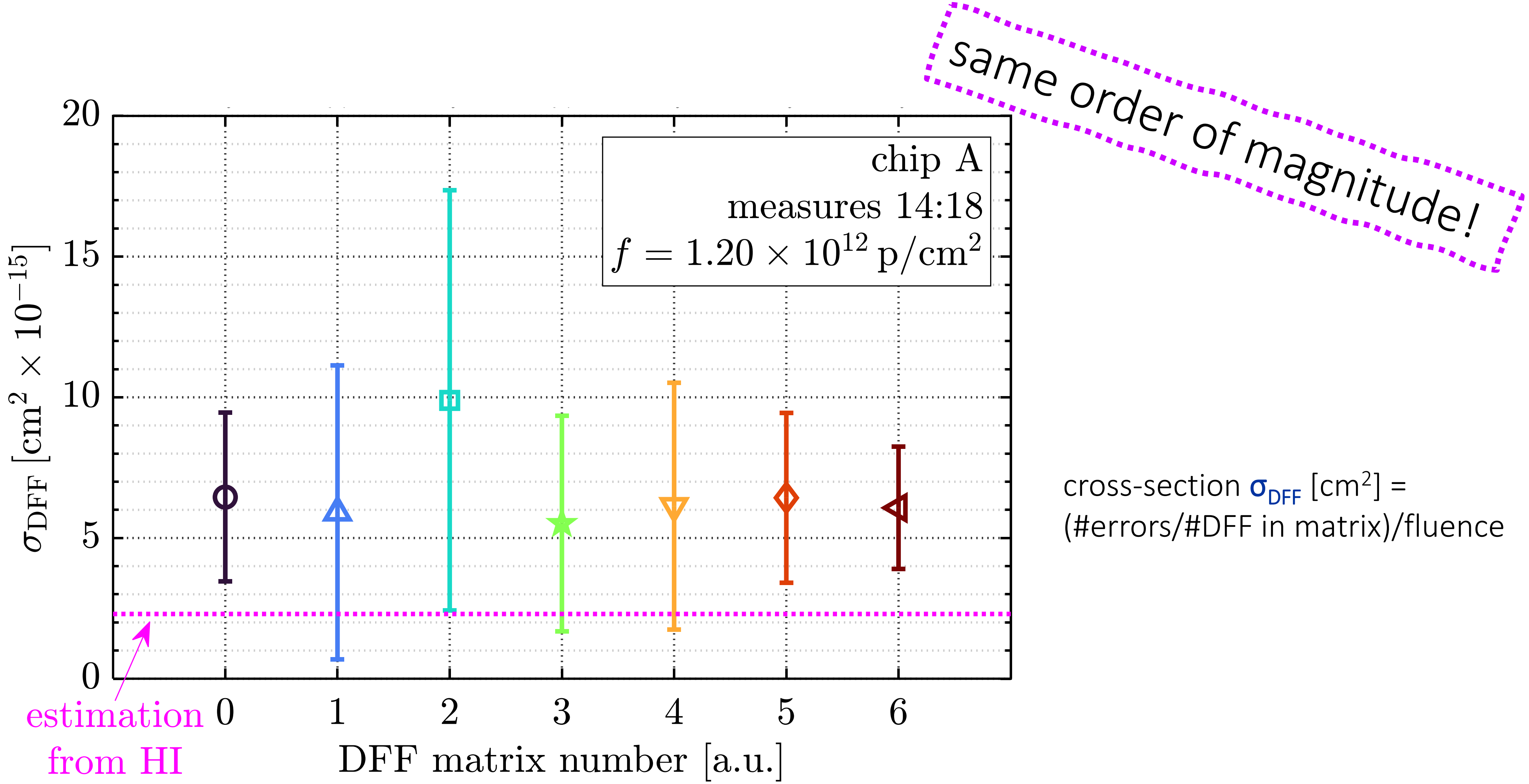
heavy-ions test:

☺ large statistic (many errors in a short amount of time)

☺ easier to trigger single-event-latch-up (SEL)

☹ not representative of the radiation environment in particle detectors

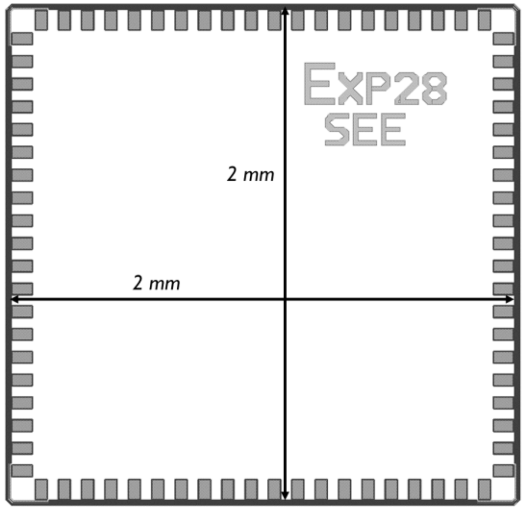
EXP28:SEE – DFF – σ – protons



cross-section σ_{DFF} [cm^2] = (#errors/#DFF in matrix)/fluence

EXP28:SEE

SINGLE EVENT EFFECT (SEE)



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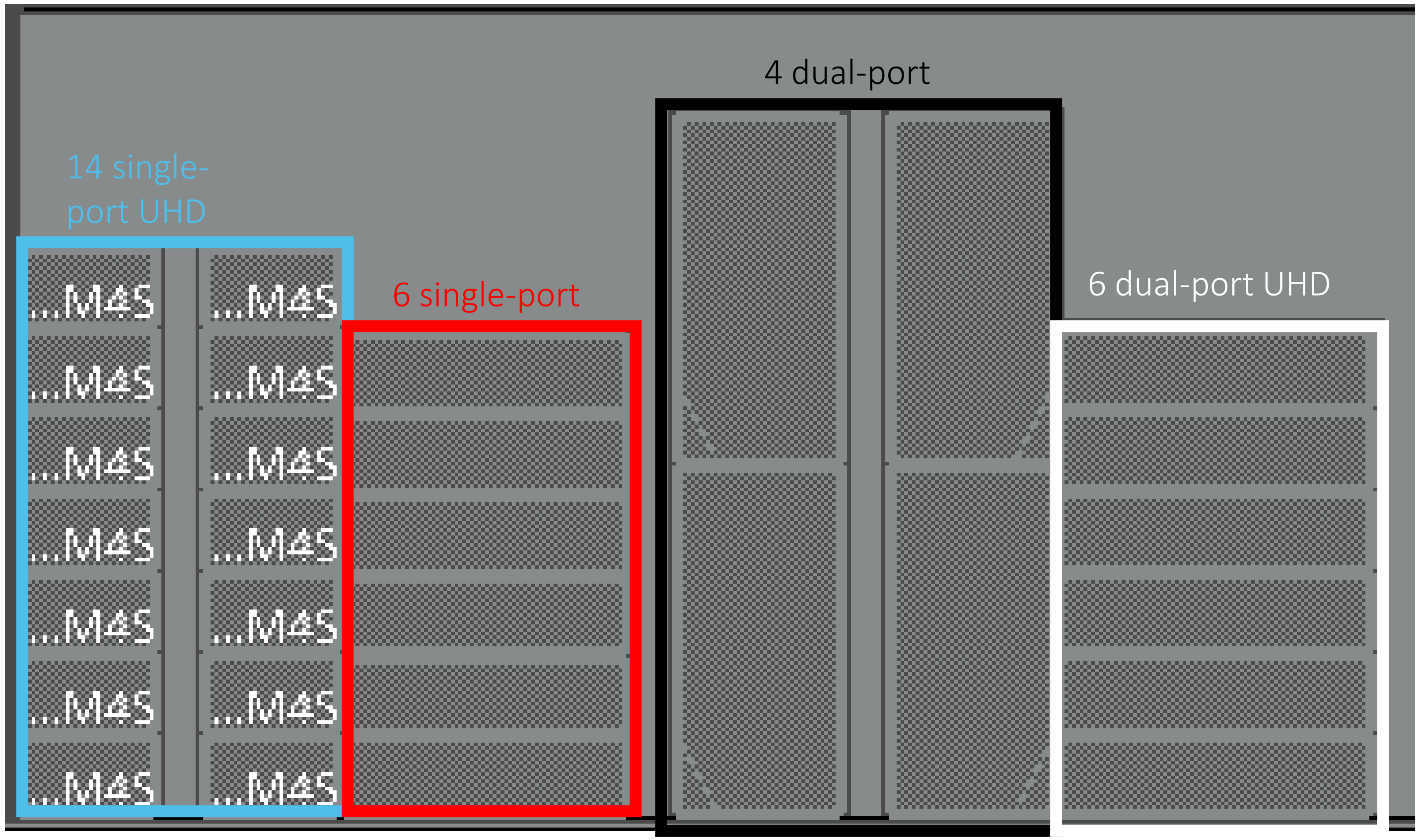
- 16 chains of inverters + vernier detector

} single-event-transient (SET)

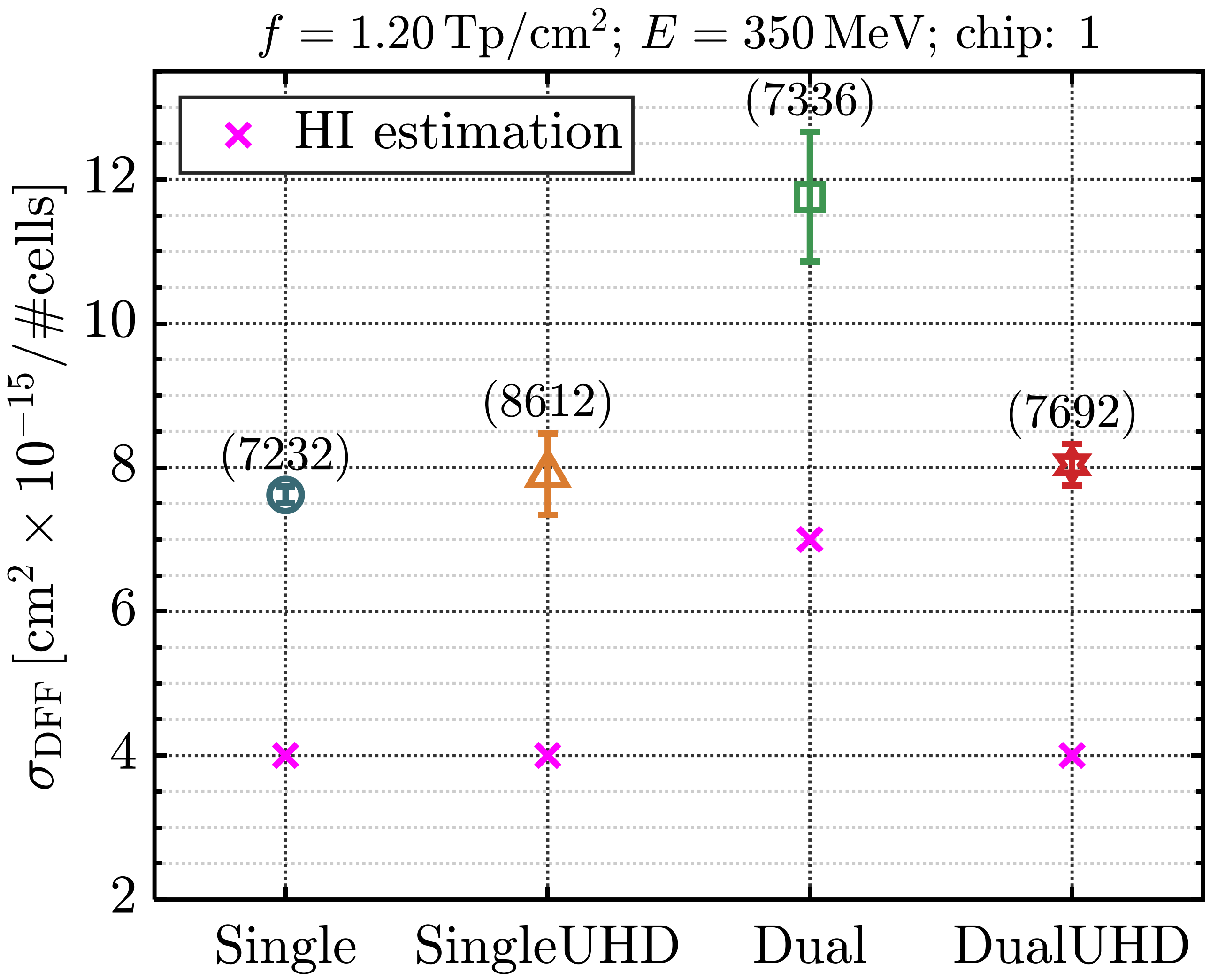
EXP28:SEE – SRAM



- **6** 4096x32b single-port
- **14** 2048x32b single-port UHD
- **4** 4096x32b dual-port
- **6** 4096x32b dual-port UHD

Total active area: 0.76 mm^2

EXP28:SEE – SRAM – σ – protons



same order of magnitude!

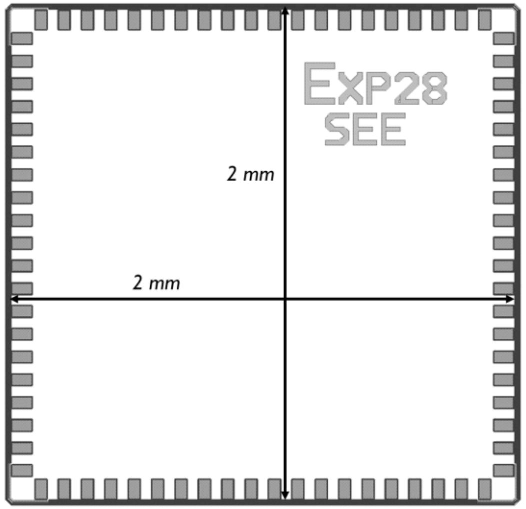
EXP28:SEE/ANA

D. Ceresa, G. Borghello, G. Bergamin, F. Piernas Diaz, R. Pejašinović, K. Kloukinas

- minimum distance between D-flip-flop to **avoid MBU**
- evaluation of a method to **predict SEEs rate in the accelerator environment using heavy-ion data**
- **pulse length of SET** for HI and protons
- sensitivity to **Single-Event-Latch-UP**

EXP28:SEE

SINGLE EVENT EFFECT (SEE)



3 test structures:

- 7 matrices of D-flip-flops
- 4 foundry SRAMs

single- and multi-bit-upsets (SBU, MBU)

- 16 chains of inverters + vernier detector

single-event-transient (SET)

EXP28:SEE – SET

VERNIER DELAY LINE TEST STRUCTURE :

Measure **cross-section for transient**

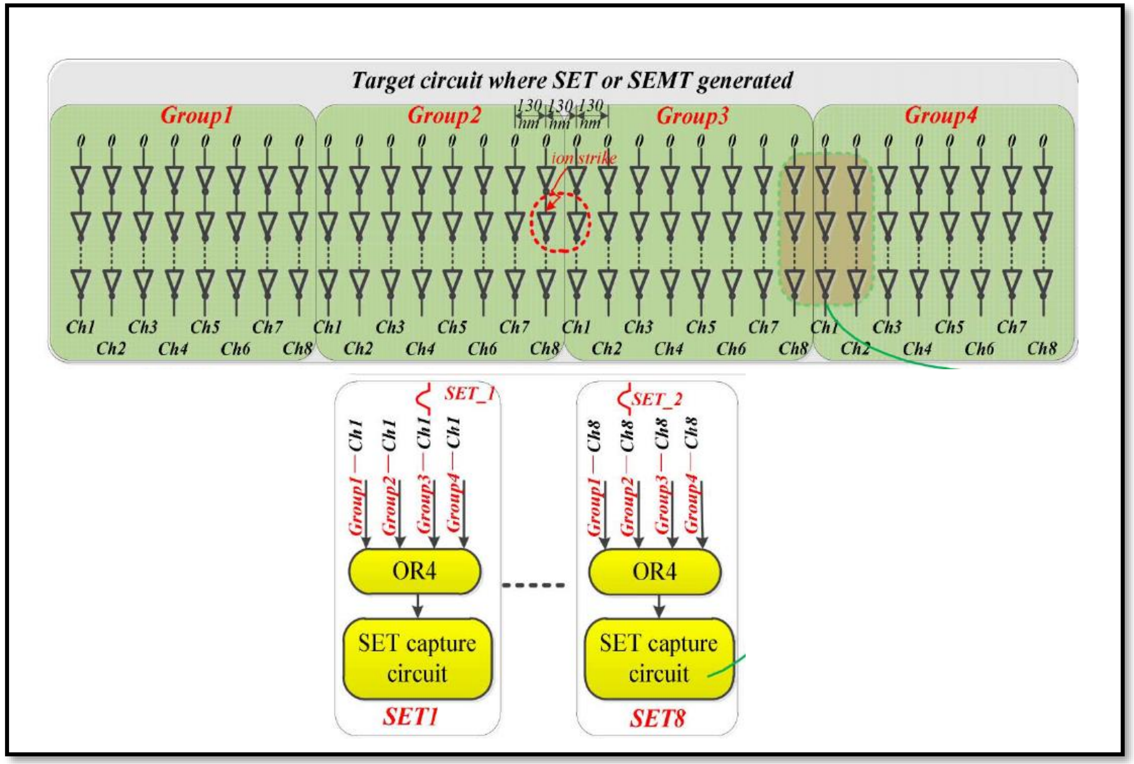
Estimate **transient length vs let**

Detect multiple-transient

Fully digital implementation

Fast readout through differential lines

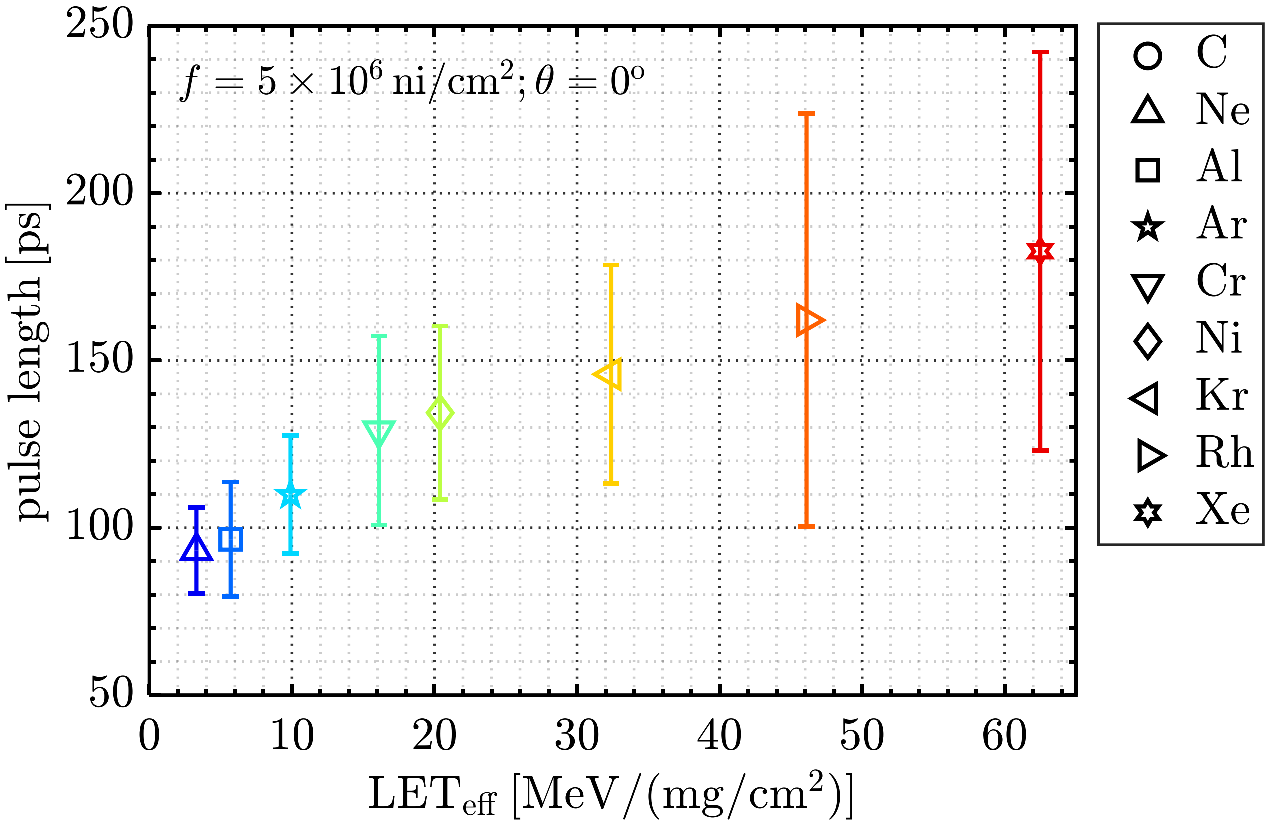
Sensitive area ~400 x 80 um2 with minimum size inverters

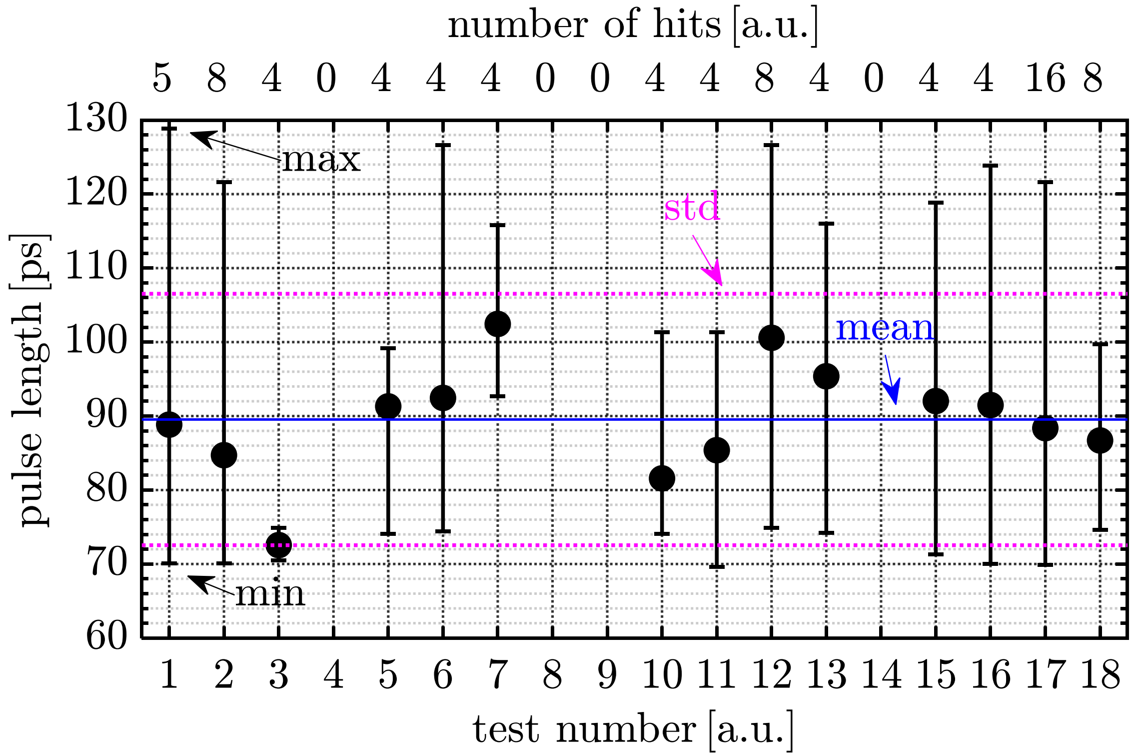


M. Glorieux et al., "Detailed SET Measurement and Characterization of a 65 nm Bulk Technology," in IEEE Transactions on Nuclear Science, vol. 64, no. 1, pp. 81-88, Jan. 2017, doi: 10.1109/TNS.2016.2637935.
P. Huang et Al, "Heavy-Ion-Induced Charge Sharing Measurement With a Novel Uniform Vertical Inverter Chains (UniVIC) SEMT Test Structure," in IEEE Transactions on Nuclear Science, vol. 62, no. 6, pp. 3330-3338, Dec. 2015

EXP28:SEE – SET – pulse length

heavy ions





protons

EXP28:SEE/ANA

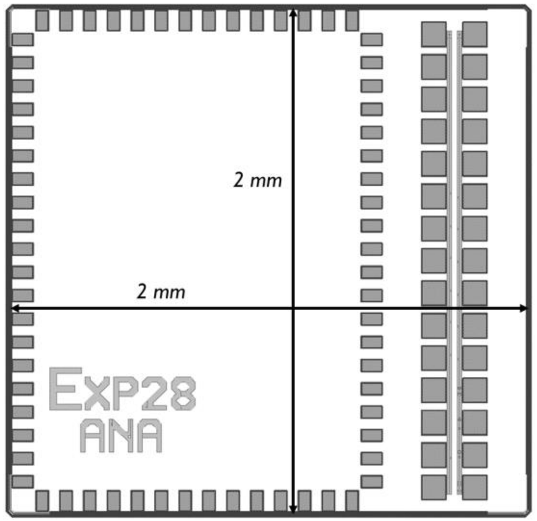
D. Ceresa, G. Borghello, G. Bergamin, F. Piernas Diaz, R. Pejašinović, K. Kloukinas

- minimum distance between D-flip-flop to **avoid MBU**
- evaluation of a method to **predict SEEs rate in the accelerator environment using heavy-ion data**
- sensitivity to **Single-Event-Latch-UP**

EXP28:ANA

Single-Event Latch-UP (SEL)

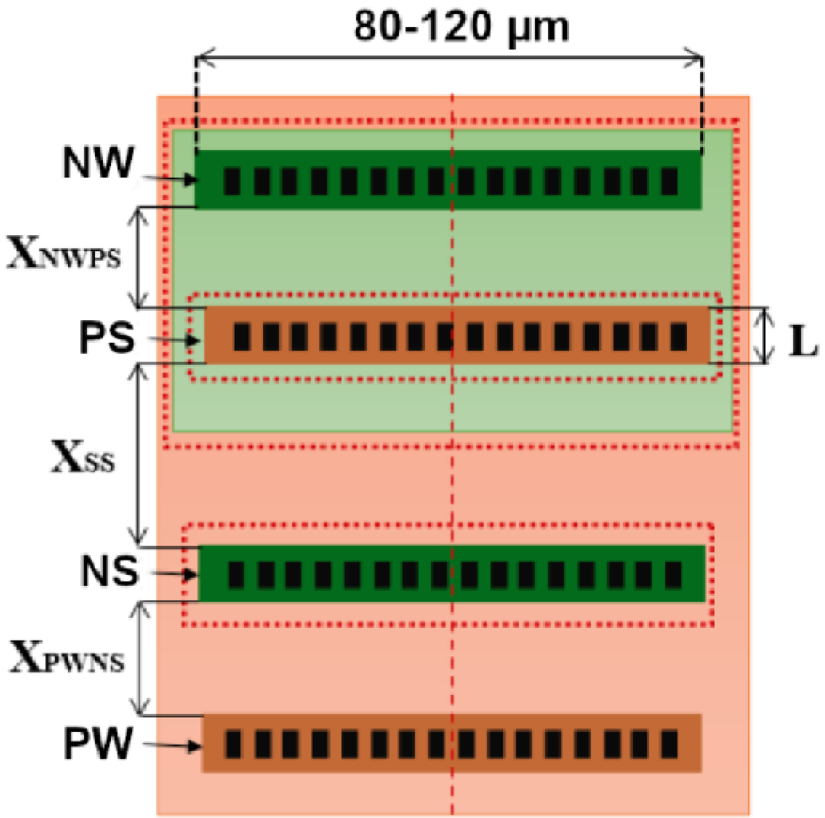
ANALOG IP BLOCKS



DESTRUCTIVE EVENTS (SEL)

SEL test structure

Letch-up sensitivity depends on doping levels (which cannot be changed) and distance between wells



40 structures with different combinations of X_{NWPS}, X_{SS}, X_{PWNS}

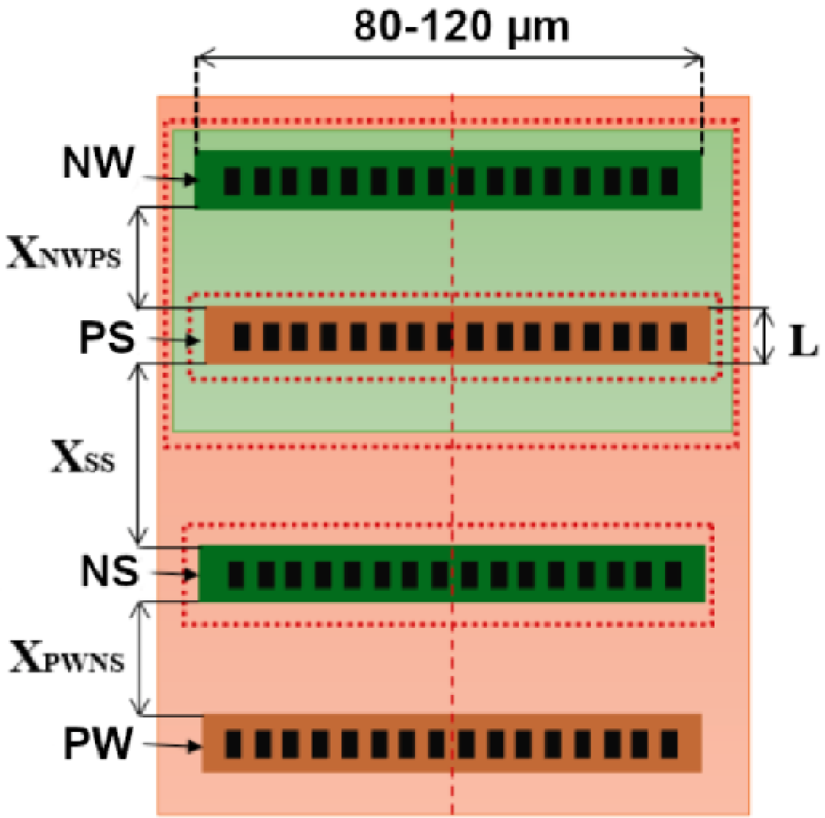
EXP28:ANA – HI

ion	angle [°]	LET [MeV/(mg/cm^2)]	fluence [10^6 ni/cm^2]	voltage
Ni	0	20.4	23.3	VDD (0.9 V)
Ni	45	28.85	16.2	VDD
Kr	45	45.82	11.4	VDD
Xe	0	62.5	51.6	VDD
Rh	45	65.2	11.4	VDD
Xe	45	88.39	6.2	VDD
Xe	45	88.39	45.0	1.15*VDD
Xe	75	241.48	1.72	1.15*VDD

high LET, high voltage

SEL test structure

Letch-up sensitivity depends on doping levels (which cannot be changed) and distance between wells



40 structures with different combinations of X_{NWPS}, X_{SS}, X_{PWNS}

No SEL
in any of the structures
for any for the tests!!!

CONCLUSIONS

D. Ceresa, G. Borghello, G. Bergamin, F. Piernas Diaz, R. Pejašinović, K. Kloukinas

first comprehensive overview of the SEE sensitivity of 28nm CMOS technology

- ✓ 5 µm distance to avoid MBU in DFF
- ✓ validation of model to estimate of proton cross section from HI tests
- ✓ SET pulse length for heavy-ions and protons
- ✓ no SEL for any structure/LET

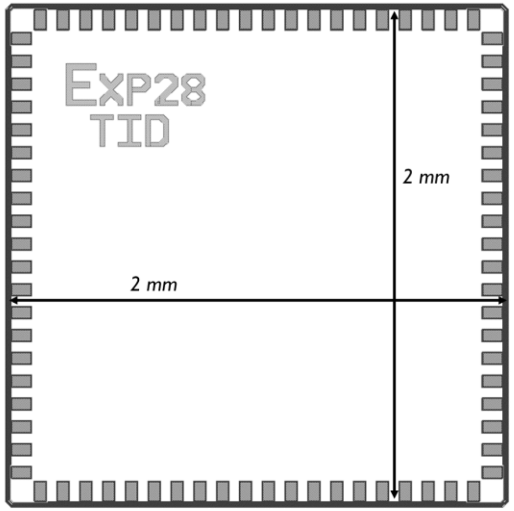
- \+ cross section of DFF and 4 foundry SRAMs for HI and protons
- \+ MBU probability of DFF and 4 foundry SRAMs for HI and protons
- \+ MBU evaluation of scrambled SRAM
- \+ cross section for SET with HI and protons
- \+ multi SET

EXTRA SLIDES

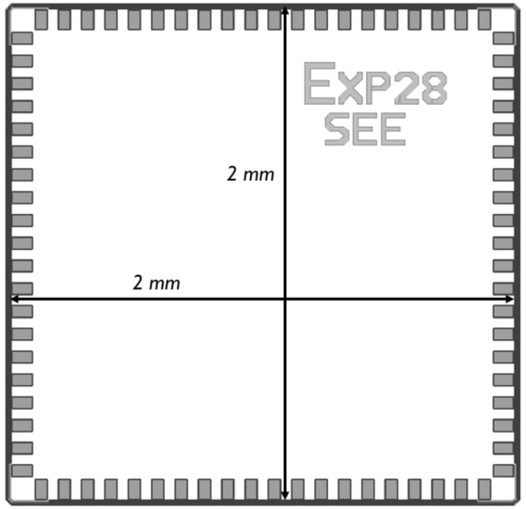
EXP28 CHIPS SUITE

D. Ceresa, G. Borghello, F. Piernas Diaz, R. Pejašinović, G. Bergamin, K. Kloukinas

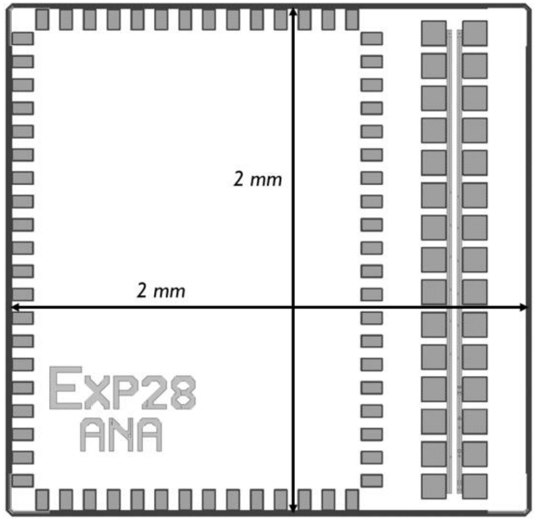
TOTAL IONIZING DOSE (TID)



SINGLE EVENT EFFECT (SEE)



ANALOG IP BLOCKS



chips received mid 2022

Goal:

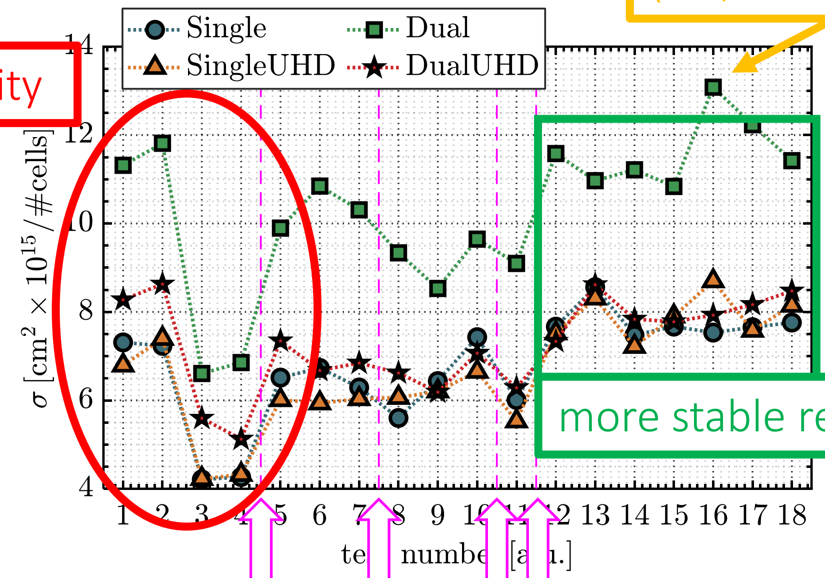
- experience the design flow
- characterize the 28nm CMOS technology
  - performance and radiation response

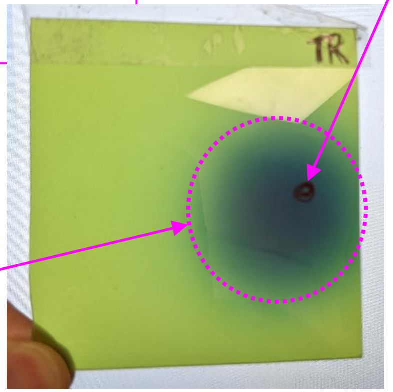
EXP28:SEE/ANA – PROTON TEST

1 (long) day beginning of December 2022

test n.	1	2	3	4	5	6	7
chip	A	A	A	A	B	B	B
energy [MeV]	480	480	480	480	480	480	480
fluence [$cm^{-2} \times 10^9$]	174	182	184	184	183	184	184
flux [$cm^{-2} \times 10^6/s$]	520	130	1300	1300	1300	1300	1300

test n.	8	9	10	11	12	13	14	15	16	17	18
chip	B	B	B	B	B	B	A	A	A	A	A
energy [MeV]	350	350	350	350	350	350	350	350	350	350	350
fluence [$cm^{-2} \times 10^9$]	90	183	183	184	184	90	184	184	64	385	385
flux [$cm^{-2} \times 10^6/s$]	256	256	640	640	640	128	640	640	128	640	640

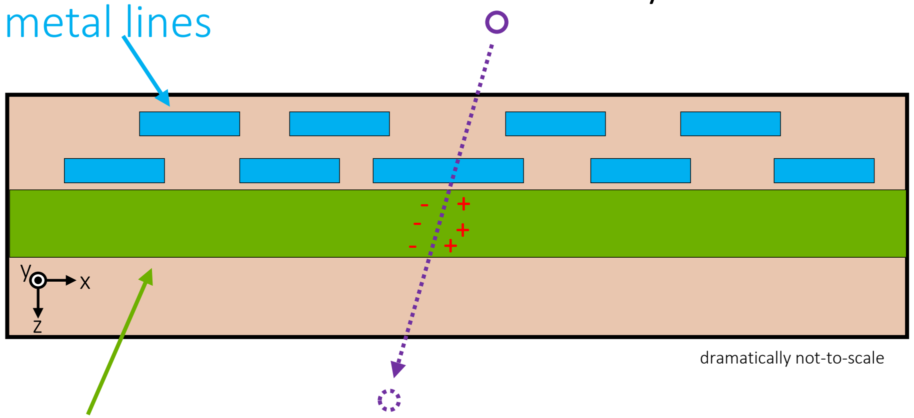


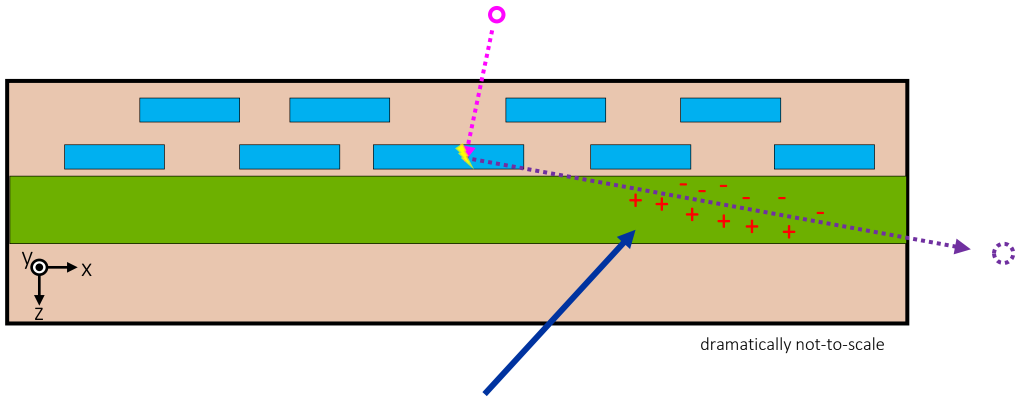


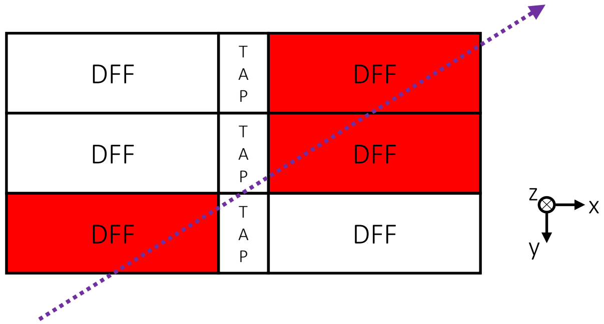
RADNEXT

(This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101008126.)

HI vs PROTONS





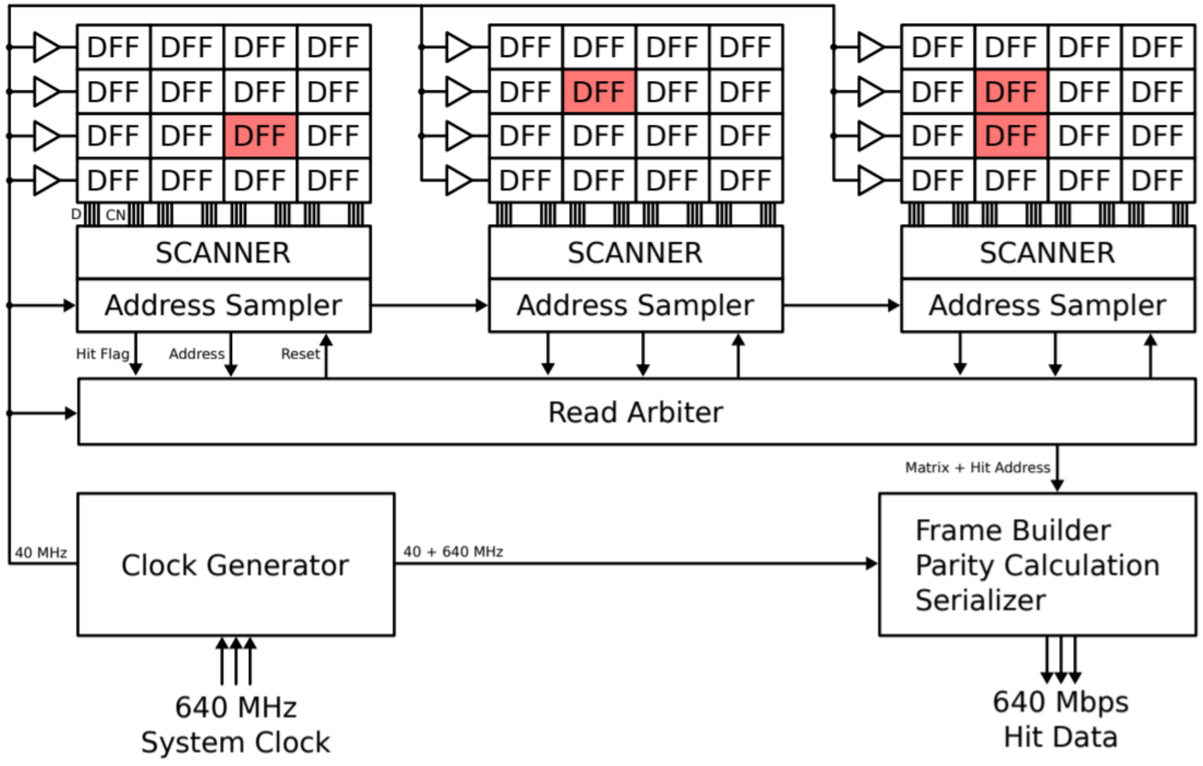


thanks Davide Ceresa for the slides!

EXP28 SEU: SINGLE EVENT UPSET ON SEQUENTIAL ELEMENTS

Test structure derived from a multi-bit upsets test structure in 65nm (Stefan Biereigel, https://indico.cern.ch/event/959655)

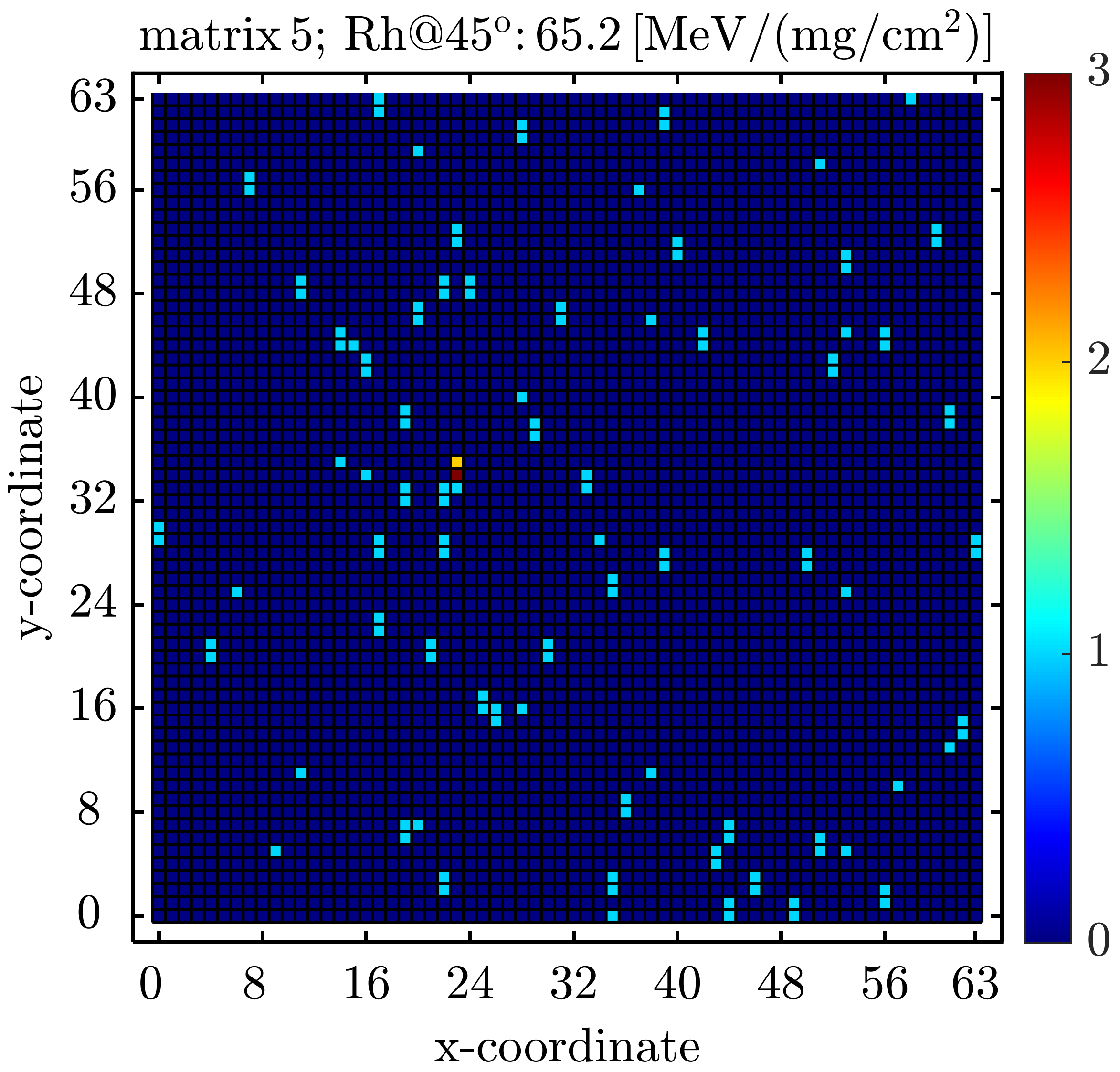
- 7 matrices of 4096 DFF continuously clocked, D tied to Q.
- 9 tracks, different flavors.



Rad-Hard data processing and readout.

- 1 input line for clock (640MHz).
- 1 output line for data (16-bits packet at 640MHz).
- SEU detected – readout – FF reset.
- In case of MSEU, an arbiter ensures priority.

EXP28:SEE – DFF – cross section (σ)

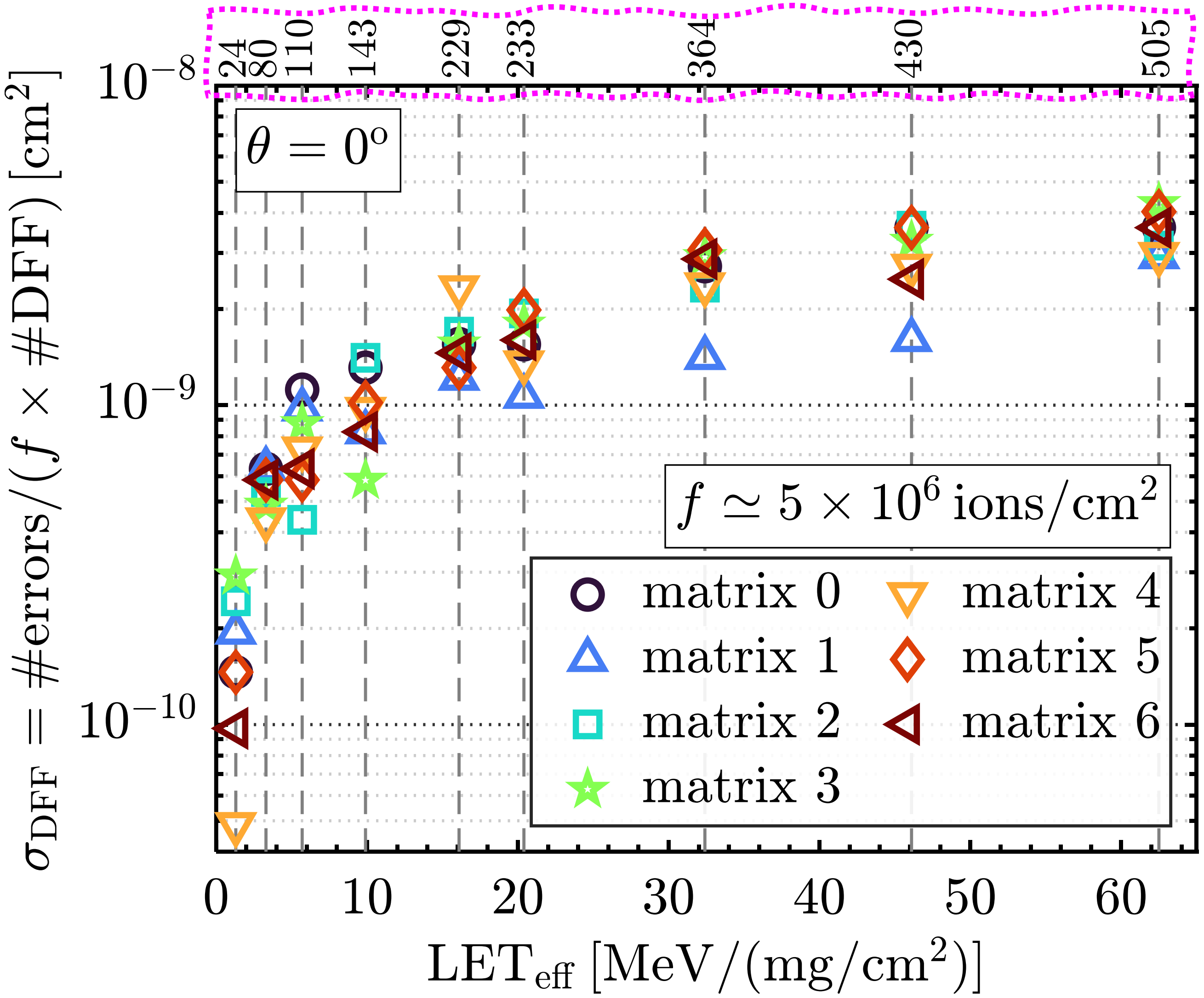


cross-section σ_{DFF} [cm^2] = (#errors/#DFF in matrix)/fluence

64x64 = 4096

EXP28:SEE – DFF – σ – HI

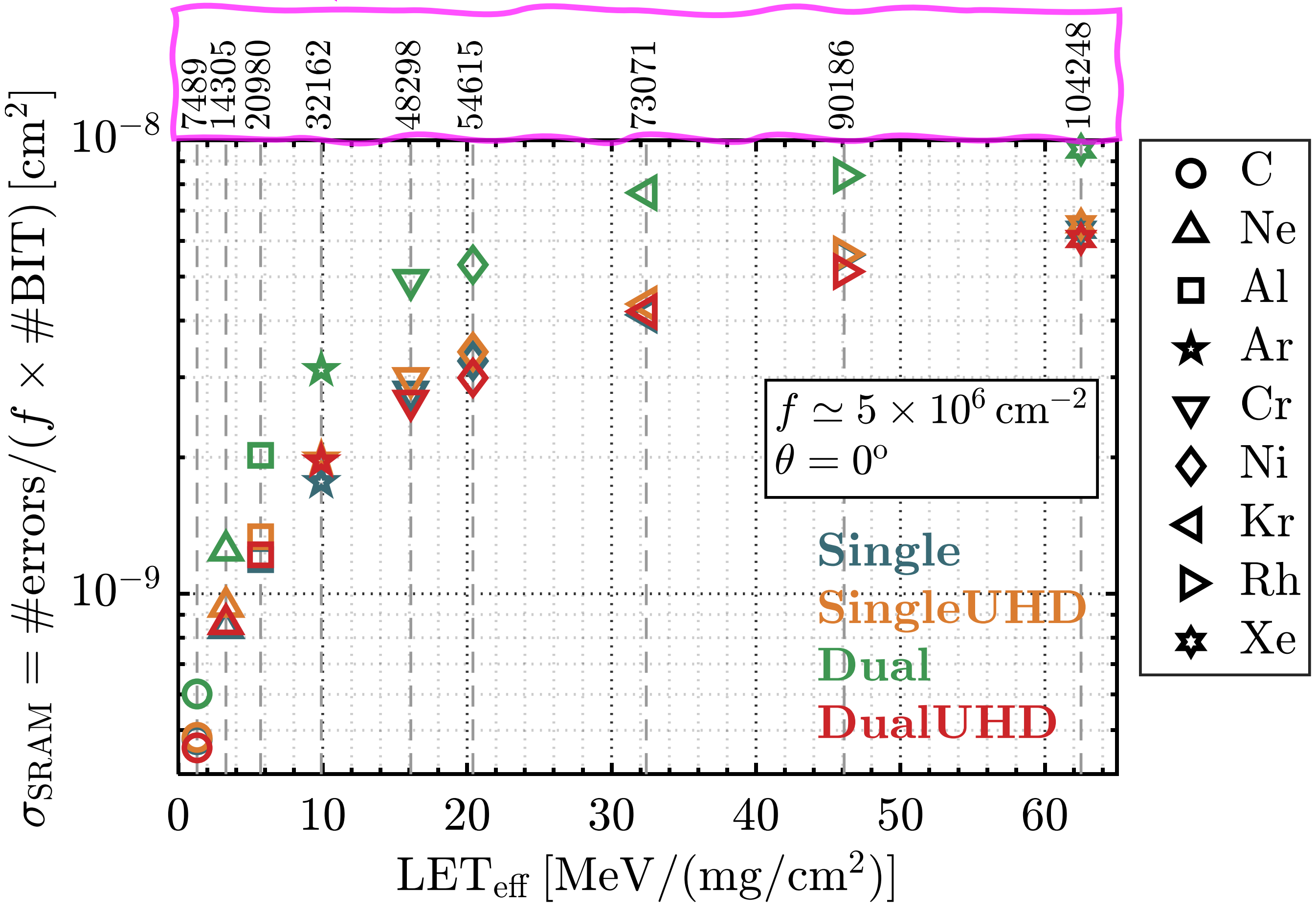
total number of errors



cross-section σ_{DFF} [cm^2] = (#errors/#DFF in matrix)/fluence

EXP28:SEE – SRAM – σ – HI

much larger statistics than DFF

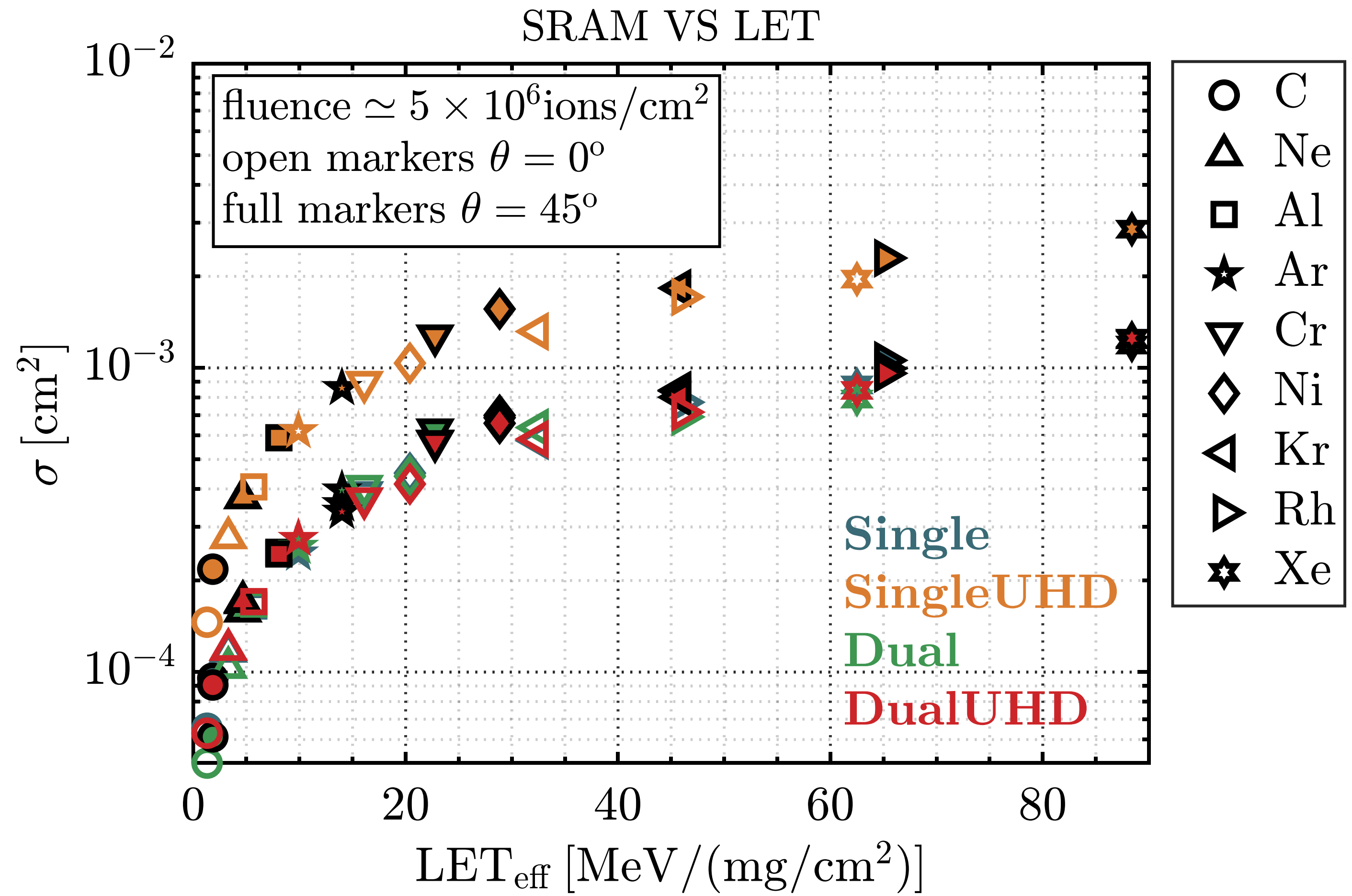


Dual SRAM has a slightly higher cross-section

larger cells in dual SRAM
-> larger sensitive area

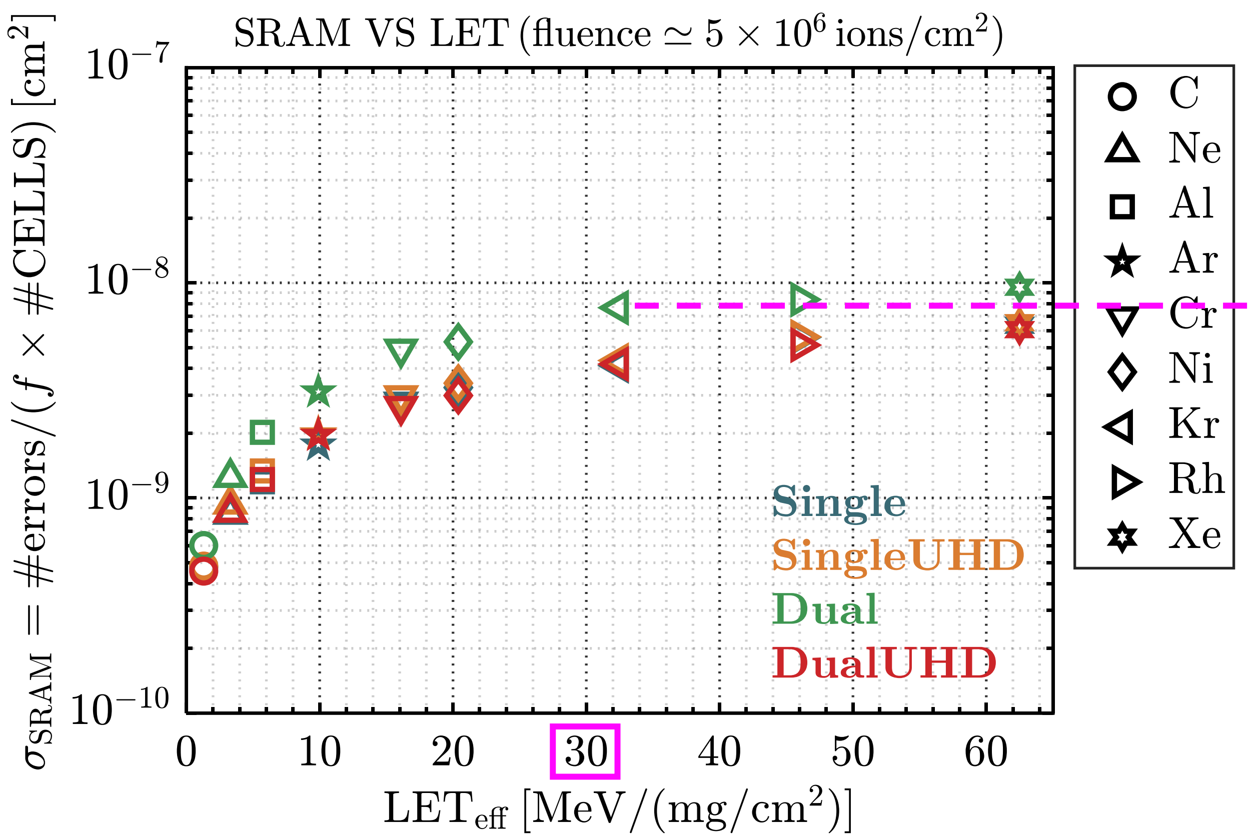
BITCELL transistor dimensions

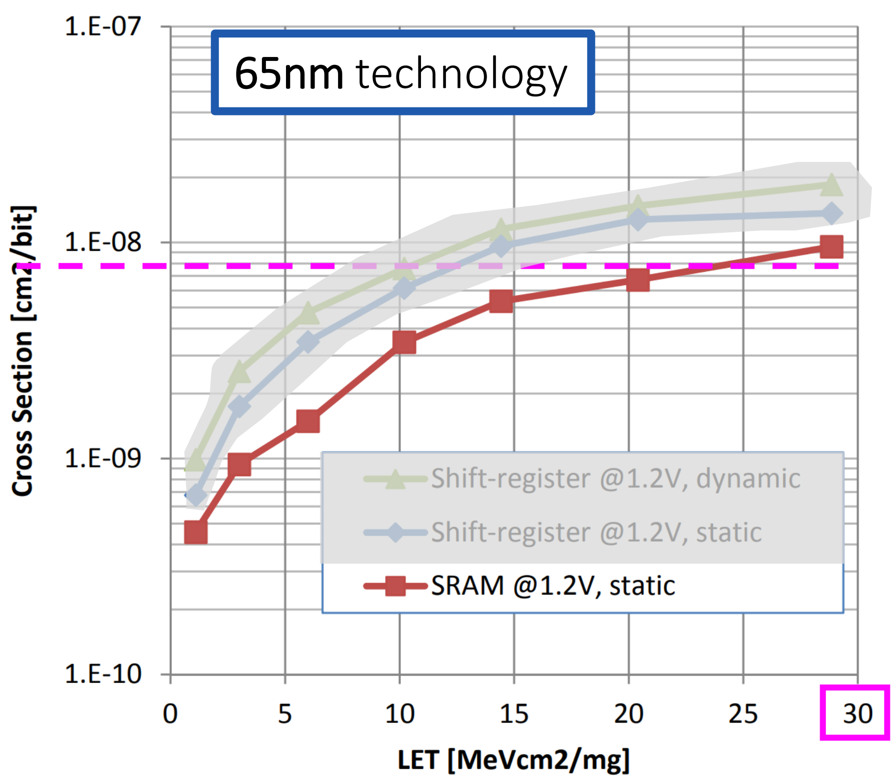
SINGLE PORT (L,W,M) 6T	nchpd_sr	nchpg_sr	pchpu_sr
S1BHVTSWBASO100W10_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVTSWBASO100W10_TKBL_BCELL_SD	35 95 1	35 65 1	35 40 1
S1BHVTSWBASO100W10_TKBL_EDGE_SD	35 95 1	35 65 1	35 40 1
DUAL PORT (L,W,M) 8T	**pchpu_dpsr (2)**	**nchpd_dpsr(4)**	**nchpg_dpsr (4)**
SDMWBASO100W10_MCB	35 50 1	35 195 1	35 140 1
SDMWBASO100W10_TKBL	35 50 1	35 195 1	35 140 1
SDMWBASO100W10_TKNOR	35 50 1	35 195 1	35 140 1
ULTRA HIGH DENSITY SINGLE PORT (L,W,M) 6T	**nchpd_sr**	**nchpg_sr**	**pchpu_sr**
S1BUHDHVTSWBSO100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
S1BUHDHVTSWBSO100W10_MCB	35 95 1	35 65 1	35 40 1
S1BUHDHVTSWBSO100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
ULTRA HIGH DENSITY DUAL PORT (L,W,M) 6T	**nchpd_sr**	**nchpg_sr**	**pchpu_sr**
SDBMWA100W10_TKBL_EDGE	35 95 1	35 65 1	35 40 1
SDBMWA100W10_TKBL_BCELL	35 95 1	35 65 1	35 40 1
SDBMWA100W10_MCB_TKWL_ISO	35 95 1	35 65 1	35 40 1
SDBMWA100W10_MCB_TKWL	35 95 1	35 65 1	35 40 1
SDBMWA100W10_MCB	35 95 1	35 65 1	35 40 1



SRAM VS LET
fluence ≃ 5 × 10^6 ions/cm^2
open markers θ = 0°
full markers θ = 45°
Single
SingleUHD
Dual
DualUHD
C
Ne
Al
Ar
Cr
Ni
Kr
Rh
Xe
σ [cm^2]
LET_eff [MeV/(mg/cm^2)]
10^-2
10^-3
10^-4
0
20
40
60
80

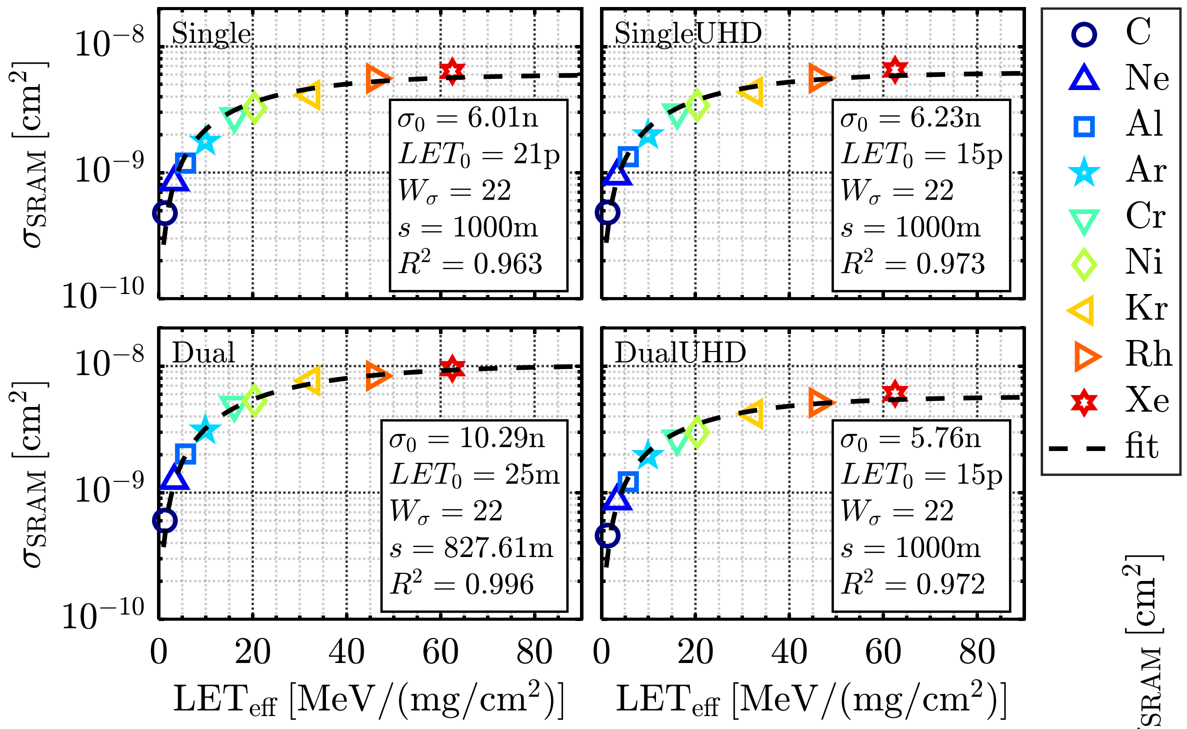
EXP28:SEE – SRAM – cross section - HI



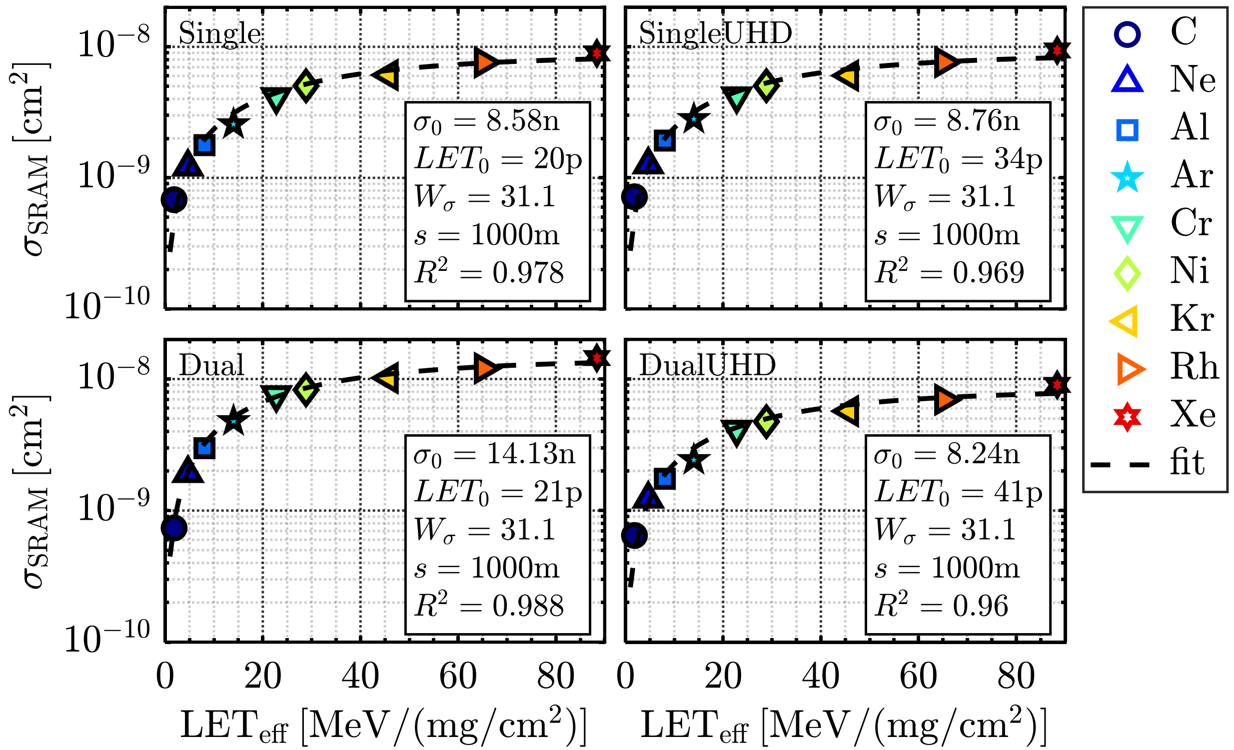


Bonacini, S., et al. "Characterization of a commercial 65 nm CMOS technology for SLHC applications." *Journal of Instrumentation* 7.01 (2012): P01015.

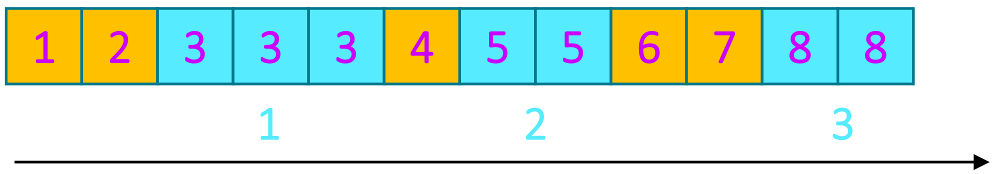
comparable or slightly better than 65nm



Single
SingleUHD
Dual
DualUHD
$\sigma_0 = 6.01$n
$LET_0 = 21$p
$W_\sigma = 22$
$s = 1000$m
$R^2 = 0.963$
$\sigma_0 = 6.23$n
$LET_0 = 15$p
$W_\sigma = 22$
$s = 1000$m
$R^2 = 0.973$
$\sigma_0 = 10.29$n
$LET_0 = 25$m
$W_\sigma = 22$
$s = 827.61$m
$R^2 = 0.996$
$\sigma_0 = 5.76$n
$LET_0 = 15$p
$W_\sigma = 22$
$s = 1000$m
$R^2 = 0.972$
σ_{SRAM} [cm^2]
10^{-8}
10^{-9}
10^{-10}
0 20 40 60 80
$\mathrm{LET_{eff}}$ [MeV/(mg/cm^2)]
C
Ne
Al
Ar
Cr
Ni
Kr
Rh
Xe
fit



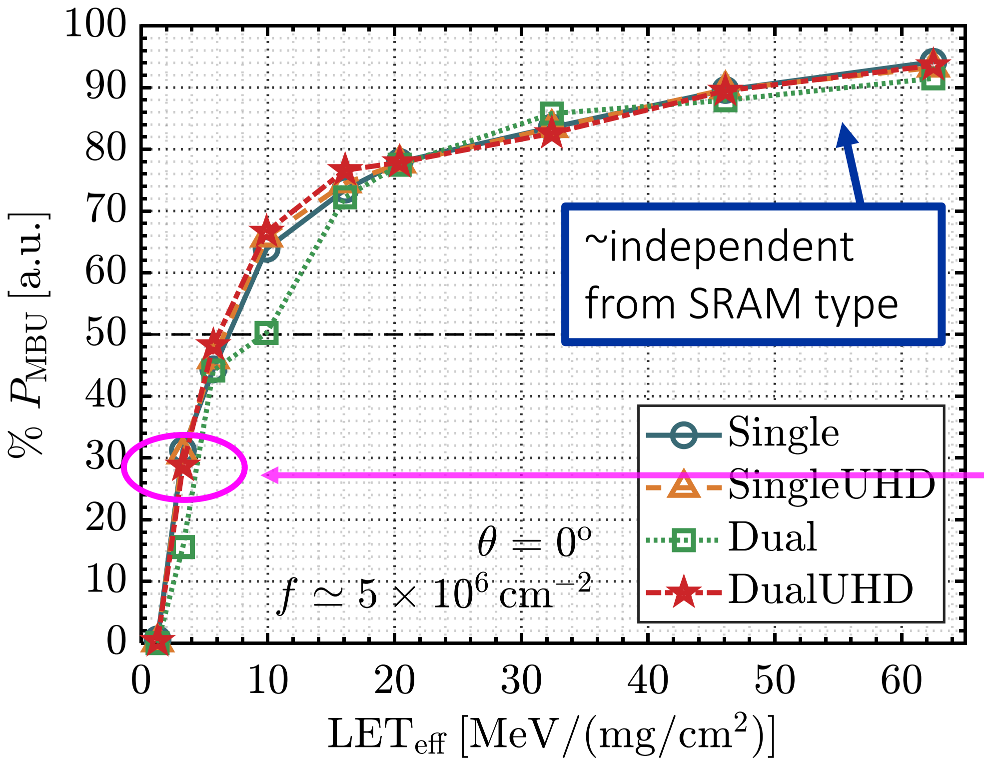
Single
SingleUHD
Dual
DualUHD
$\sigma_0 = 8.58$n
$LET_0 = 20$p
$W_\sigma = 31.1$
$s = 1000$m
$R^2 = 0.978$
$\sigma_0 = 8.76$n
$LET_0 = 34$p
$W_\sigma = 31.1$
$s = 1000$m
$R^2 = 0.969$
$\sigma_0 = 14.13$n
$LET_0 = 21$p
$W_\sigma = 31.1$
$s = 1000$m
$R^2 = 0.988$
$\sigma_0 = 8.24$n
$LET_0 = 41$p
$W_\sigma = 31.1$
$s = 1000$m
$R^2 = 0.96$
σ_{SRAM} [cm^2]
10^{-8}
10^{-9}
10^{-10}
0 20 40 60 80
$\mathrm{LET_{eff}}$ [MeV/(mg/cm^2)]
C
Ne
Al
Ar
Cr
Ni
Kr
Rh
Xe
fit



3 MBU/8 HITS = 37.5% : probability that a particle triggers an MBU (P_{MBU})

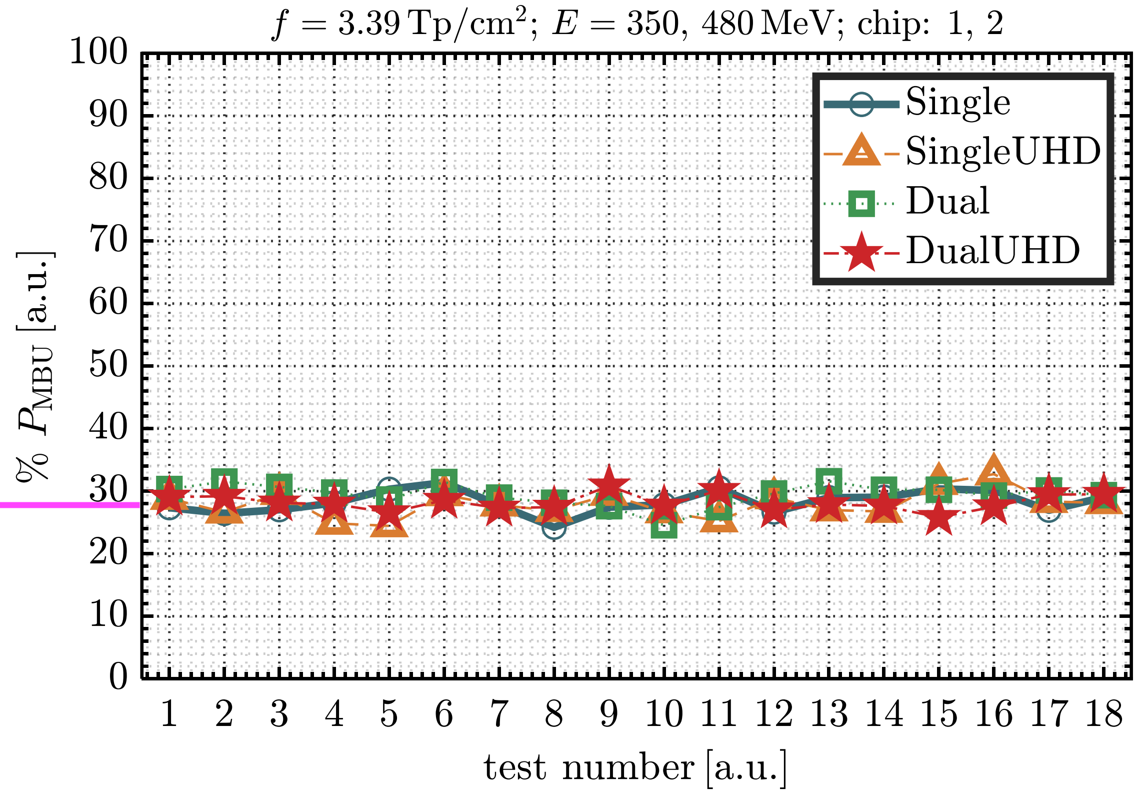
EXP28:SEE – SRAM – MBU

heavy-ions



errors dominated by
MBUs for LET > ~6 MeV/(mg/cm^2)

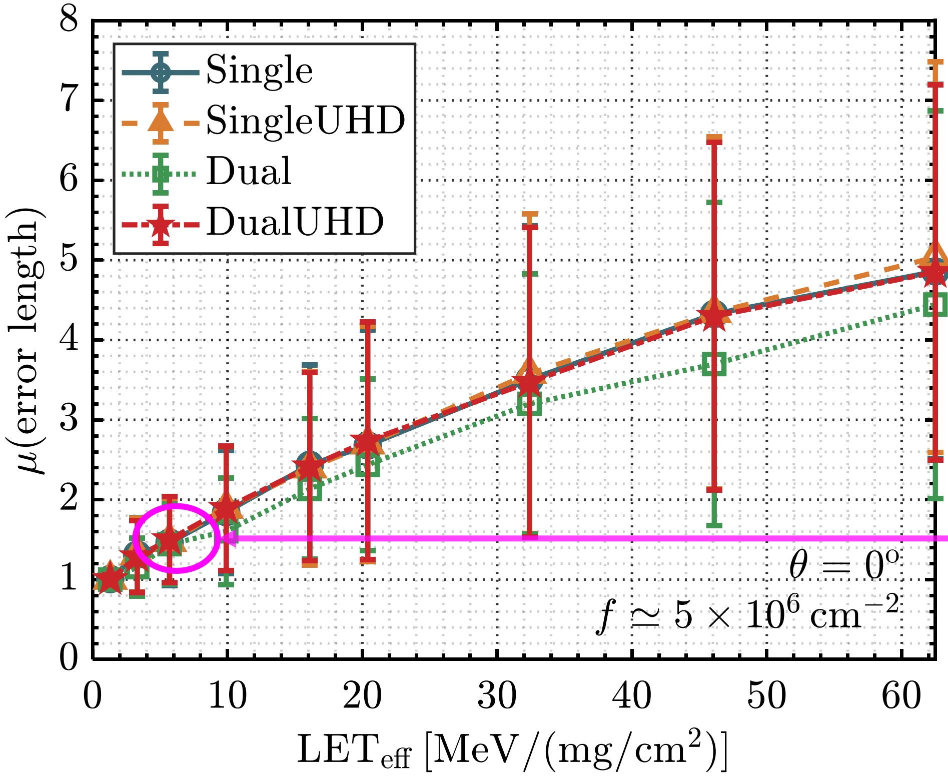
protons



similar to HI @ 3.3 MeV/(mg/cm^2)
(independent form SRAM type)

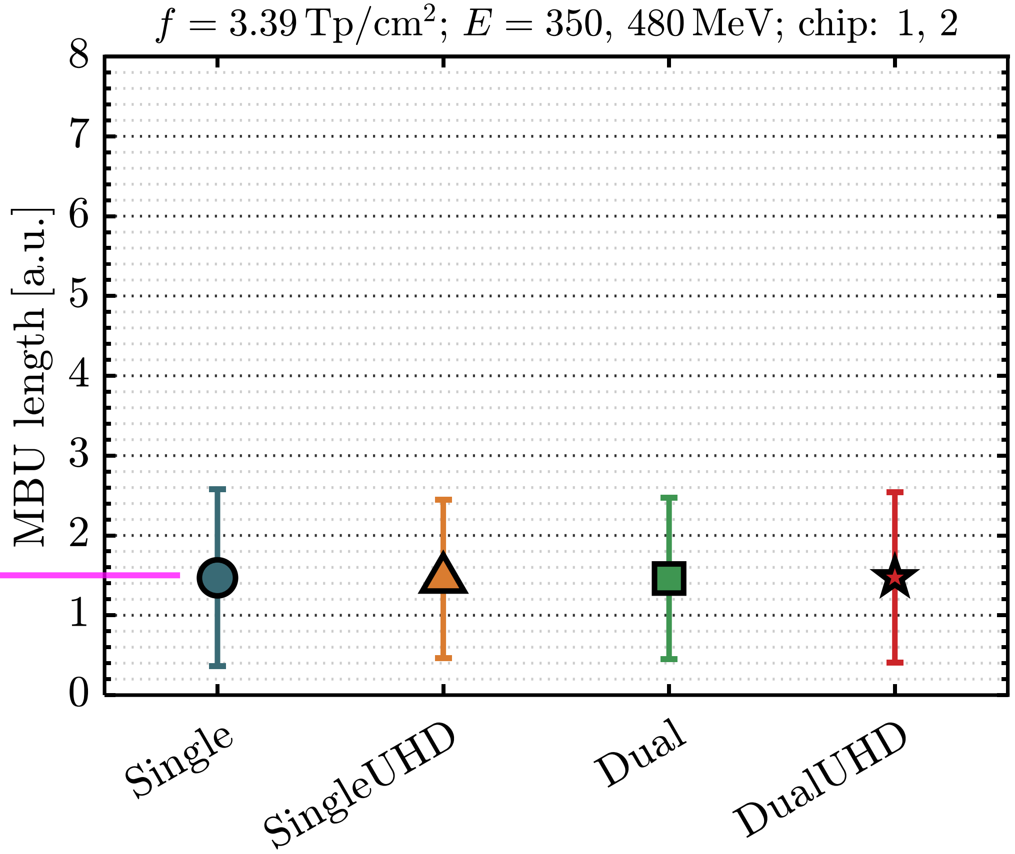
EXP28:SEE – SRAM – MBU

heavy-ions



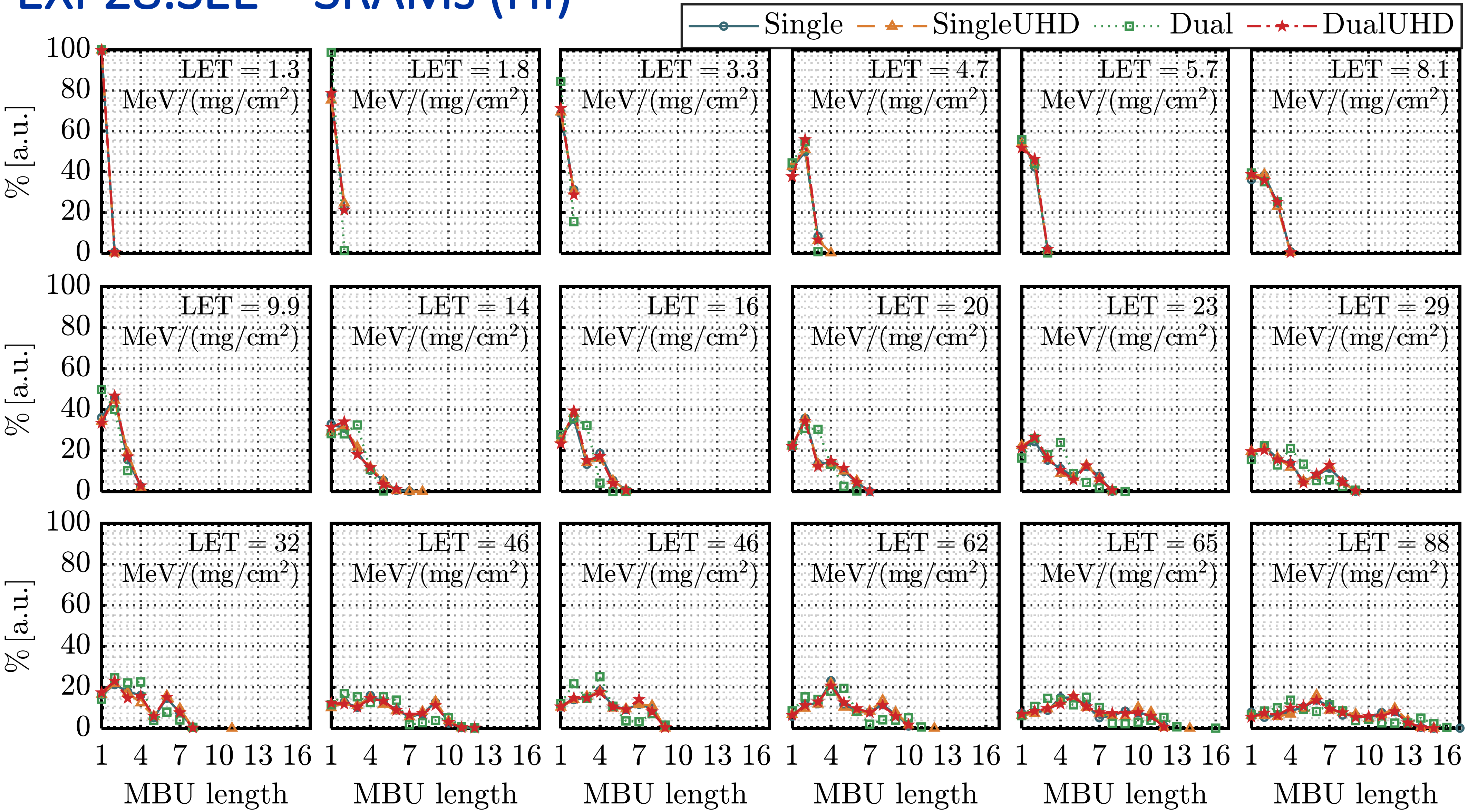
MBU length increases with LET

protons



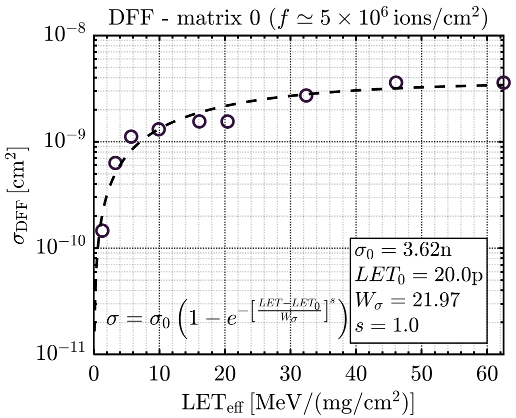
similar to HI @ 5.7 MeV/(mg/cm^2)

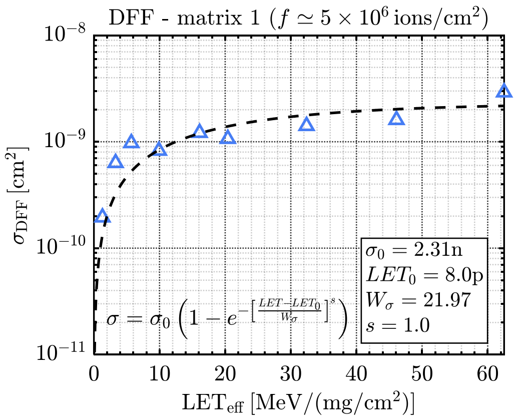
EXP28:SEE – SRAMs (HI)

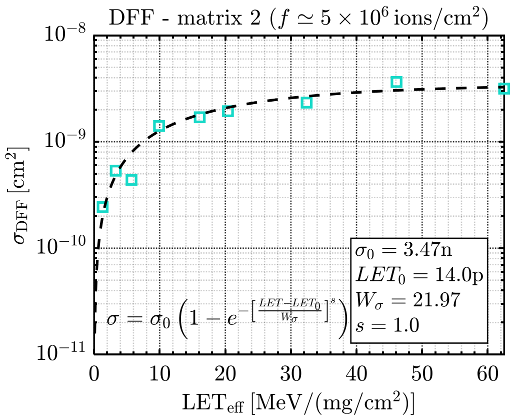


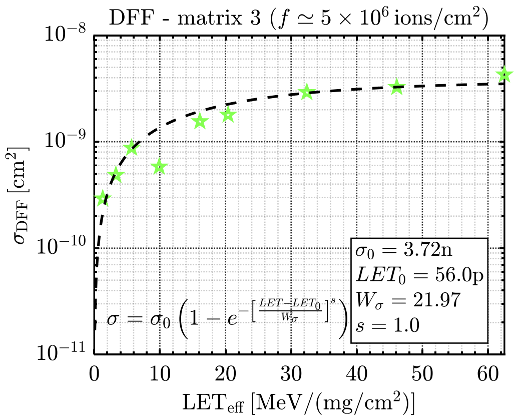
EXP28:SEE – DFF – σ – HI

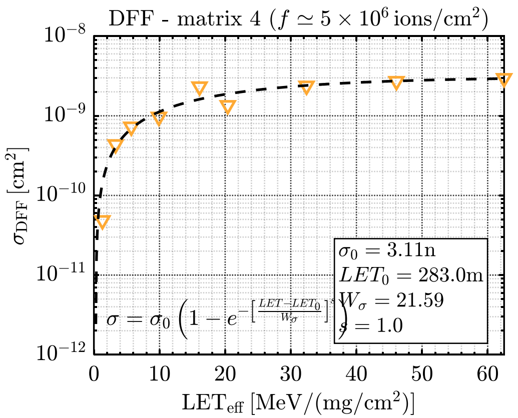
form HI to representative environment → Weibull fit → $\sigma = \boldsymbol{\sigma_0}\left(1 - e^{-\left[\frac{LET - LET_0}{W_\sigma}\right]^{s}}\right)$

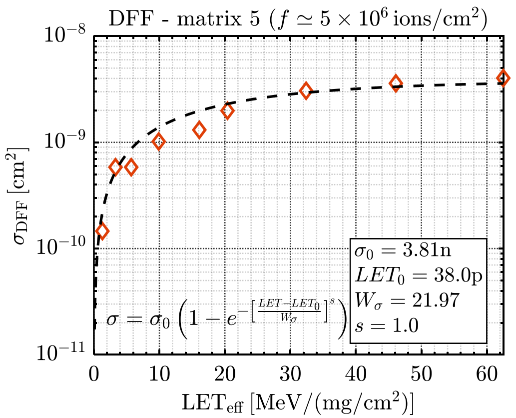


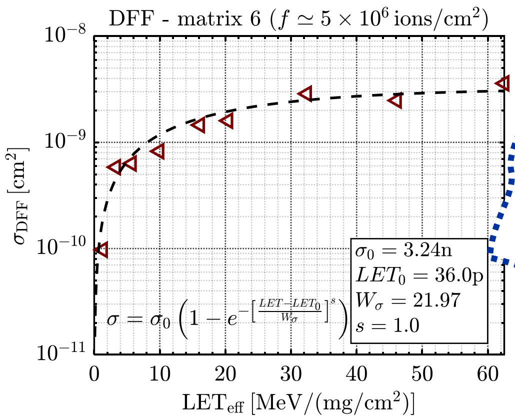








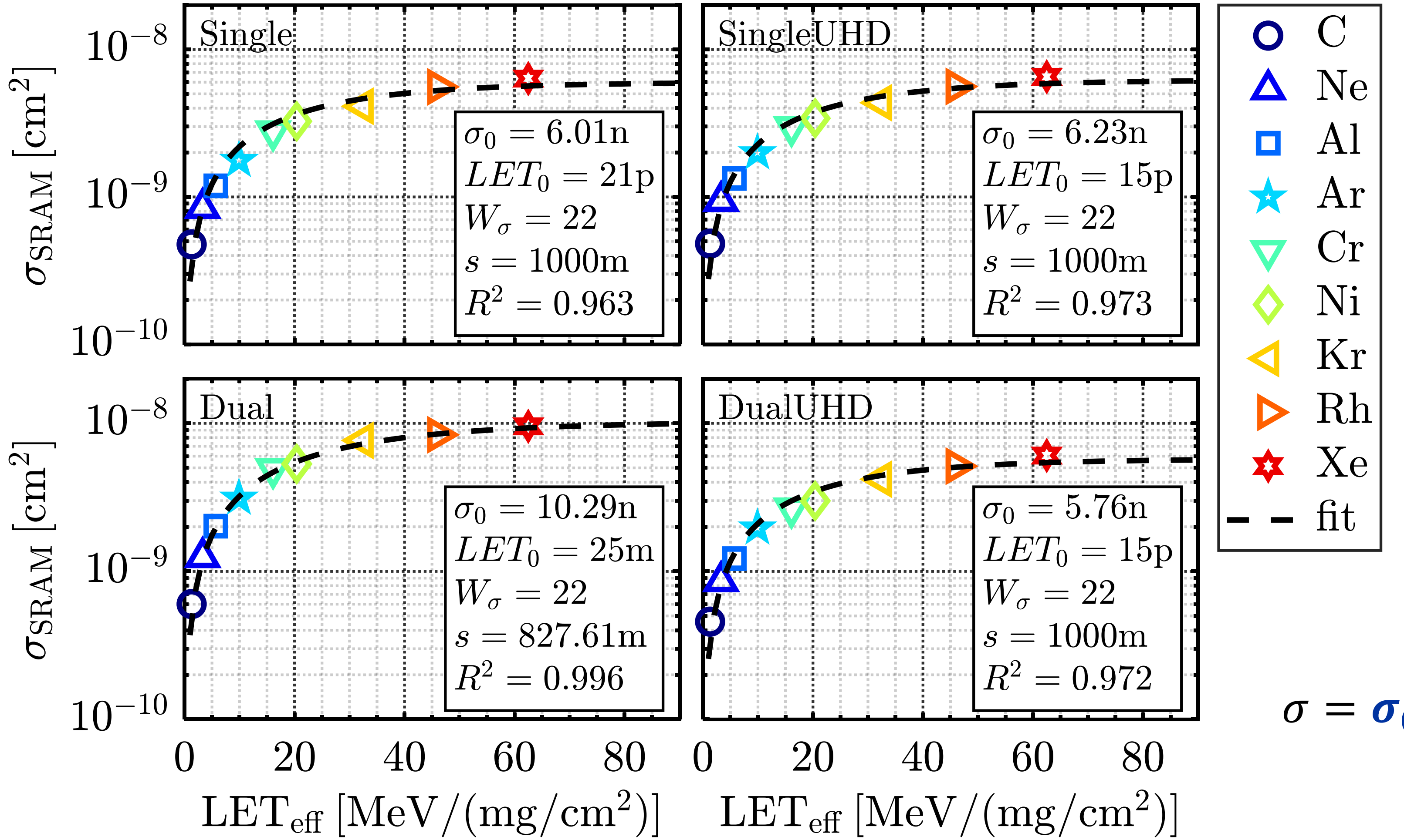




Huhtinen, M., and F. Faccio. "Computational method to estimate Single Event Upset rates in an accelerator environment." NIMA 450.1 (2000): 155-172.

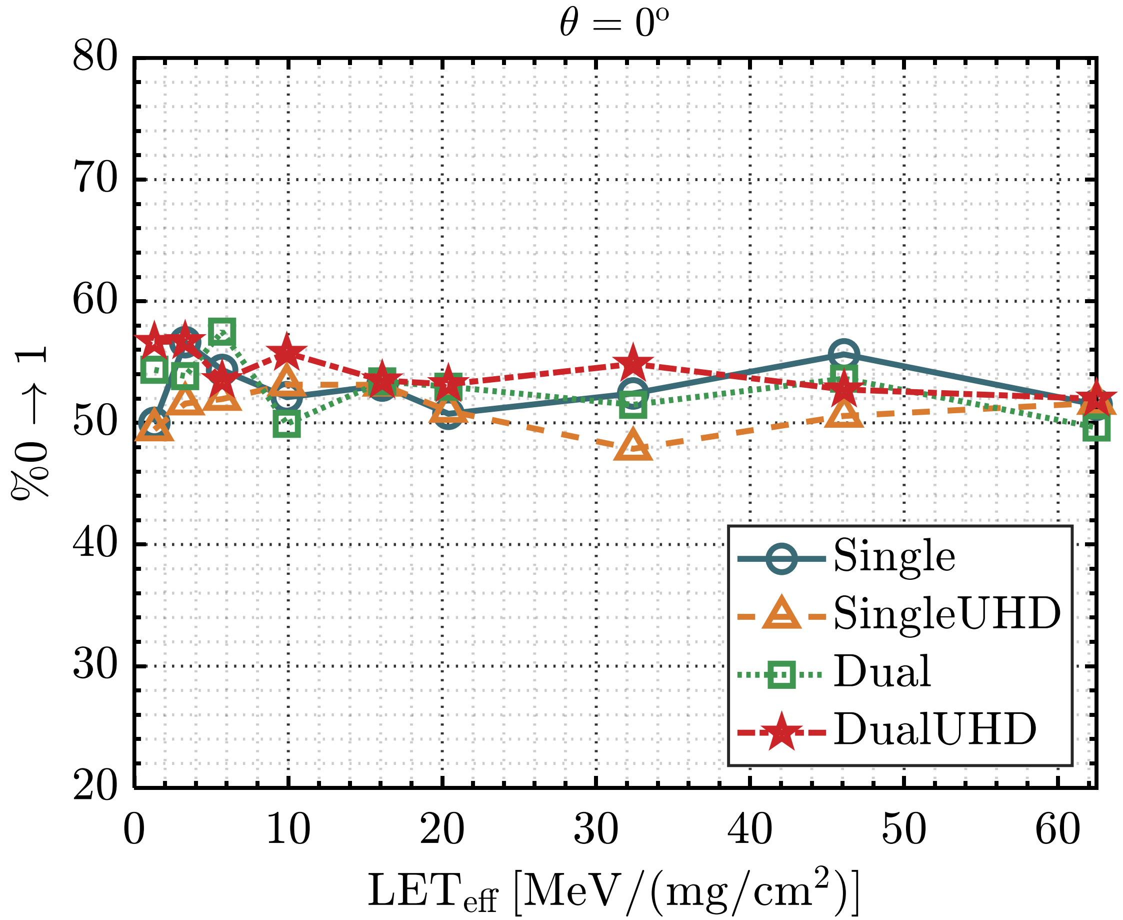
EXP28:SEE – SRAM – σ – HI

Weibull fit



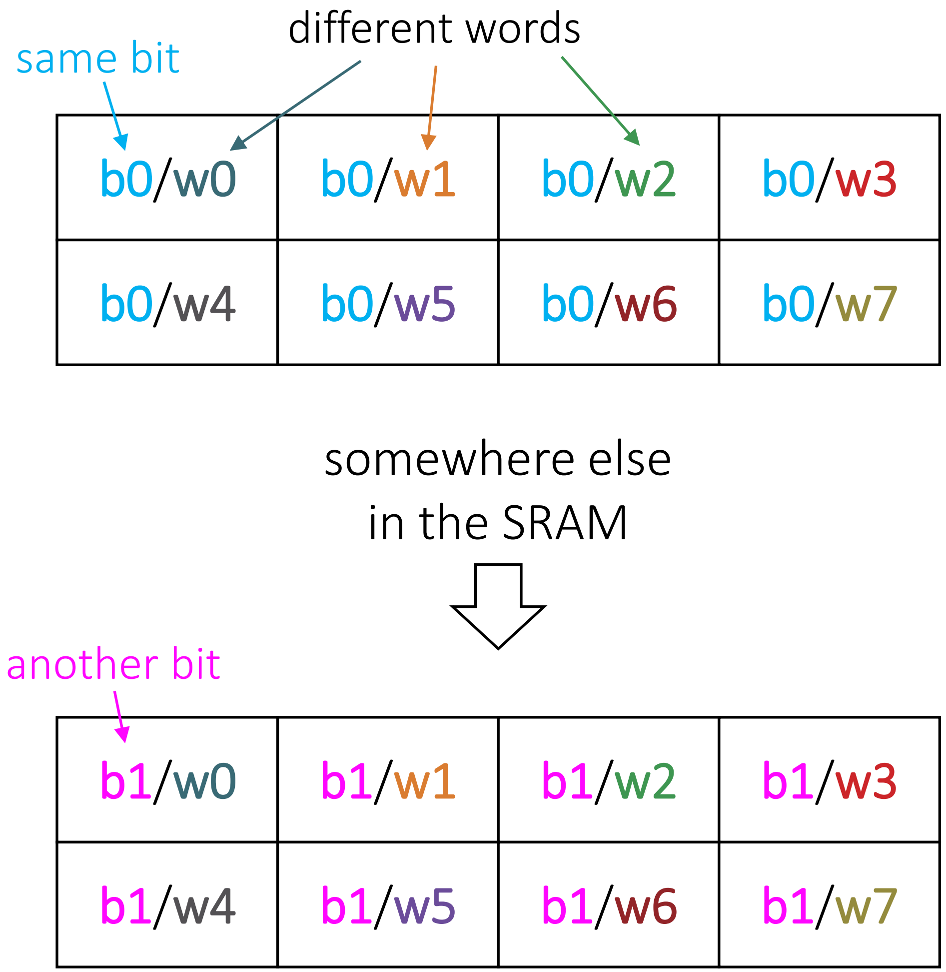
$$\sigma = \boldsymbol{\sigma_0}\left(1 - e^{-\left[\frac{LET - \boldsymbol{LET_0}}{\boldsymbol{W_\sigma}}\right]^{\boldsymbol{s}}}\right)$$

EXP28:SEE – SRAMs (HI)



~ independent of bit value

EXP28:SEE – SRAM – MBU



scrambled address:
32-world bits scrambled around the SRAM

bits of the same world physically separated

⇩

difficult to have multi-bits-upset on the same word

EXP28:SEE – SRAM – MBU

same bit/different words

b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7

MBU type A

different bits/different words

b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7
b*N*/w8	b*N*/w9	b*N*/w10	b*N*/w11

MBU type B

different bits/same word

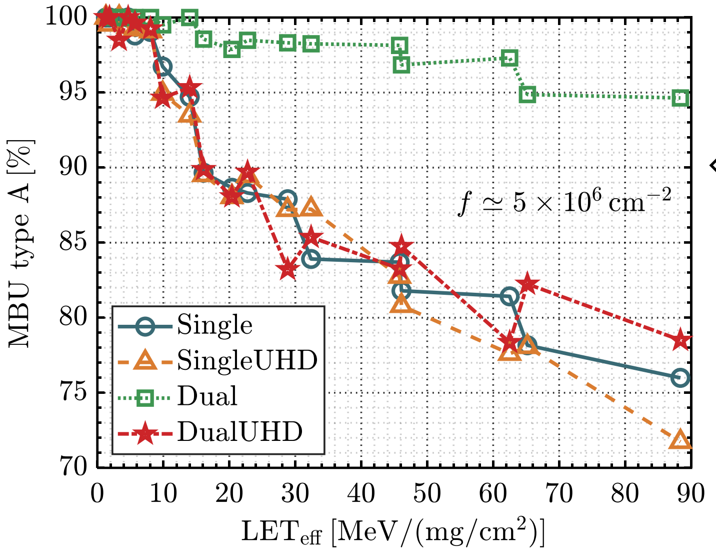
b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7

...

b1/w0	b1/w1	b1/w2	b1/w3

MBU type C

EXP28:SEE – SRAM – MBU – HI



same bit/different words

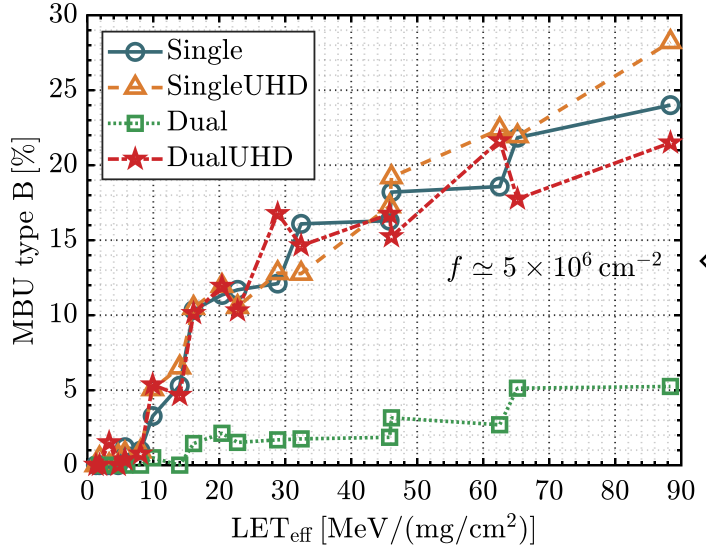
b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7

different bits/same word

b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7

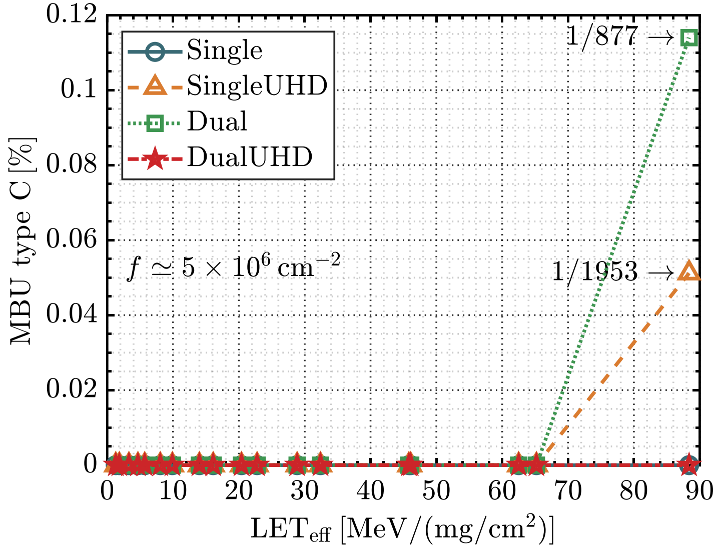
...

b1/w0	b1/w1	b1/w2	b1/w3

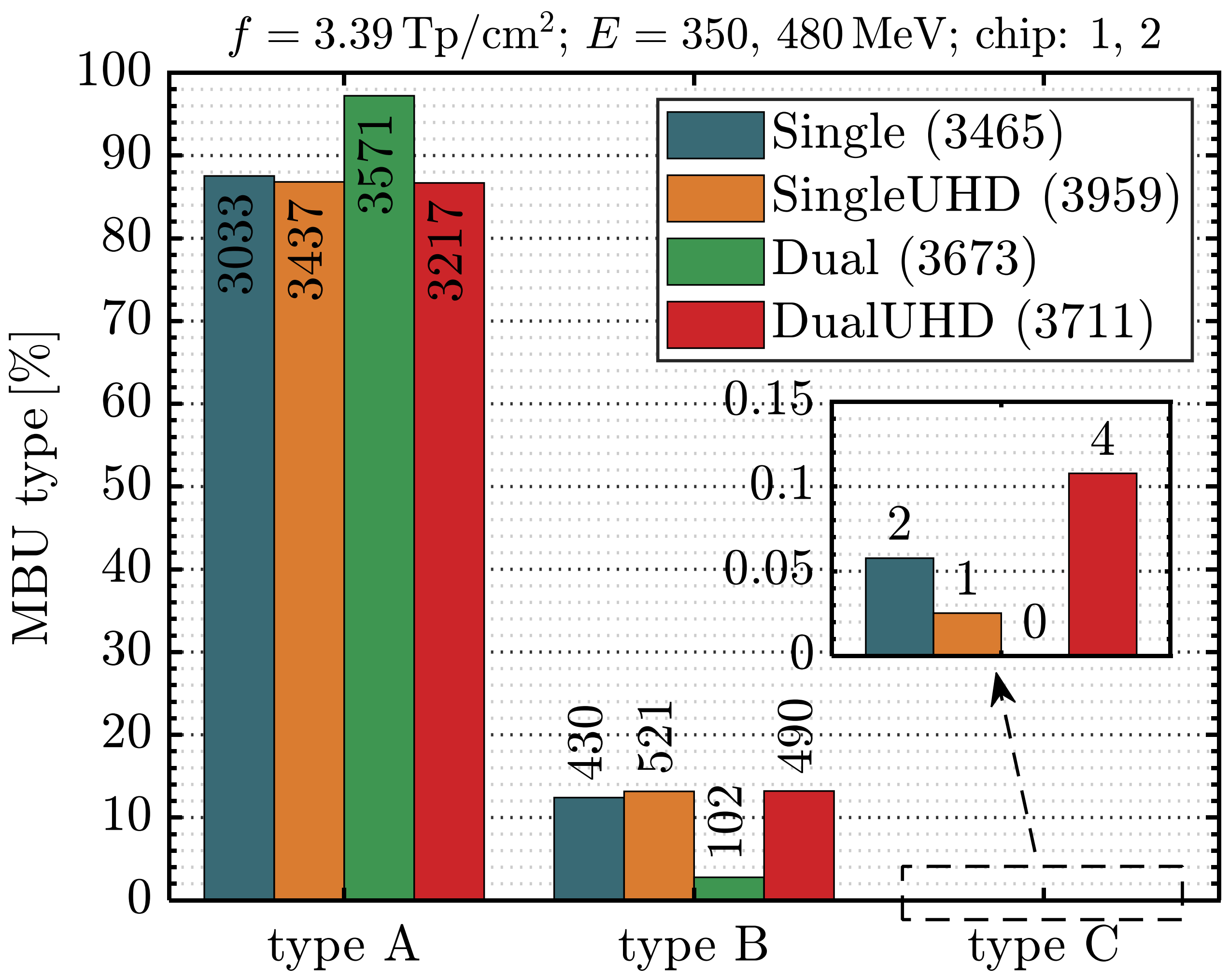


different bits/different words

b0/w0	b0/w1	b0/w2	b0/w3
b0/w4	b0/w5	b0/w6	b0/w7
b*N*/w8	b*N*/w9	b*N*/w10	b*N*/w11



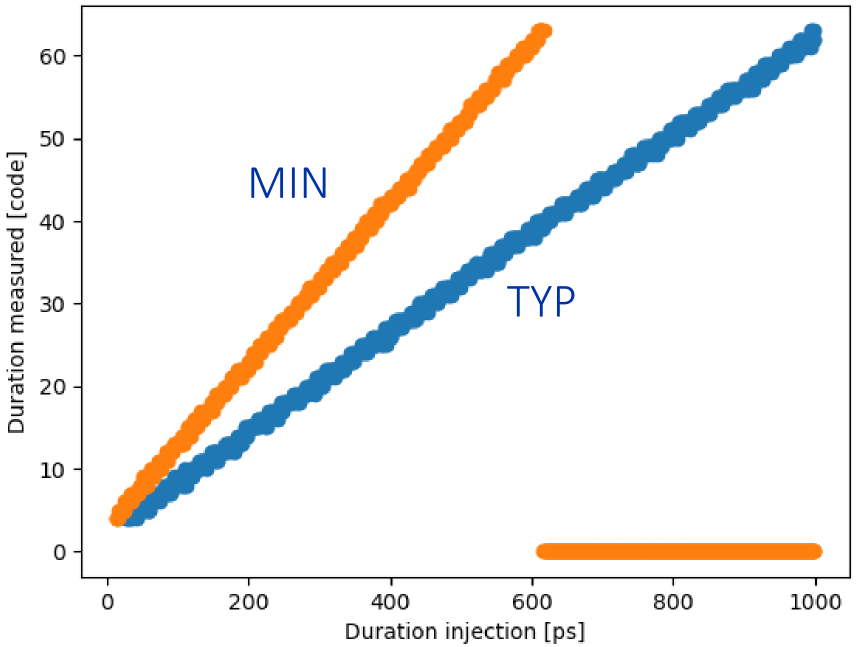
EXP28:SEE – SRAM – MBU – protons

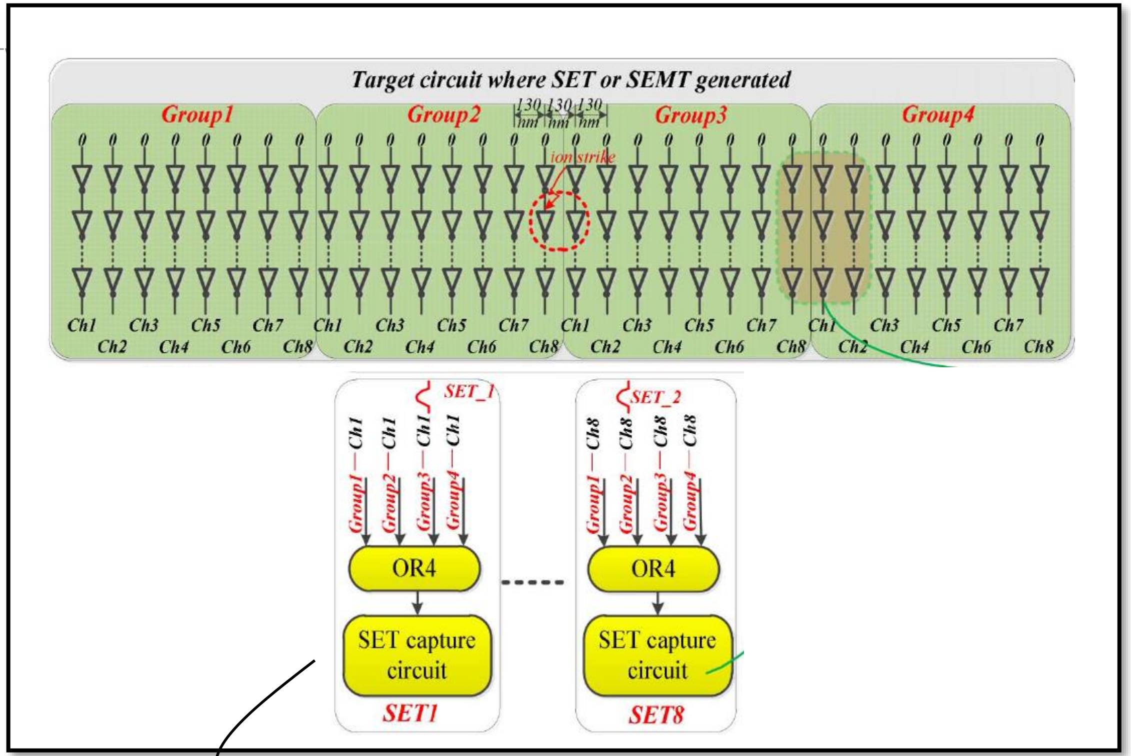


thanks Davide Ceresa for the slides!

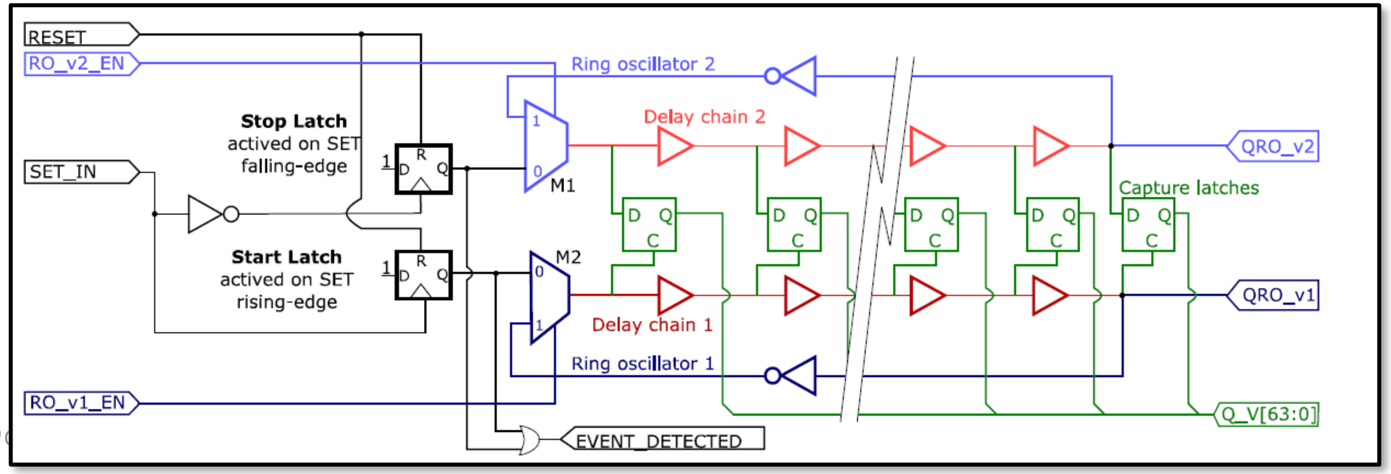
EXP28 SEE: SINGLE EVENT TRANSIENT

Simulation results





SET capture circuit

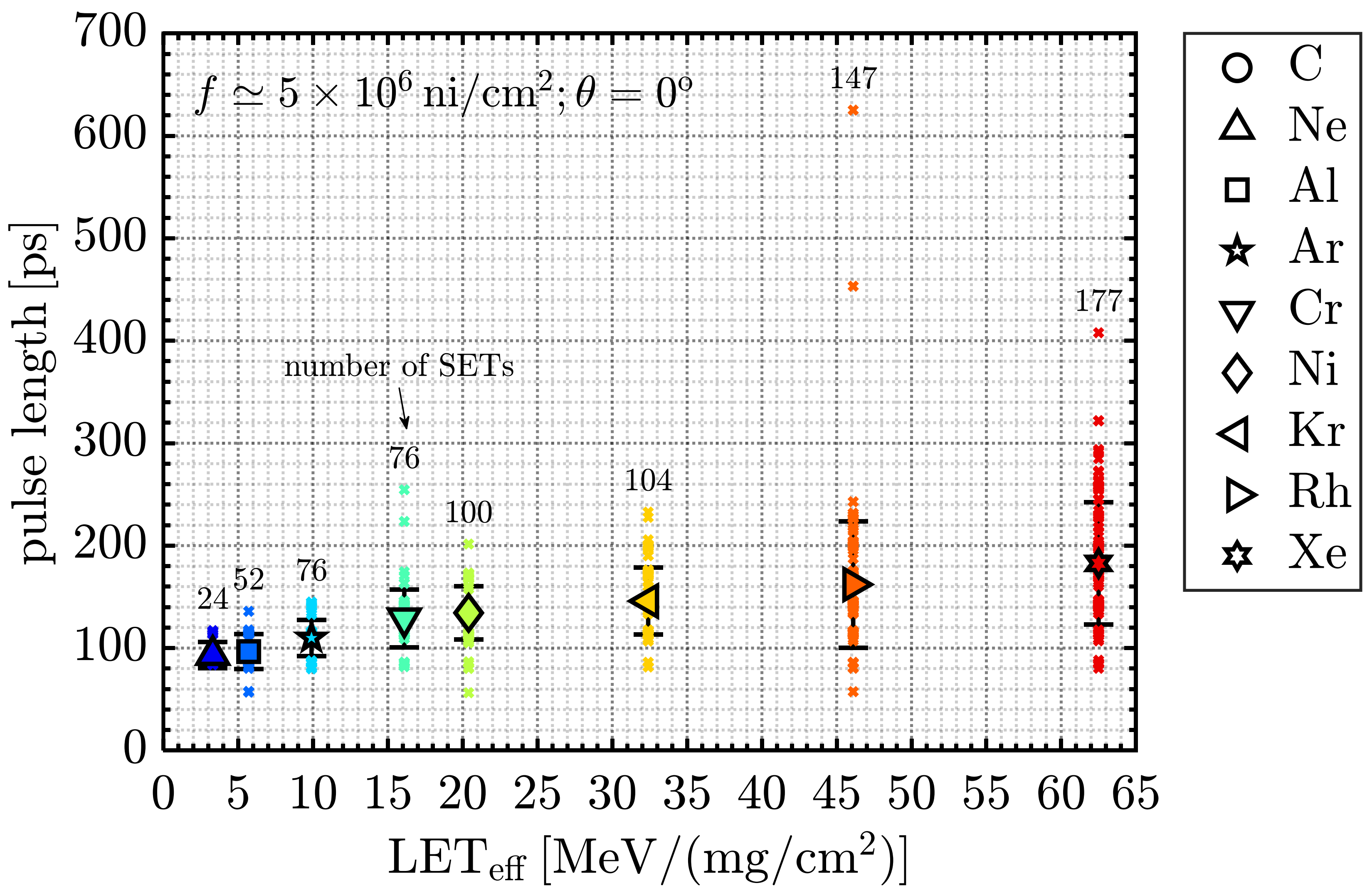


Requires process calibration with Ring-Oscillator

Transient length range up to 1 ns (typical)

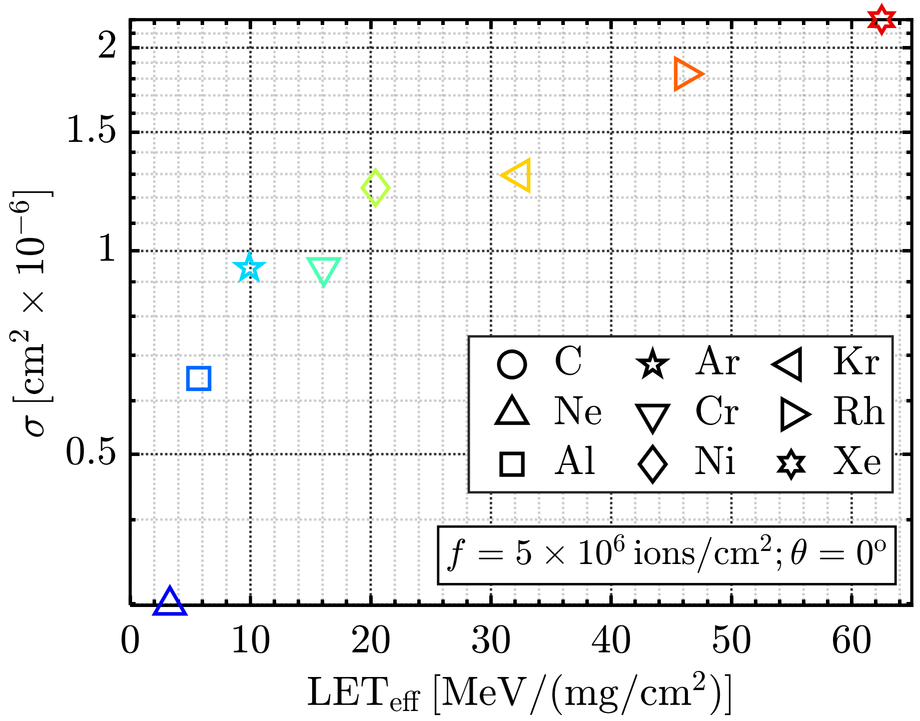
Transient minimum detection ~ 25 ps (typical)

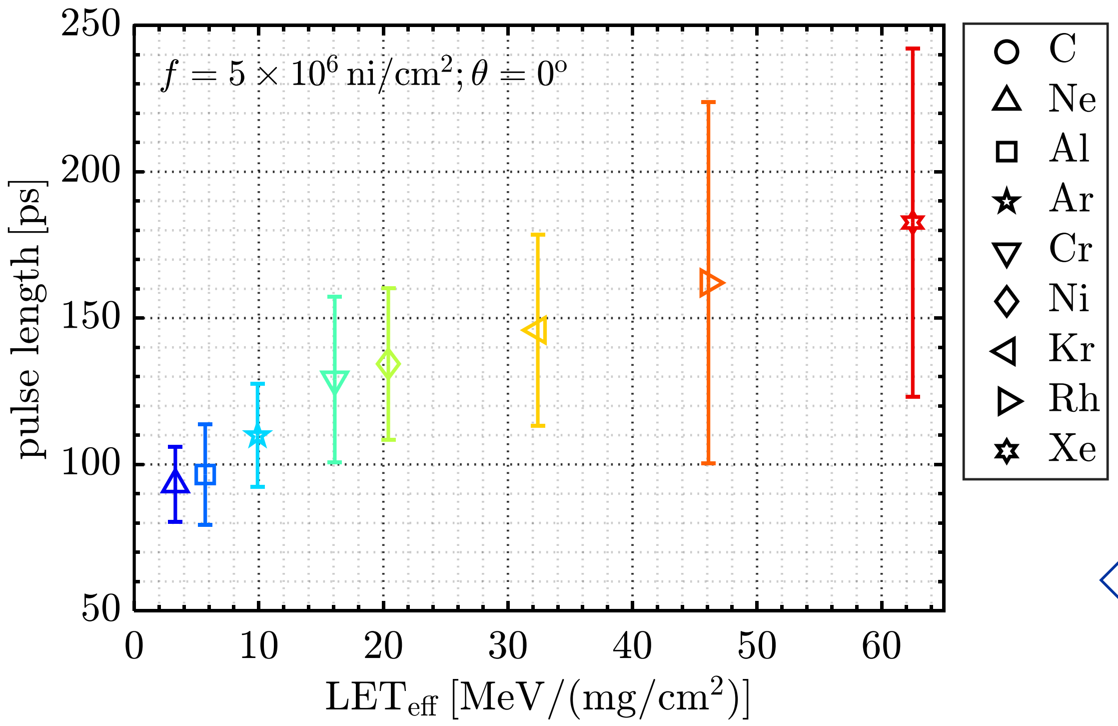
EXP28:SEE – SET – HI



EXP28:SEE – SET – HI

cross section

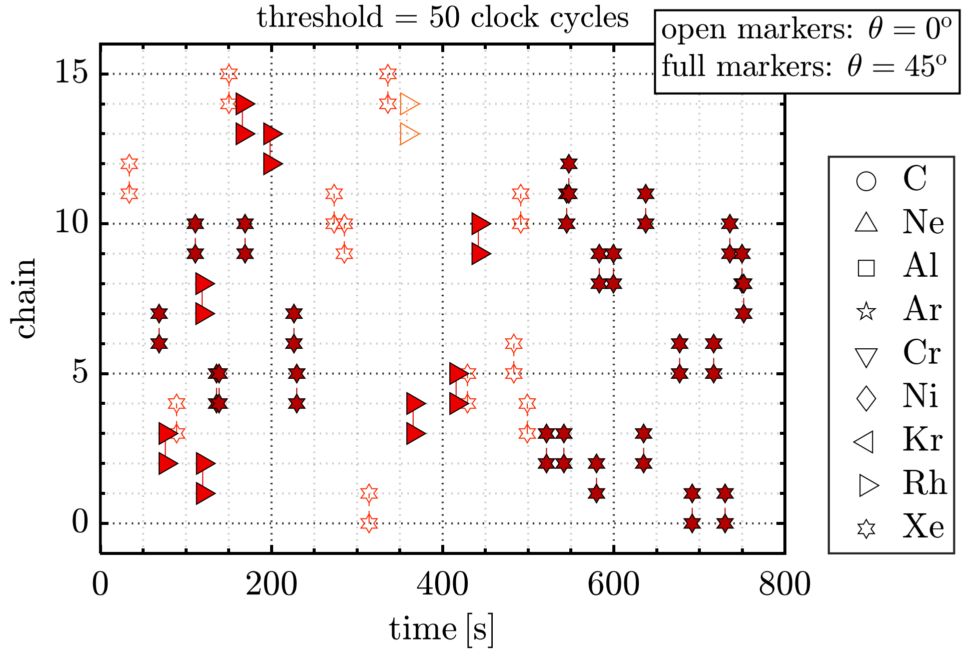


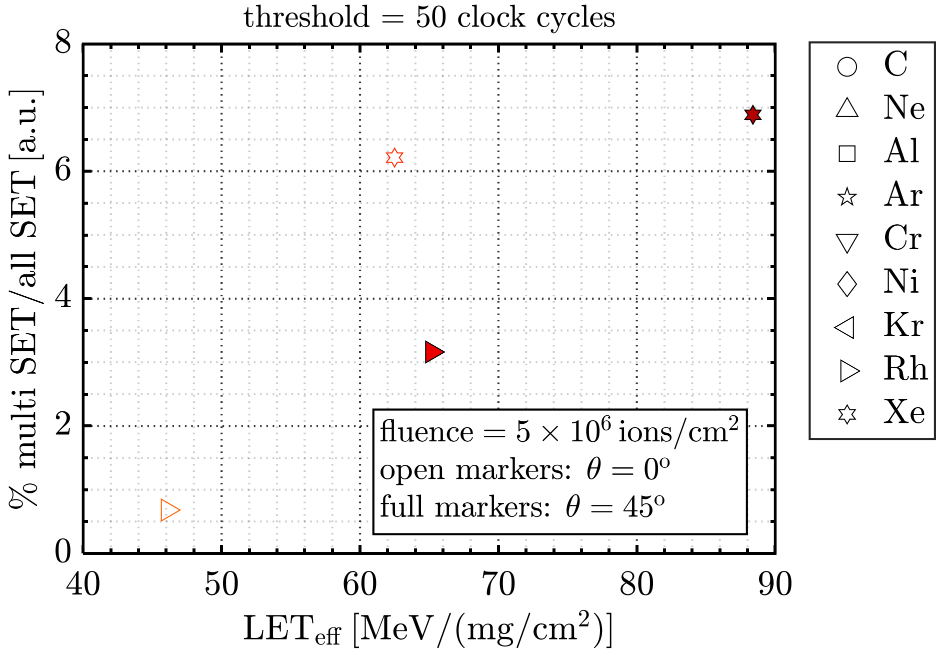


pulse length

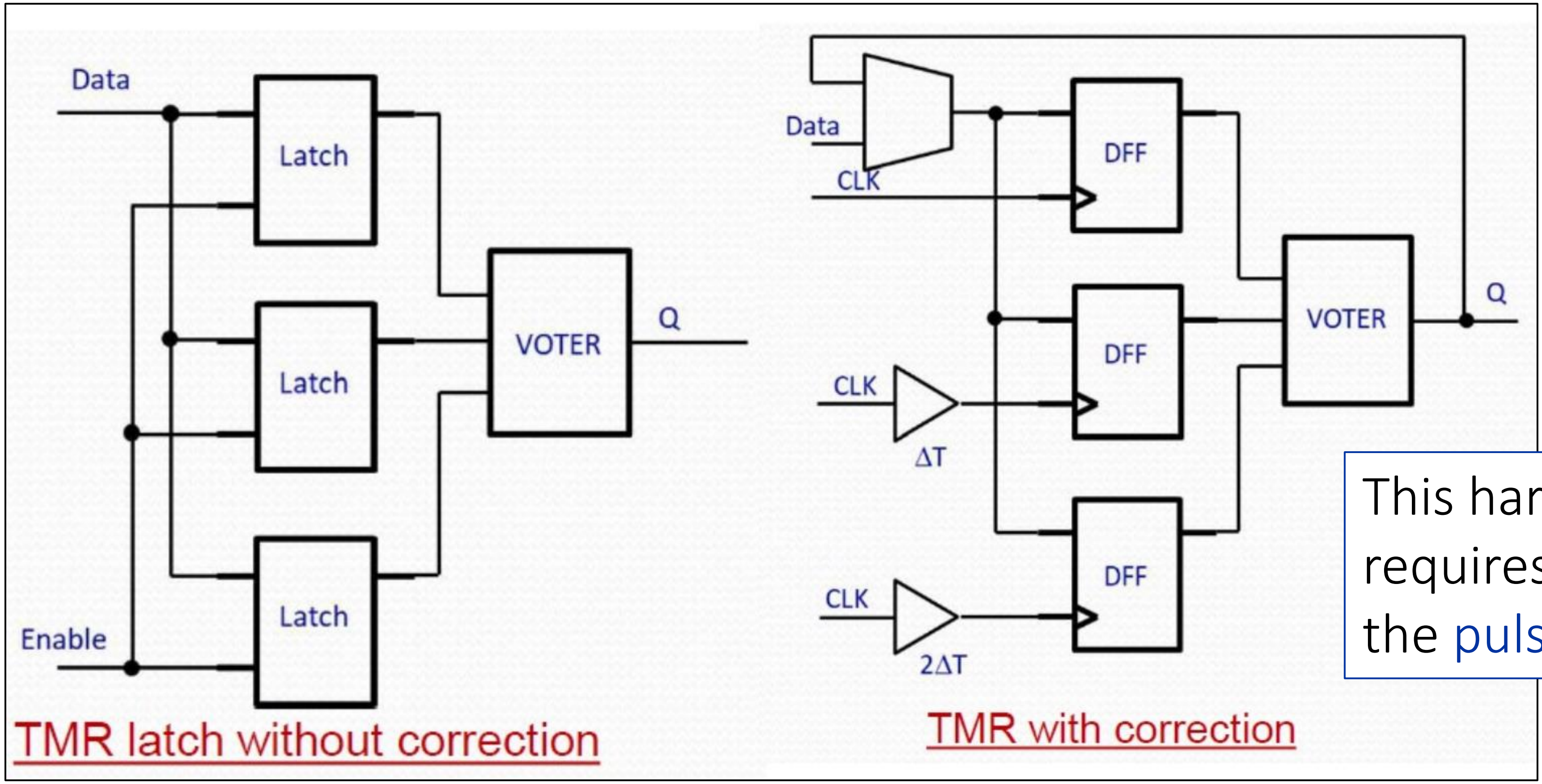
EXP28:SEE – SET (HI)

Multi-SET only of high LET





RD53*: triplicated clock tree with skew for SET filtering



https://indico.cern.ch/event/1038992/contributions/4363708/attachments/2256379/3829070/LHCC_RD53_June2021.pdf

This hardening techniques requires the knowledge of the pulse length!

*readout chips for the ATLAS and CMS pixel detector (https://rd53.web.cern.ch/)

recently measured in chips for ALICE and LHCb!
(130nm CMOS technology)

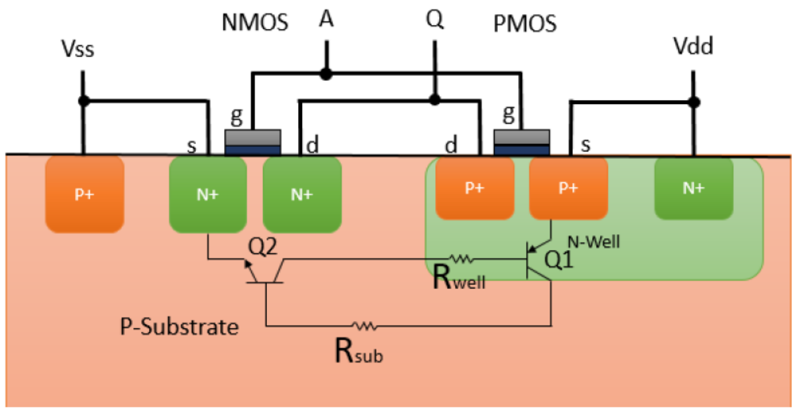
[1] Mahmood S.M., Roeed K., ALICE Collaboration Collaboration, “Investigation of single event latch-up effects in the ALICE SAMPA ASIC”, PoS, TWEPP2018 (2019), p. 023 5 p, 10.22323/1.343.0023, URL https://cds.cern.ch/record/2710375
[2] Lemos Cid E., Vázquez Regueiro P., “The VeloPix ASIC test results”, PoS, Vertex 2017 (2018), p. 052, 10.22323/1.309.0052
[3] Faccio, Federico. "ASIC survival in the radiation environment of the LHC experiments: 30 years of struggle and still tantalizing." NIMA (2023)

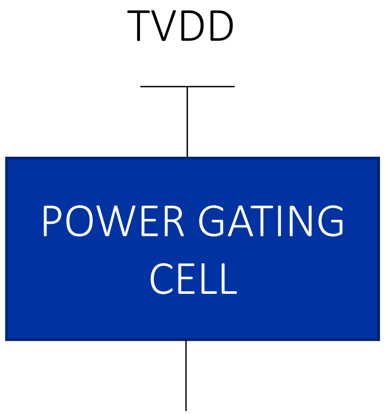
thanks Davide Ceresa for the slides!

Exp28 ANA: GENERAL DESIGN GUIDELINE

SINGLE EVENT LATCHUP:

- EVALUATE MINIMUM DISTANCE BETWEEN SUBSTRATE CONTACTS
- REQUIRES PER CELL POWER MEASUREMENT
- RE-USE POWER GATING CELL FROM RING-OSCILLATOR
- WITH AND WITHOUT DEEP N-WELL





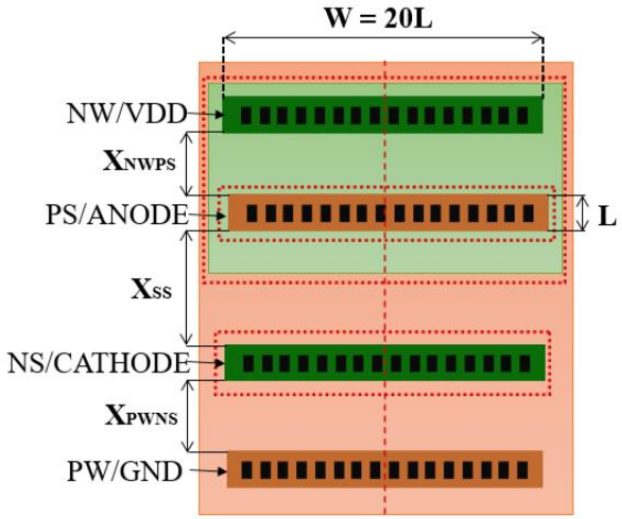
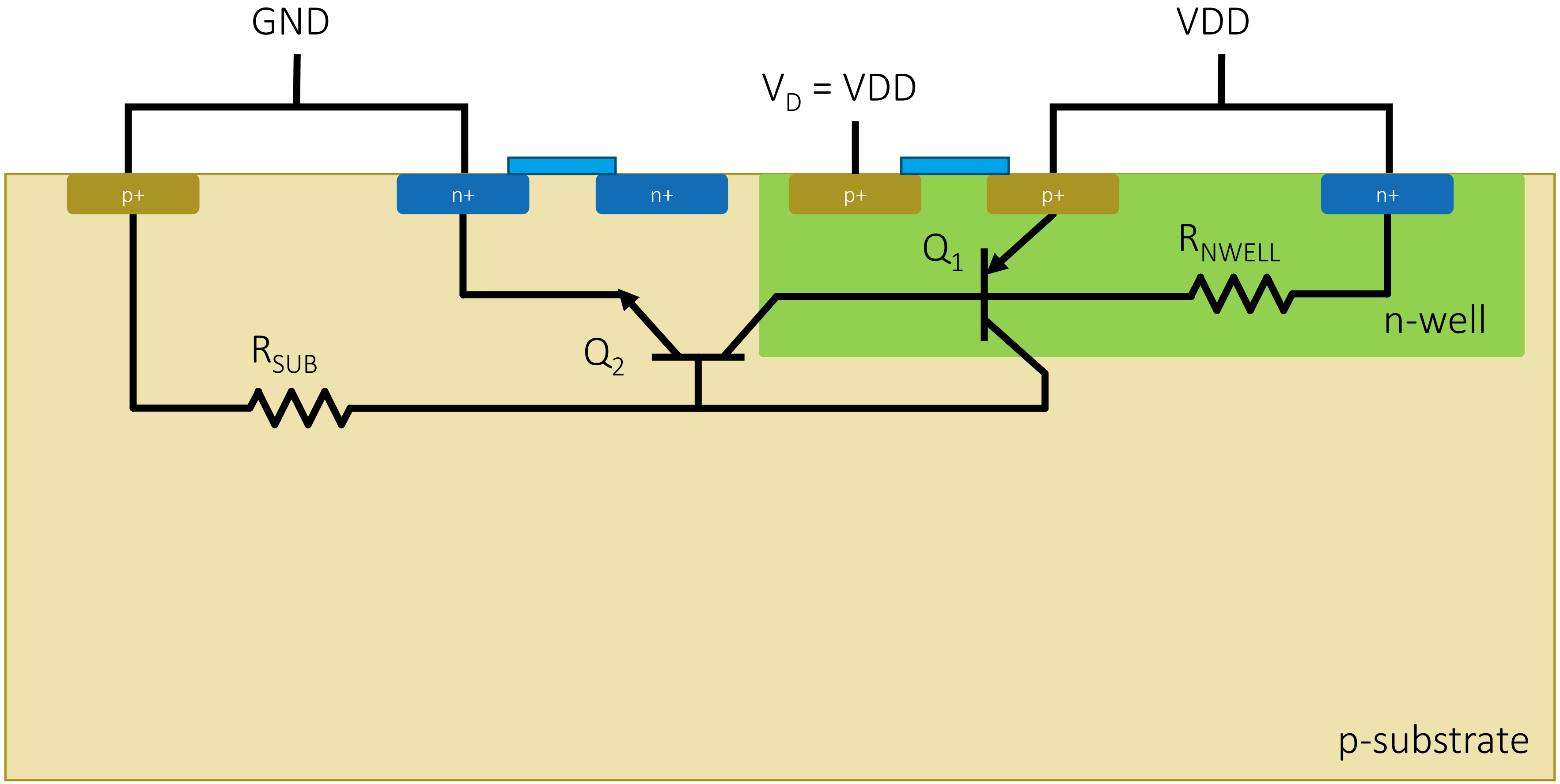
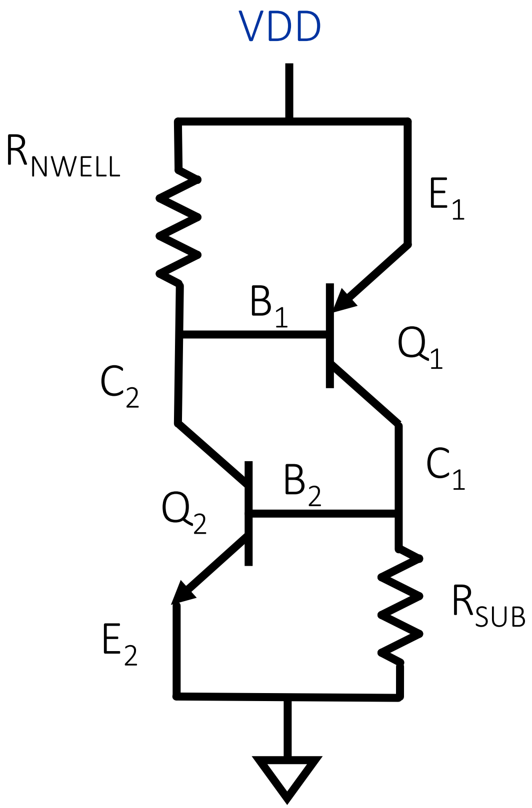


Figure 13

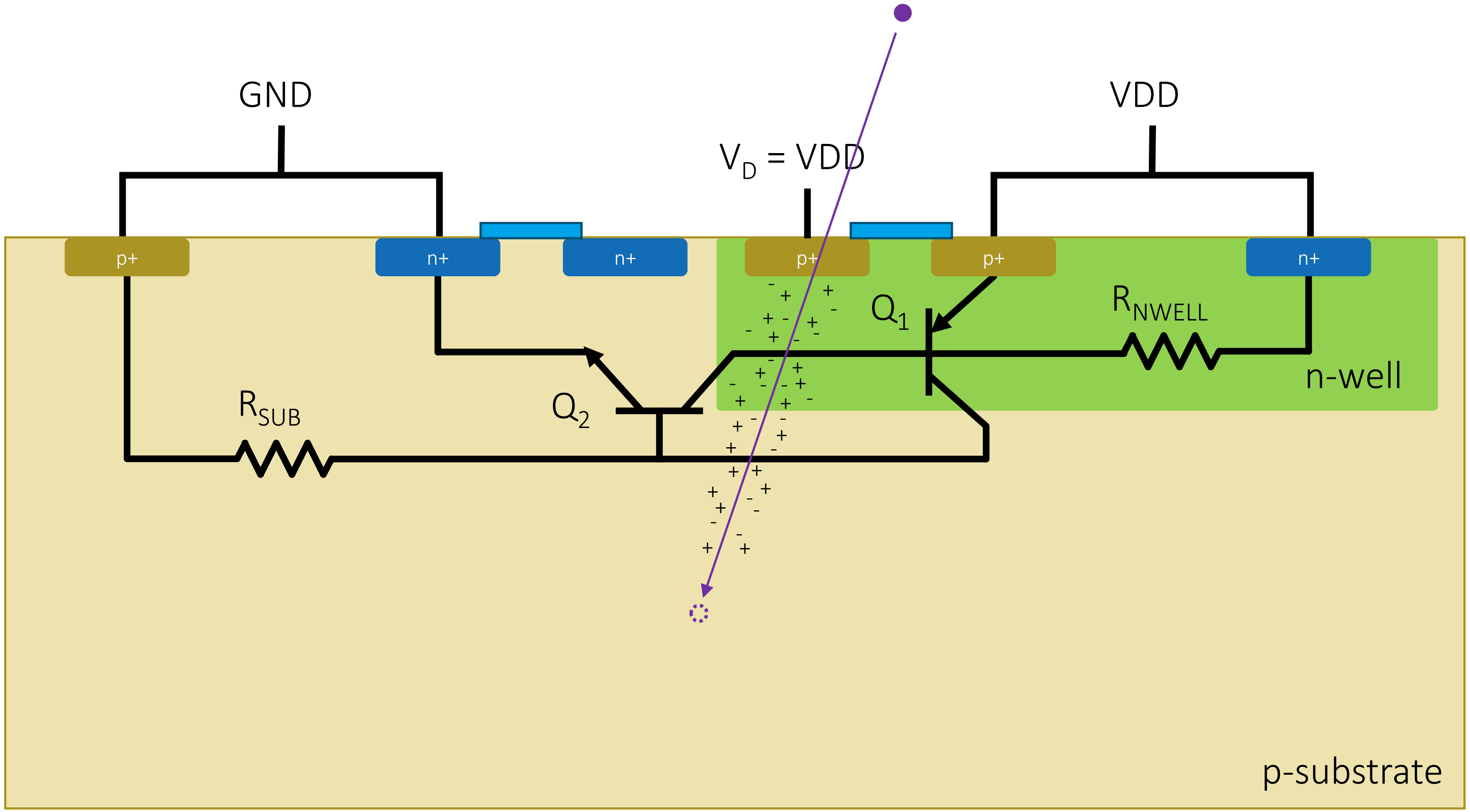
Annotated diagram of the PNPN SEL test structure showing terminal names, terminal values, and linear dimensions

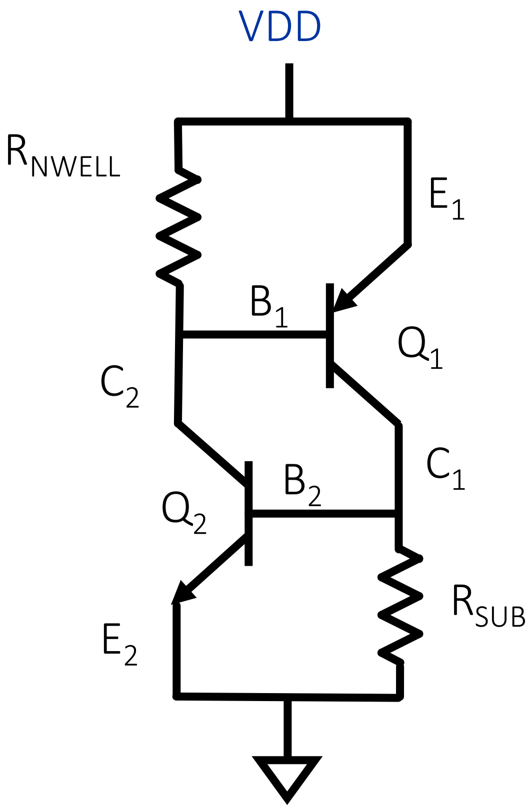
$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1 - \alpha_F) I_E$$



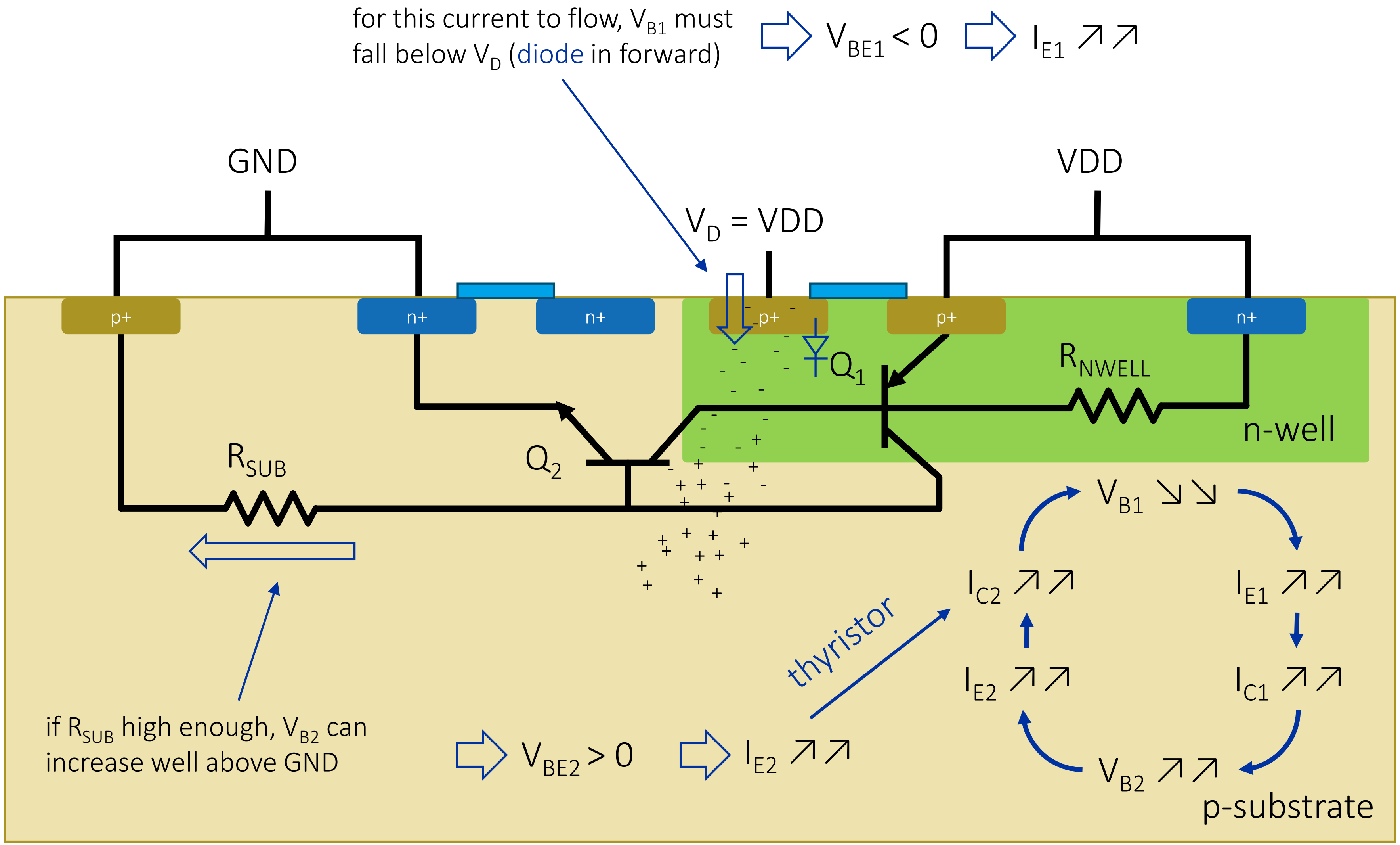


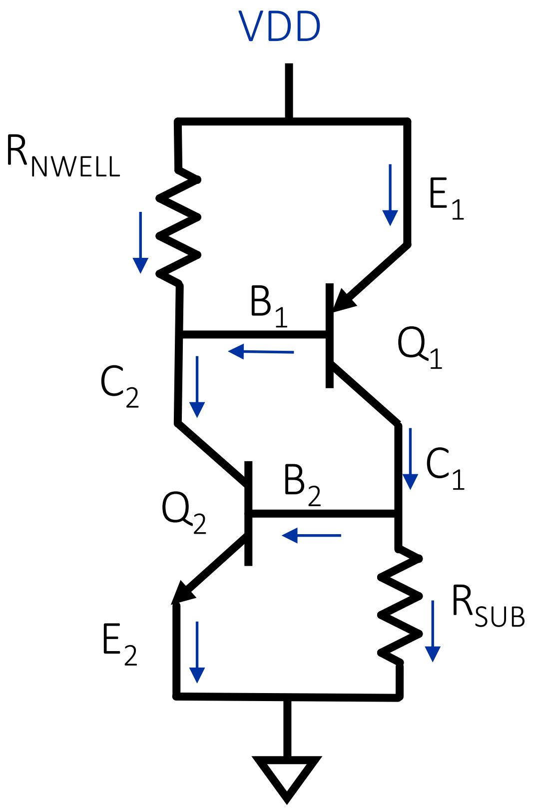
$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1 - \alpha_F) I_E$$





$$I_E = I_S\left(e^{\frac{\pm V_{BE}}{V_{th}}} - 1\right)$$
$$I_C = \alpha_F I_E$$
$$I_B = (1 - \alpha_F) I_E$$





EXP28-SEE

heavy ions and proton test: end of 2022/beginning of 2023

beam time obtained through RADNEXT (for free)

https://radnext.web.cern.ch/