Contribution ID: **112** Type: **Oral**

Characteristics and total ionizing dose response of 22nm Fully Depleted Silicon-on-Insulator

Thursday 5 October 2023 16:00 (20 minutes)

The radiation hardness of transistors in a 22nm Fully Depleted Silicon-On-Insulator (FDSOI) technology exposed to ultra-high total ionizing dose (TID) was investigated. Custom structures including n- and p-channel devices with different sizes and threshold voltage flavours were irradiated with X-rays up to a TID of 100 Mrad(SiO2) with different back-gate bias configurations, up to 2 V. The investigation revealed that the performance is significantly affected by TID with their radiation response being dominated by the charge trapped in the buried oxide. Interestingly, the application of a back-bias of 2 V was not enough to compensate the TID-induced damage.

Summary (500 words)

Single Event Effects (SEEs) are a major cause of failure for Application Specific Integrated Circuits (ASICs) operating in harsh radiation environments, such as space or particle accelerators. A particle with large Linear Energy Transfer (LET), like an energetic ion, crossing the substrate of a semiconductor device creates an ionization tail of electron-hole pairs. In a bulk technology, this charge can be collected relatively deep in the substrate and originate current pulses at active nodes of the circuit, giving origin to SEU (upsets), SET (transient) or SEL (latchup).
In Silicon-On-Insulator (SOI) technologies, the thin silicon film that forms the channel overlays a thick buried oxide (BOX) that isolates it from the bulk substrate. The presence of the BOX limits the extension of the charge collection region and makes these technologies intrinsically more tolerant to SEE. Moreover, it allows the possibility of tuning the electrical characteristics of individual transistors by the application of individual (or grouped) body or back-gate bias. However, the BOX is typically tens of nanometers thick and therefore prone to trap a large amount of charge when exposed to ionizing dose. In view of possible application in HEP, where doses can be orders of magnitude higher than those typically reached in space applications, it is interesting to study the Total Ionizing Dose (TID) response of commercial SOI technologies and if/how it can be improved by dedicated biasing techniques.
In this work, the characteristics of n- and p-channel transistors with different sizes and threshold voltage flavors in a 22nm Fully Depleted SOI (FDSOI) technology were evaluated before irradiation and after exposure to X-rays up to a TID of 100 Mrad(SiO2). Preliminary data showed that both nMOS and pMOS are severely affected by TID. A TID of 1 Mrad(SiO2) is sufficient to cause a ˜-70% degradation of the on-current in pMOS devices, regardless the width of the transistor. The size independence is a strong indication that performance degradation is primarily caused by the charge trapped in the BOX. In both nMOS and pMOS the variations of the on-current can be explained by the threshold voltage shift induced by the trapped charge. The observed rebound in the response of nMOS devices is related to the late formation of negatively charged interface traps, which compensate the charge trapped in the oxide, a mechanism similar to that observed in other bulk CMOS transistors.
The compensation of radiation effects by changing the body or back-gate bias was explored. It is possible to compensate the effects only for TID < 1 Mrad. Unfortunately, the bias to be applied for the same dose is different between nMOS and pMOS transistors. In our presentation we will additionally show results of an on-going study about the impact of the back-gate bias during high-temperature annealing and of back-bias

voltages higher than the maximum Vdd of the technology (2V). The aim is to enhance electron tunneling from the substrate to compensate for the charge trapped in the BOX and improve the radiation response.

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Session Classification: Radiation-Tolerant Components and Systems

Track Classification: Radiation-Tolerant Components and Systems