

CRATEBO: A High-speed, Radiation-Tolerant and Versatile Testing Platform for FPGA Radiation Qualification for High-Energy Particle Accelerator applications

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Abstract (max 100 words)

The CHARM Radiation Tolerant Tester Board (CRATEBO) is a testing platform for the CERN High-energy Accelerator (CHARM) irradiation facility. It is meant to ease the radiation testing of FPGA-based systems by providing users with a radiation-tolerant carrier card for the Device Under Test (DUT). It provides a high-speed communication interface, a flexible power supply, and DUT connections via a System-On-Module socket and an HPC-FMC connector. It is a permanent installation in the CHARM facility at CERN that gives the possibility to users to perform radiation tests of their system with minimum development effort on the test setup.

Summary (max 500 words)

Field-Programmable Gate Arrays (FPGAs) are widely used in electronic systems due to their high performance, flexibility, and cost-effectiveness. At CERN, many systems involving FPGAs are used in the Large Hadron Collider (LHC) radiation environment, therefore their qualification is crucial to ensure a reliable operation.

Our previous work involved benchmark circuits to test FPGAs, which in addition to the classical element testing improved the qualification process enabling comparisons between different FPGA technologies. However, retrieving the failure rate of actual FPGA-based designs, especially in complex systems like detector electronics, is still a challenging task.

To address these challenges, the CHARM Radiation Tolerant Tester Board (CRATEBO) was developed. It is designed to ease the radiation testing process for FPGAs and other systems. It is intended for permanent installation in the CERN High-energy Accelerator (CHARM) irradiation facility offering the opportunity to test and qualify systems in a mixed-radiation field that replicates real radiation environments.

CRATEBO provides all the features essential to conduct radiation testing, i.e. DUT interfaces, communication link, and power supply. These features have a great degree of flexibility to accommodate many kinds of tests.

The board implements a System-On-Module socket to host FPGAs. Currently, several FPGAs SOMs have been developed and tested using CRATEBO. Other international collaborations are underway to test new FPGA applications. The board also includes a standard HPC-FMC connector, which has two main advantages. First, it is particularly useful when testing systems based on FPGAs and connected to a front-end electronic card, like detector electronics. In these cases, CRATEBO allows to perform a radiation test of the full application with minimal development on the test setup. Secondly, the compliance with the FMC standard enables testing of any other commercial module like RF Transceiver and high-speed ADCs.

Concerning the communication interface, CRATEBO implements a high-speed bidirectional link, up to 4.8 GB/s, based on the radiation tolerant Giga Bit Transceiver ASIC (GBTx). Its advantages are threefold. It enables reliable communication with the DUT, preventing corruption of experimental data. It gives the possibility to test challenging designs that involve high-data rate processing. Additionally, it allows testing of actual designs made at CERN, since they use the same communication interface. However, other communication interfaces can be used if necessary. Wireless modules are being developed in this perspective.

The board features a flexible power scheme that can be adapted to the voltage requirements of the DUTs or FPGAs. It uses radiation-tolerant power modules that come with either the radiation-hardened ASICs developed at CERN or with radiation-qualified Commercial Off-The-Shelf (COTS) components. In the latter case, the modules can be replaced before reaching their Total Ionizing Dose (TID) threshold. The front-end FMC connectors have a separate supply to avoid potential Single Event Latch-up (SEL) on the FMC DUT from propagating to the carrier board.

In summary, CRATEBO significantly reduces the user's burden in the test setup and installation for FPGA-based applications. Its flexibility in communication, power supply and DUT interface, coupled with its radiation tolerance, make it a suitable platform to test FPGAs and other systems.