



Contribution ID: 216

Type: Oral

Design and performance of the front-end electronics of the charged particle detectors of PADME experiment

Friday 6 October 2023 09:00 (20 minutes)

The PADME experiment at LNF-INFN employs positron-on-target-annihilation technique to search for new light particles. Crucial part of the experiment are the charged particle detectors, composed of plastic scintillator bars with light transmitted by wavelength shifting fibers to silicon photomultipliers (SiPM). The location of the detector –close to a turbomolecular pump, inside a vacuum tank, and exposed to 0.5 T magnetic field –has driven the design of custom modular SiPM front-end and power supply electronics. The design of the system and its performance, confirming the desired sub-ns resolution on the reconstructed particle times, will be shown and discussed.

Summary (500 words)

The PADME experiment aims to search for new light particles by performing a precise measurement of the final state products of the interaction of accelerated positrons in a thin diamond target. The charged particle detector system of the experiment has to detect deflected by 0.5 T magnetic field electrons and positrons with higher than 99% efficiency and less than 1 ns time resolution, to provide the required vetoing capabilities of the Standard Model background channels. In addition, by design, the PADME experiment uses a vacuum tank with pressure less than 10^{-6} mbar to decrease beam-gas interaction probability. The adopted solution was a plastic scintillator detector composed of polystyrene bars with a WLS fiber, placed inside a groove along the bar, with light detected by 3×3 mm² Hamamatsu S13360 silicon photomultipliers (SiPM).

Custom front end electronics modules were designed, composed by a controller, located outside close to the major data acquisition components of PADME experiment, and front-end cards with SiPMs, placed inside the vacuum tank and the 0.5 T magnetic field. The controller delivered low voltage, a fixed 100 V high voltage, and communicated through I2C with the front-end cards to allow bias voltage configuration and SiPM voltage, current, and temperature monitoring. In addition, the controller also provided ethernet connectivity with web-interface to facilitate the user configuration and monitoring.

The front end card hosted a configurable high voltage generator to provide bias to each of the SiPMs. To ensure stability, the initial stage of the bias voltage generator was realized as a current generator followed by a DAC regulated comparator. The signal from the SiPM was preamplified with a fixed gain (4 in PADME case) and then the output signal was formed by a differential line driver, which showed very high immunity against externally induced electromagnetic noise. The differential signals were taken via a feed-through flange and about 10 m long line back to the controller, where they were converted to single ended, to match the chosen digitization electronics. A single front-end card served four independently configurable SiPMs.

The described SiPM front end electronics served more than 200 readout channels for extended periods inside the magnet in vacuum with temperature ranging from 15°C to 46 °C, without degradation of its nominal performance.

Primary authors: Dr GIANOTTI, Paola (INFN Laboratori Nazionali di Frascati (IT)); IVANOV, Simeon (Sofia)

University, Bulgaria)

Presenter: IVANOV, Simeon (Sofia University, Bulgaria)

Session Classification: System Design, Description and Operation

Track Classification: System Design, Description and Operation