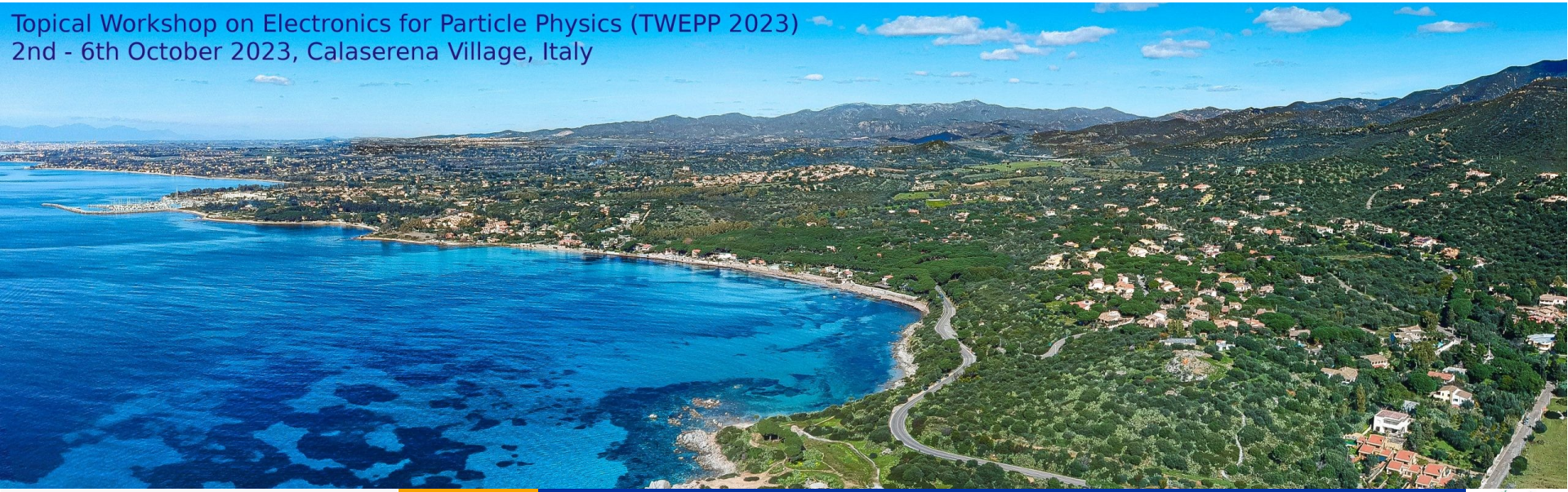
The LHCb VELO Upgrade II: design and development of the read-out electronics

Antonio Fernández Prieto (IGFAE)

On behalf of the LHCb VELO upgrade 2 collaboration

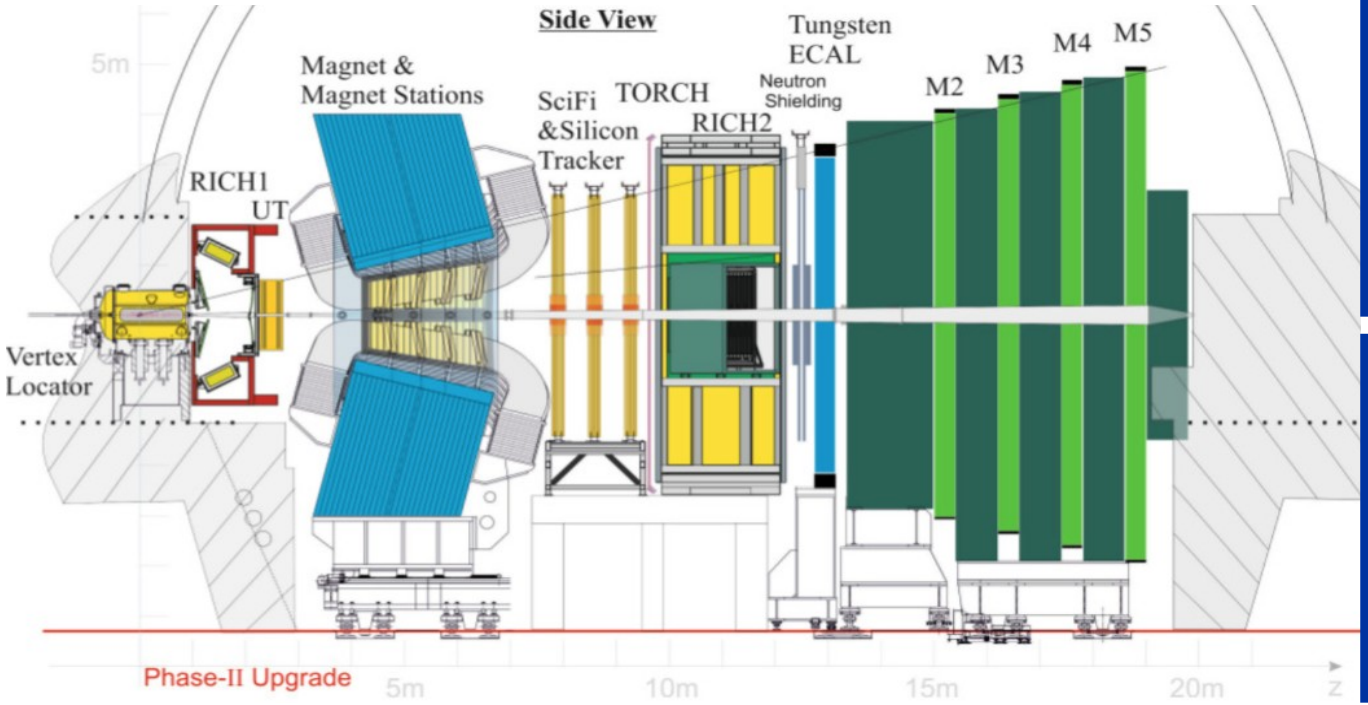


IGFAE Instituto Galego de Física de Altas Enerxías · USC · XUNTA DE GALICIA · MINISTERIO DE CIENCIA E INNOVACIÓN · VERTEX LOCATOR

Outlook

- **Overview of LHCb and VELO upgrade II**
- **System & readout challenges**
- **ASICs**
  - TimeSPOT
  - PicoPix

LHCb upgrade phase II



- Single-arm forward spectrometer
- Covers pseudorapidity 2 to 5
- Precise tracking system
- Triggerless hardware readout (40MHz)

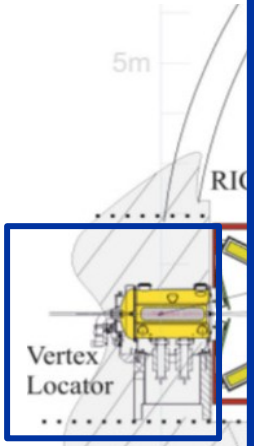
Run 5 & 6

x7.5 Luminosity (1.5×10^{34} $cm^2 s^{-1}$)

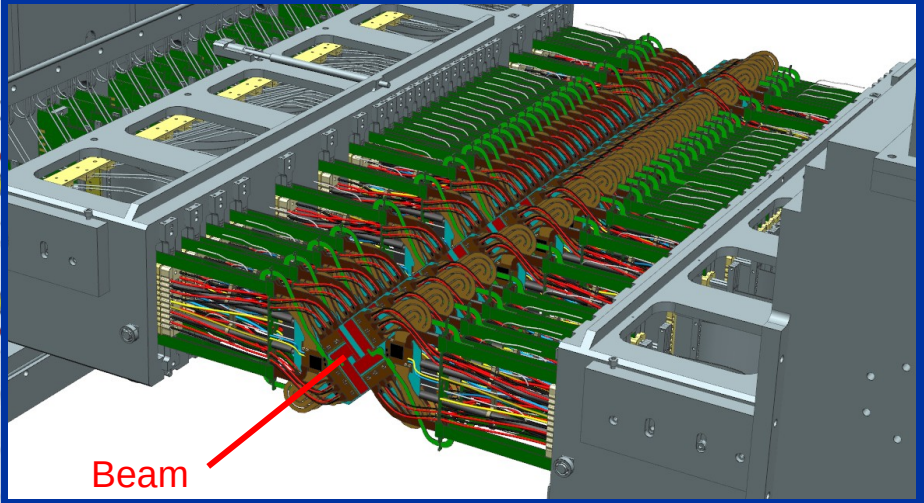
Improvements:

- Granularity
- Fast timing (ps)
- Radiation hardness

LHCb VELO upgrade phase II



Vertex Locator (VELO)



CAD model of the current VELO

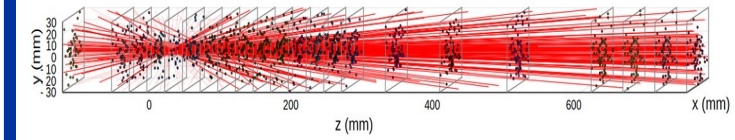
Primary tracking and vertexing detector surrounding the collision region

- **Retractable halves**
- **Secondary vacuum separated from LHC**
- **Operating temperature -20 ºC**
- **High and non-uniform irradiation ($\propto r^2$)**
- **Design must minimize the material budget in the acceptance**

VELO upgrade phase II

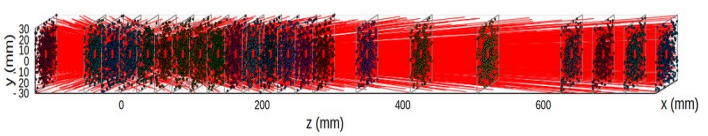
Run 3 & 4

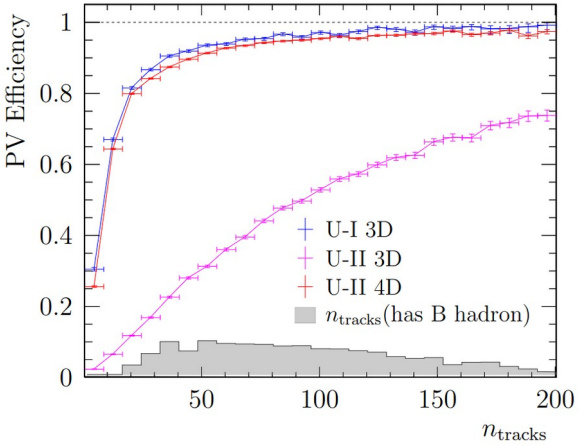
Pile-up ~6



Run 5 & 6

Pile-up ~42 => ~2000 tracks



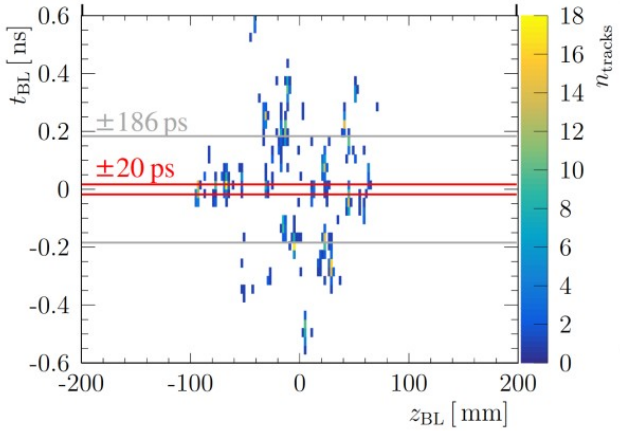


Timing needed to maintain PV Efficiency

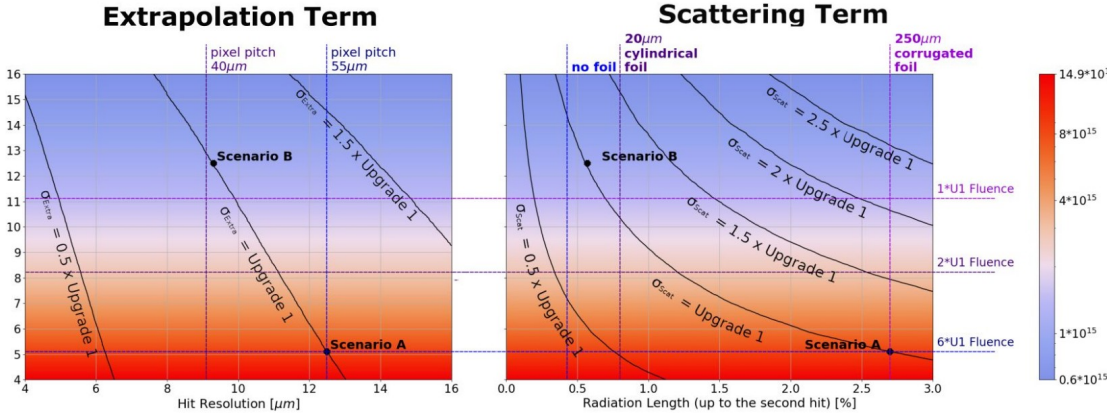
~20ps per **track** => <50ps$_{rms}$ hit

<50ps $_{rms}$ => σ^2_{sensor} (40 ps)+ σ^2_{ASIC}(30ps)

- Sensor R&D. (More details here)
  - LGAD, 3D, Planar
- ASIC R&D



Scenarios



Scenario A (Sa)

- Same distance as U1 (5.1mm to beam)
- Same Pixel size as U1 (55μm x 55μm)
- Rad hard: **3GRad**
- ASIC Bandwidth: **>250Gb/s**

Scenario B (Sb)

- Far from beam (12.5mm)
- Reduce pixel size (42μm x 42μm)
- Rad hard: **400MRad**
- Reduce foil material budget or operate in the LHC vacuum
- ASIC Bandwidth: **>94Gb/s**

System & readout

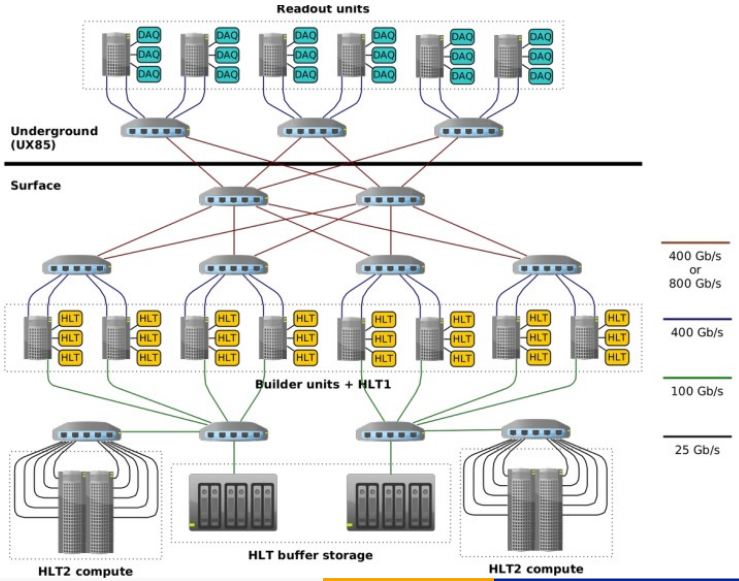
LHCb & VELO upgrade II readout

Same readout architecture philosophy as upgrade I

- Triggerless (@ 40MHz)
- Readout units populated with a PCIe card that collects the FE data

High precision timing distribution will be critical

- E. Mendes TWEPP22



Assuming similar conditions to upgrade I

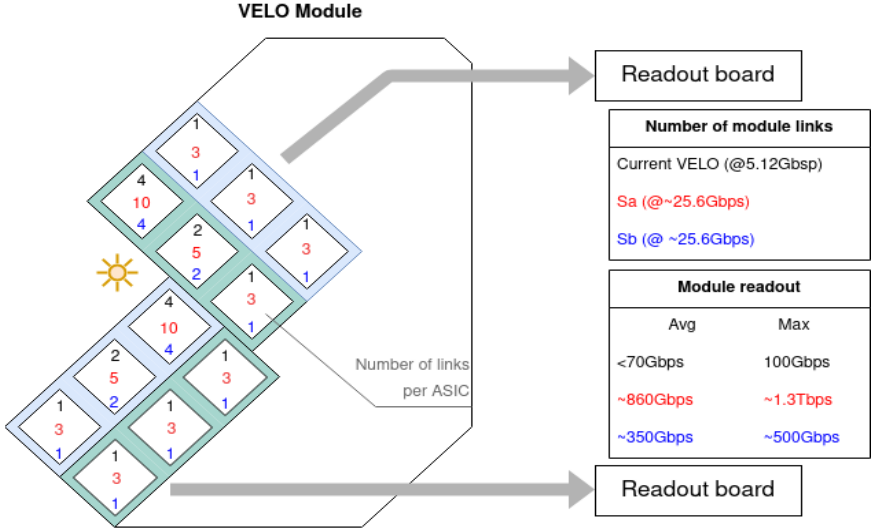
- Layout, number of ASICs, Similar sensor area …

Link constraints

- Sa => Module avg ~860Gb/s
- Sb => Module avg ~350Gb/s

Bandwidth constraints

- **FE ASIC data reduction is required**



Data transmission

Data transmission inside the detector

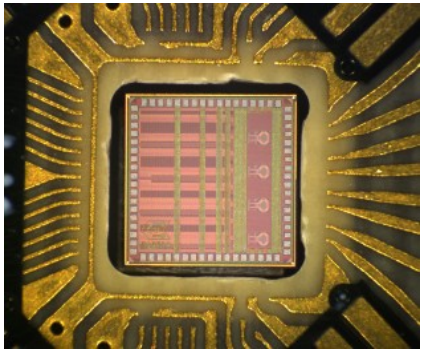
- **~1m in vacuum**
- **Radiation environment**
- **Flexible substrate**

Current solution are Flex tapes. But high speed (20-30GHz) will make it not feasible (Losses ~20dB)

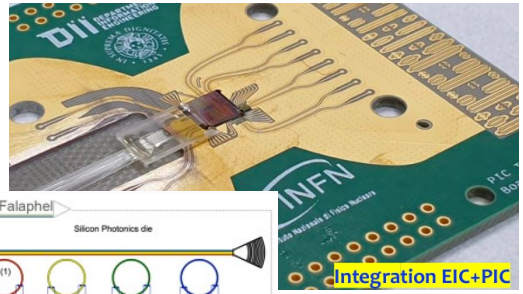
DART28 (Demonstrator ASIC for Radiation-Tolerant Transmitter in 28nm) M.K. Baszczyk F. Martina

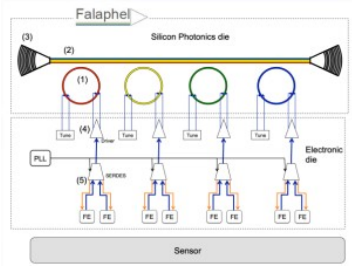
Silicon photonics

- CERN PICs (C. Scarcella TWEPP22)
- INFN FALAPHEL (S. Cammarata)



DART28 ASIC





FALAPHEL

FE ASICs

Requirements & FE ASICs R&D

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤ 55	≤ 42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	< 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

Challenging

TimeSPOT (INFN)

Small scale (32x32 pixel) demonstrator

- 55um x 55um pitch
- Built and tested
- Developing a larger sensor 64X64 matrix
- 28 nm CMOS

PicoPix (CERN, NIKHEF)

Small scale (64x64 pixel) demonstrator.

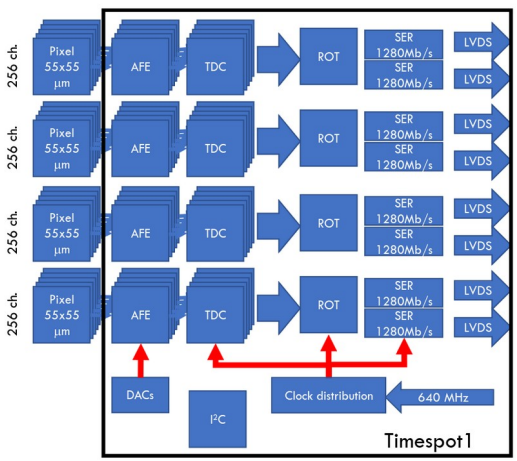
- Derived from TimePix Family
- Design open to meet pixel pitch of Scenario A and Scenario B
- 28 nm CMOS
- Submission expected in Q2 2024

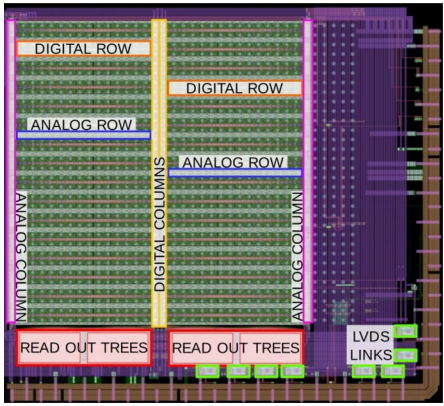
TimeSPOT

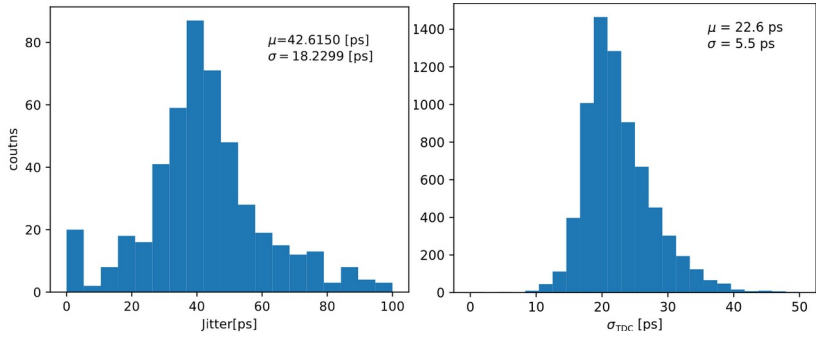
Presented last year by A.Lai

1024 channels, each equipped with Analog Front-End and TDCs (Vernier Architecture)

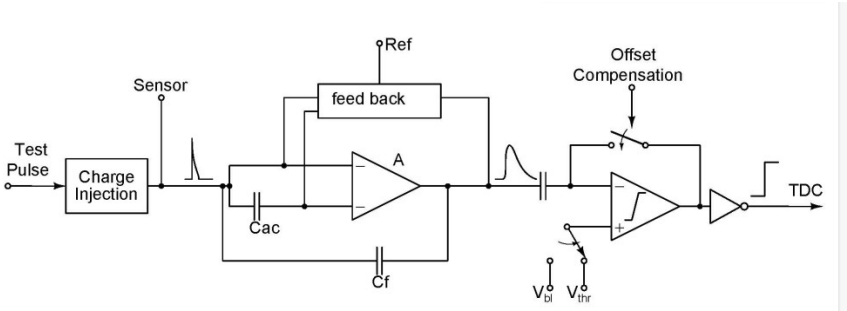
- 256 channels are read-out by a ROT (ReadOut Tree)
  - Addresses incoming data to 2 serializers driving a LVDS driver each data out @1.28 Gb/s
  - 8 data output lines
- 8 DACs giving Voltage references to the Analog Front-End
- Controlled over I2C
- Total time resolution around 50ps ±15ps



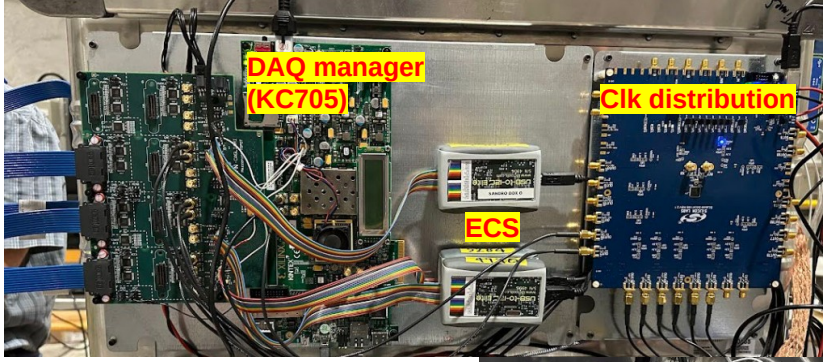


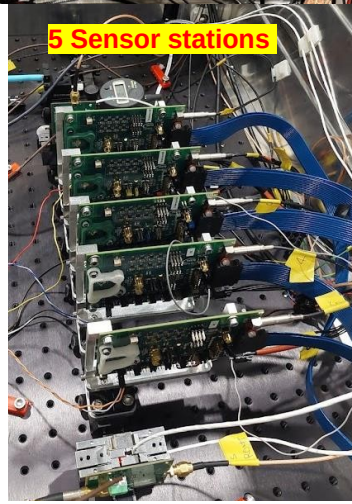


AFE TDC



TimeSPOT





- Test beam @SPS, May 2023 Poster A. Loi Tuesday
  - **First tracks** with a 28-nm based system were acquired and reconstructed
    - 5 stations (3D silicon and 3D diamond sensors)
  - System issues being improved: improve bias voltage, stability problems (power consumption & data transmission)
- **Limitations** related to the global optimization of the chip (disc. voltage baseline, reference clock distribution)
- Working on a 64x64 matrix, based on a repeatable tile structure 8x8 pixels
  - End of the ‘23 beginning of ‘24
- Test chip submitted in July ‘23 (expected for November ‘23). Architectural studies
  - Test basic structures
  - Tests on ECS configuration, TDC calibration, readout

S. Cadeddu Tuesday

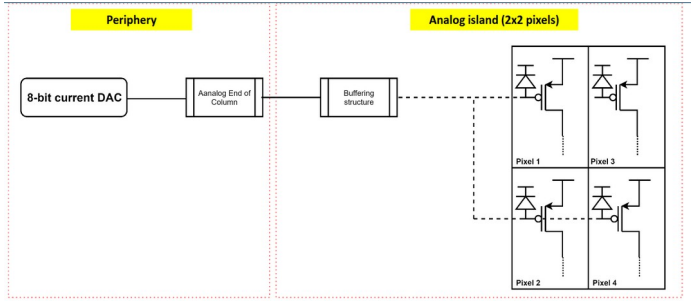
PicoPix- Design & challenges

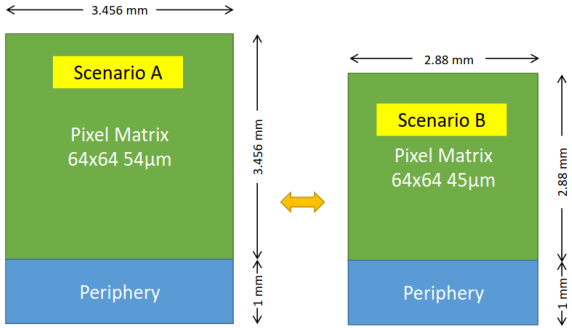
Designed as a “real” **small scale prototype** to avoid to get false expectations on final design:

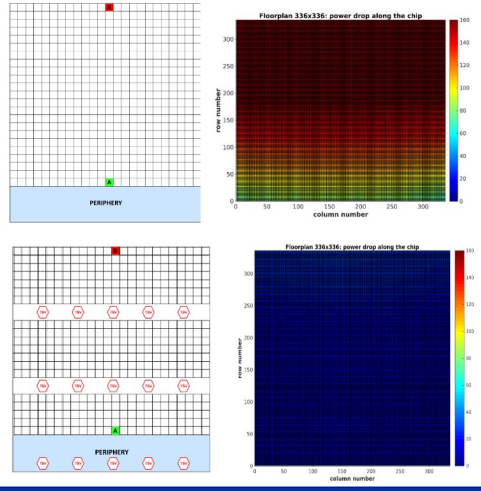
- Analog FE, Pixel readout, Pixel data clustering
- Several parts based on TimePix (Slow control, Pixel groups, clock distribution, etc.)
- Single Event Effect robust architecture

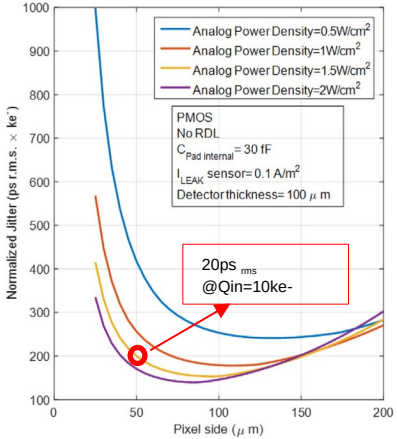
Target track resolution of <20ps$_{rms}$ => (sensor + ASIC) <50ps$_{rms}$ => ASIC < **30ps$_{rms}$**

- Power consumption vs time resolution
- The **power drop** along the pixel must be minimized to avoid top-down effect!
  - Systematic IKRUM mismatch=> ToT mismatch and gain mismatch
  - Solution
    - TSVs (better uniformity, but more expensive & complex)
    - Reduce number of rows
    - On-pixel power compensation





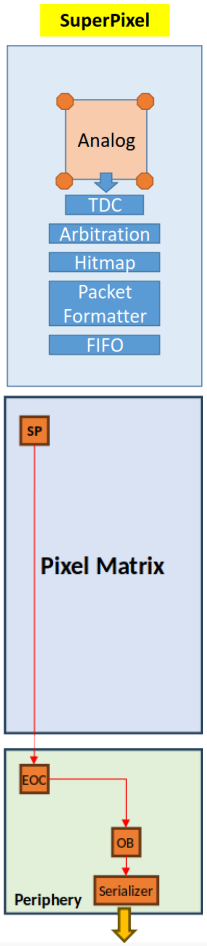




R. Ballabriga et al.

PicoPix - Readout architecture

See Davide's Talk on Tuesday



1 Analog island:

- 4 Analog FE + 4 Discriminator

1 TDC per analog island (or-ed input)

Arbitration:

- Large charge pixel in a cluster is the master
- Works across SuperPixels in all directions

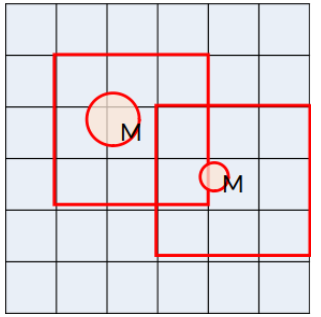
Hitmap (8 bits around master with hit)

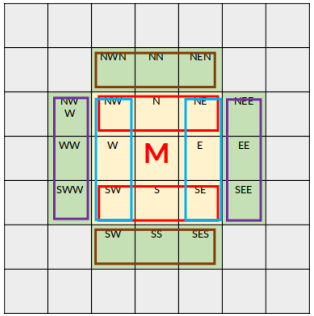
Formatter. ToT information with 24.4ps resolution

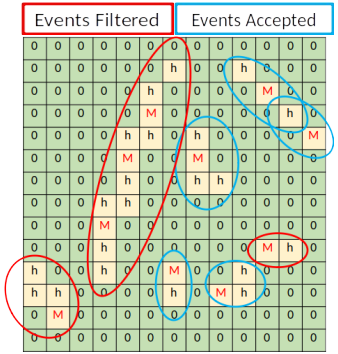
Bandwidth optimization

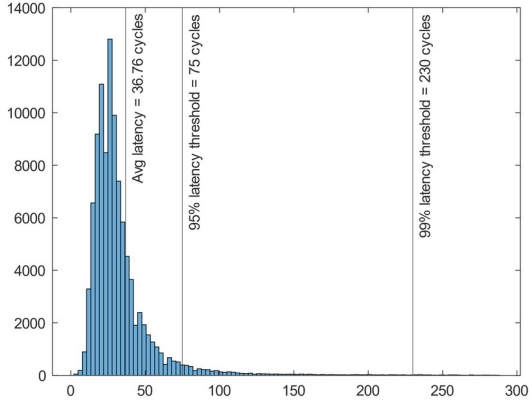
Mandatory to filter undesired data as upstream as possible. Ongoing bandwidth optimization studies:

- Perform on chip Clustering
  - 1 data packet per cluster
  - Master arbitration by ToT
- Filtering of large events. Events >3x3 pixels are outside LHCb acceptance
- Data sorting (by timestamp) on the periphery
- Combined **estimated data reduction ~85%** (~600Gb/s => ~86 Gb/s)



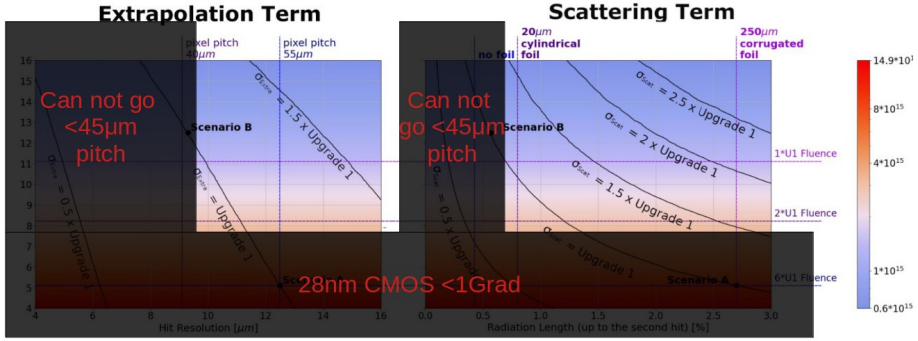






Conclusions

- **Timing is essential for the VELO U2 (4D tracking, etc.)**
- **Starting challenging ASIC R&D**
  - Time resolution of 30ps
  - Limited power budget (<1.5-2W/cm^2)
  - Not module replacement is foreseen => <1Grad
  - Pixel Pitch >45µm. Below that is hard thedesign for Sensors, ASIC design and data rate

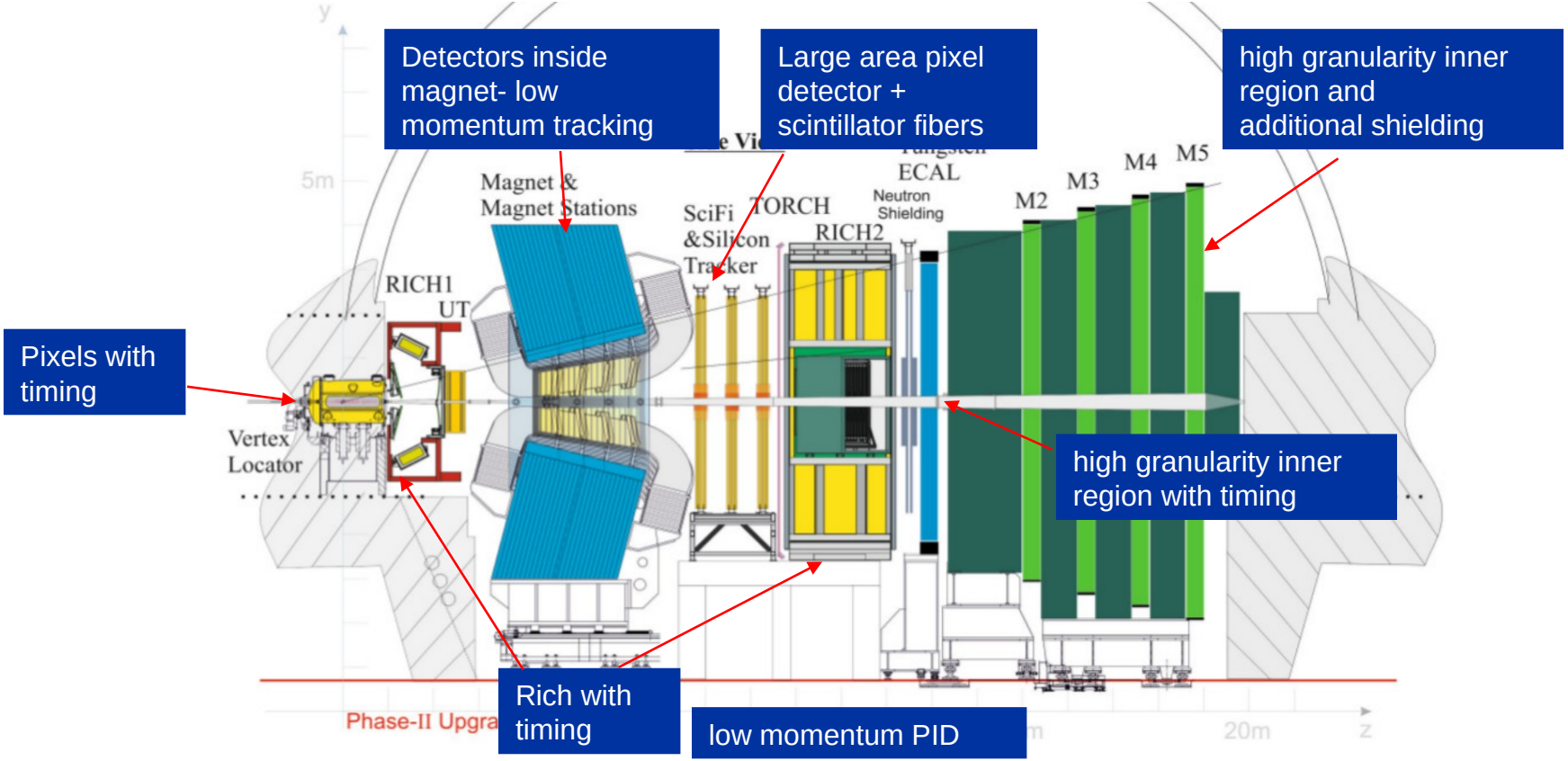


- **Two prototypes of FE ASICs**
  - TimeSPOT
    - Reached a time resolution of 50ps
    - New submission with larger matrix (64x64) on the way
  - PicoPix
    - Exploring new readout schemes
    - Expected submission by Q2/2024
- **Exploring alternatives for reading out the module at high speed (~25Gb/s) in vacuum**

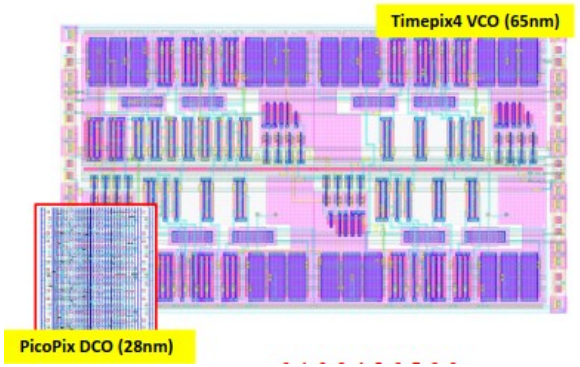
Thank you

Questions?

LHCb upgrade 2



PicoPix - DCO



Explored the idea of the on-pixel free-running DCO with event-by-event calibration:

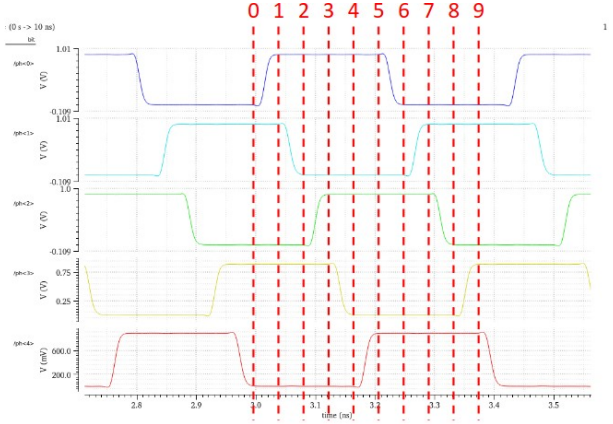
- With 3 bits oscillation control
- Using 7T cells with extracted parasitic

Advantages:

- No control voltage distributed along the column
- Systematic effects can be suppressed
- Faster oscillation times and lower dynamic power → better time resolution

Disadvantages:

- Requires DCO calibration measurement=> data bandwitdth!



	freq	Phases	Phase mismatch [max-min]	LSB	Area	power
Timepix4 VCO	640 MHz	8	~25%	195ps	~350µm^2	~500µW
PicoPix DCO	2-3 GHz	10	< 5%	50-33ps	~38µm^2	~150µW

Time resolution

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Priority — Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm²]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e⁻]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm² [Gb/s]	> 250	> 94

Challenging! doable

Single plane resolution of <50ps $_{rms}$ => $\sigma^2_{sensor} + \sigma^2_{ASIC}$

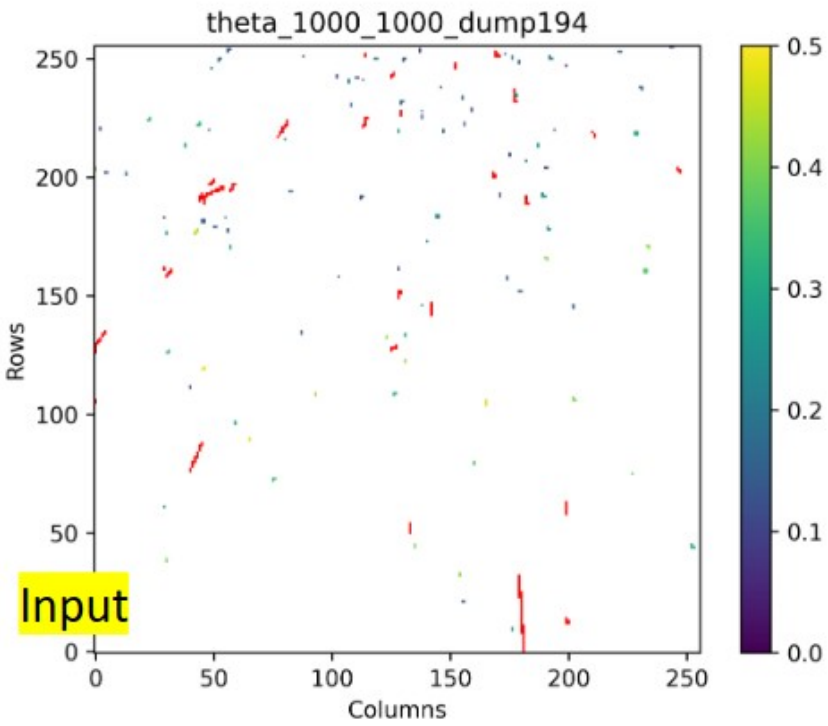
σ^2_{ASIC} (30ps $_{rms}$) => $\sigma^2_{analogFE} + \sigma^2_{conversion} + \sigma^2_{clock}$

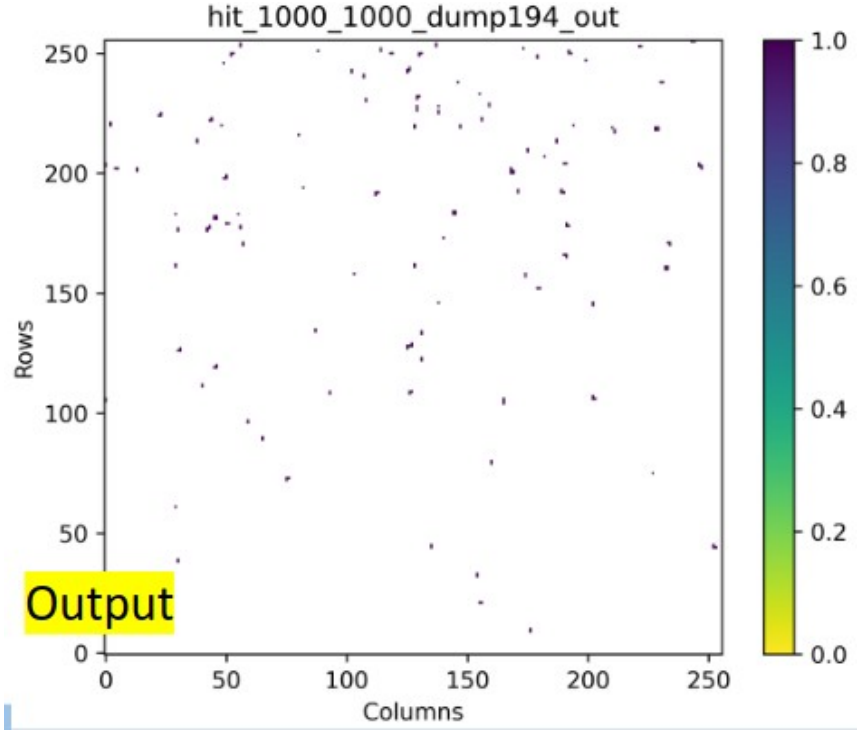
$\sigma^2_{conversion}$=> $\frac{TDC_{bin}}{\sqrt{12}}$ => TDC_{bin} = 40ps => 11.5 ps_{rms}

σ^2_{clk}=> reference level at pixel=> $10ps_{rms}$

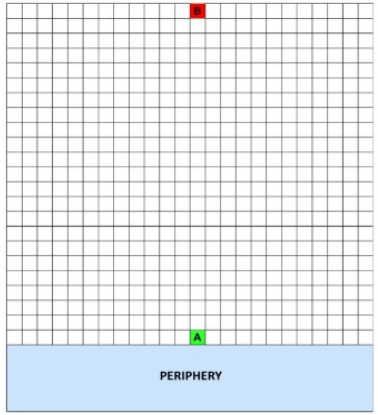
σ^2_{AFE}=> <$25ps_{rms}$

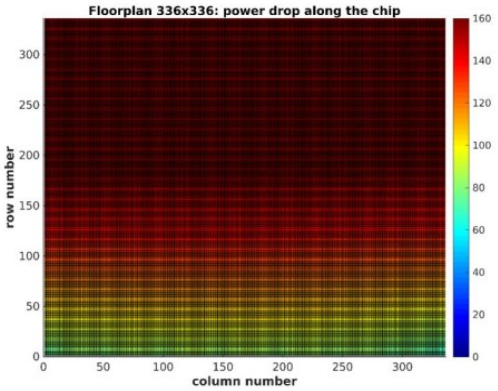
PicoPix data filtering



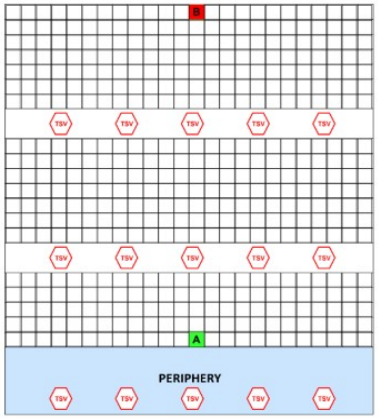


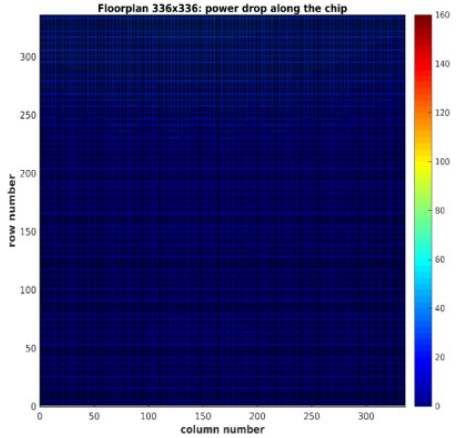
PicoPix TSV





	Pixel A	Pixel B
V_{GND} [mV]	45	90
V_{GND_KRUM} [mV]	45	61
Peaking time [ns]	1.71	2.27
$I_{DS}(M_{INPUT})$ [µA]	17.3	11.9
σ_{TOA} (ps r.m.s)	12	24
I_{KRUM} [nA]	98	69
ToT [ns]	42	68

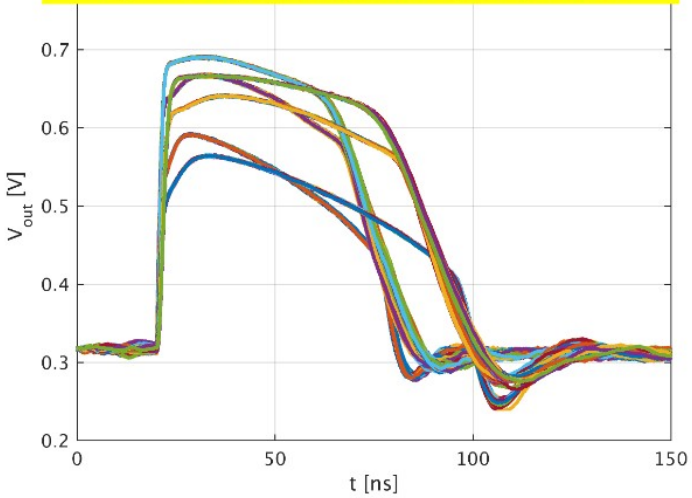




	Pixel A	Pixel B
V_{GND} [mV]	8	14
V_{GND_KRUM} [mV]	8	14
Peaking time [ns]	2.06	2.1
$I_{DS}(M_{INPUT})$ [µA]	17.3	16.5
σ_{TOA} (ps r.m.s)	9	11.5
I_{KRUM} [nA]	98	82.6
ToT [ns]	42	49

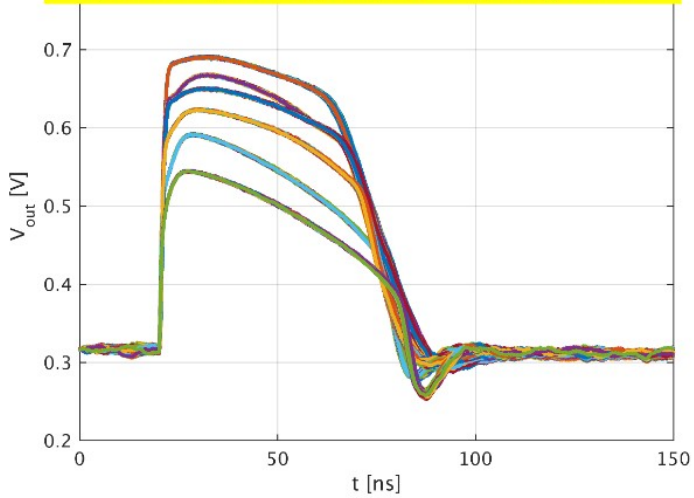
PicoPix on-pixel power compensation

CSA transient response for 20ke⁻ input charge at T={-40 , 25, and 60 °C} without power drop compensation



Temperature	Pixel close to periphery	Pixel close to beam
-40˚C	14 ps	25 ps
27˚C	14.5 ps	29 ps
60˚C	17 ps	34 ps

CSA transient response for 20ke⁻ input charge at T={-40 , 25, and 60 °C} with on-pixel power drop compensation



Temperature	Pixel close to periphery	Pixel close to beam
-40˚C	14 ps	13.5 ps
27˚C	14.5 ps	13 ps
60˚C	17 ps	16 ps

TimeSPOT: next steps

High expected power per pixel (LHCb max rate, 38μW/ch)

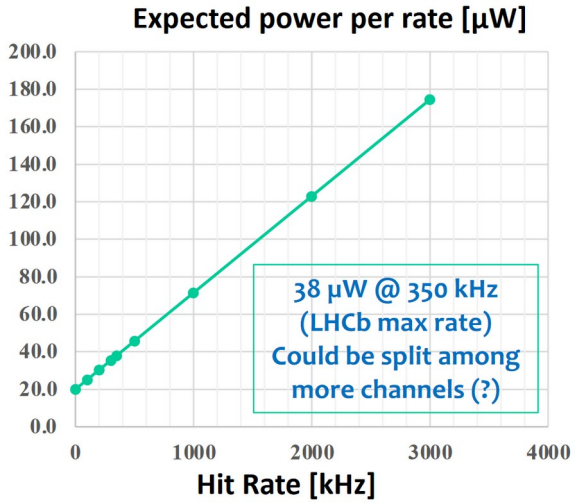
Better clock distribution (reference clock jitter)

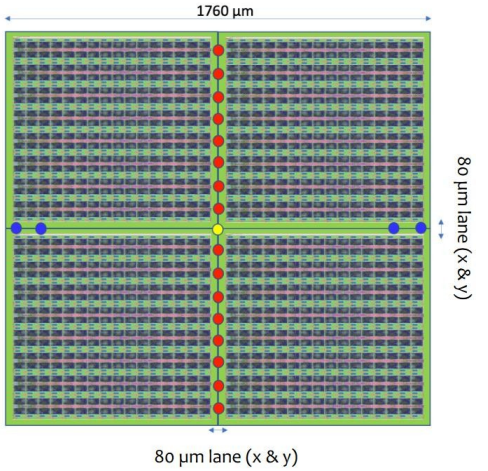
Time resolution of the analogue front-end is better than 20ps or below by design

- Discriminator baseline voltage baseline issue for low voltages

Next step: Larger matrix with improved time resolution

- Through Silicon Vias (TSV) being investigated for power and clock distribution, and data transmission
  - Efforts will be continued by the IGNITED

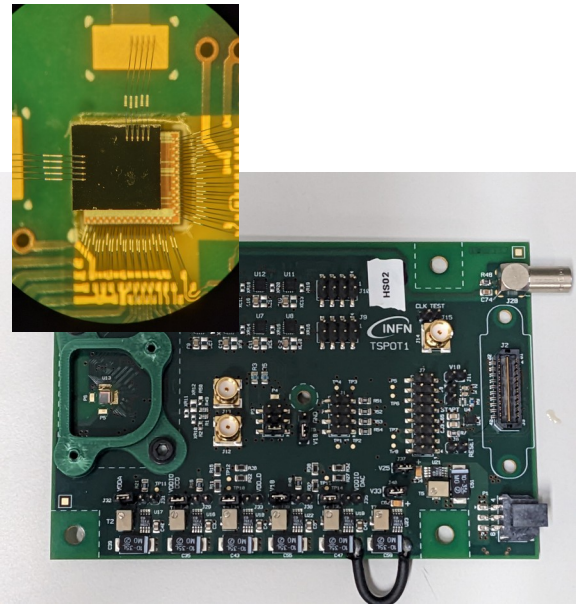


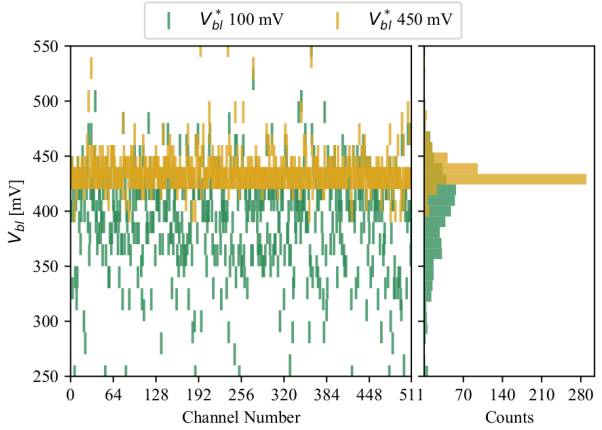


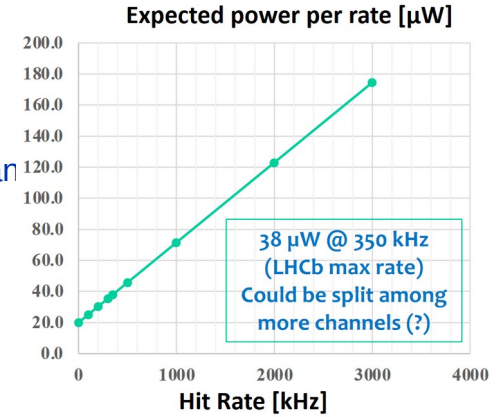
TimeSPOT: more

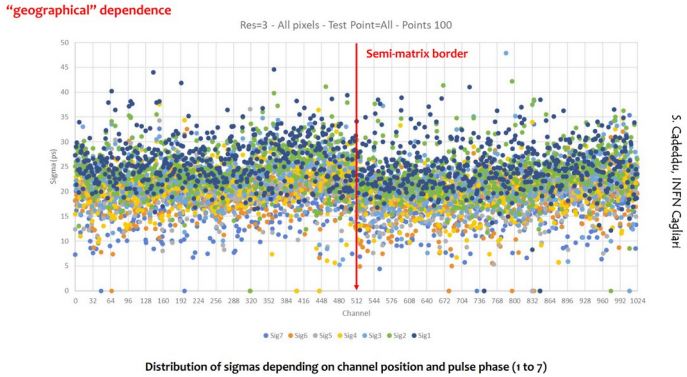
Signal and TDC test pulse capabilities allow time resolution measurements for the analogue an TDC contributions

- Digital and analogue services distributed to 2x16 pixel blocks
- No dead area (reduced pixel pitch)









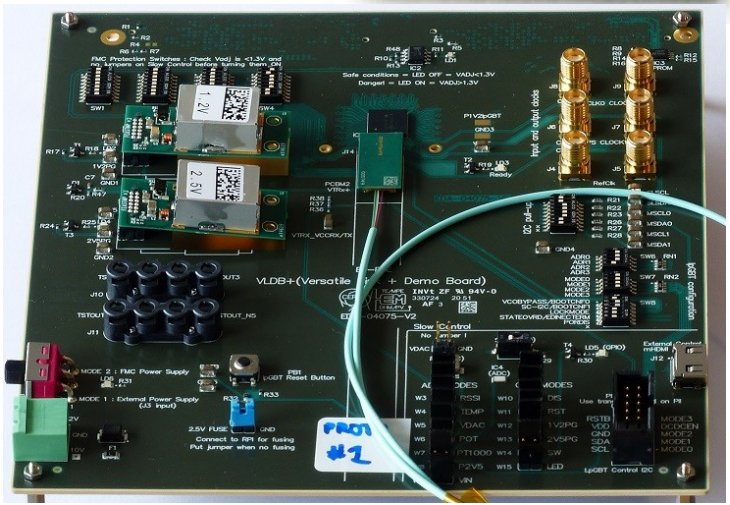
Offset- compensation bug

FE ASICs control and timing distribution

We need a fanout control ASIC for the VeloPix 2

- The avaliable ASIC is the lpGBT and most probably the only one avaliable in LS4 timeline.
- Some possible issues:
- Only 4 PSCLK (to be taken in account for the future) (8 in GBTx).
- Min delay 50 ps. It is possible to have the alignment below 50 ps in the VeloPix 2 ?
- Similar radiation damage as the GBTx (far from FE ASIC)
- Higher rates that GBTx on the eports (80 MHz, 160 MHz).
- How to have a low jitter timing reference?

We recently acquired a VLDB+ to integrate the control with PicoPix



Upgrade I readout architecture