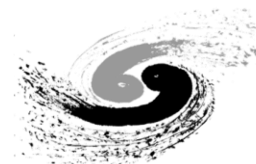
HEPS-BPIX40: The Upgrade of the Hybrid Pixel Detector for the High Energy Photon Source

Jie Zhang on behalf of the detector design team
Institute of High Energy Physics, CAS

TWEPP 2023, Geremeas, Sardinia, 2023-10-05

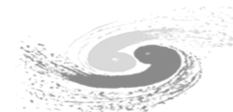


Institute of High Energy Physics
Chinese Academy of Sciences

Outline

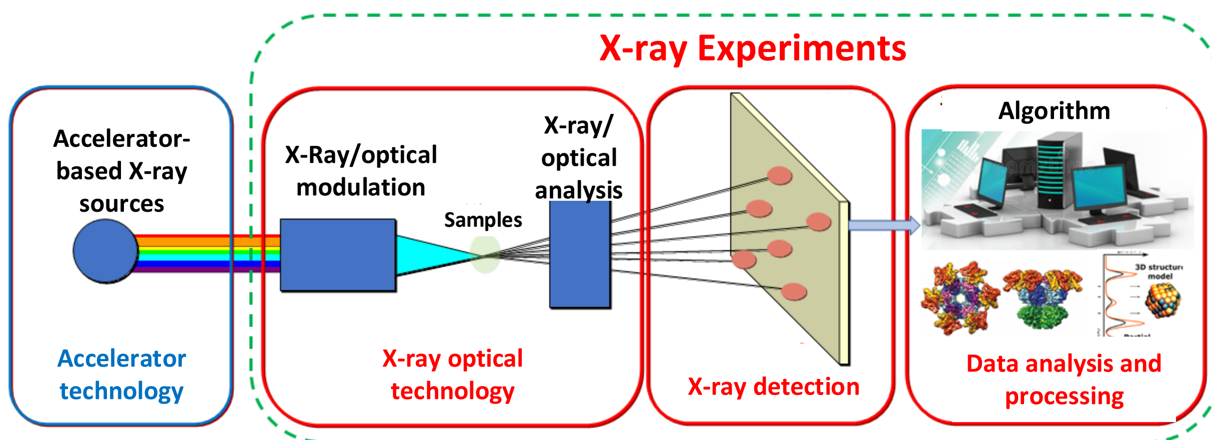
- **Background & Requirements**
- **Hybrid Module**
  - **ASIC Upgrade**
  - **Front-end Module Upgrade**
  - **Single Module Test**
- **Electronics System**
  - **FPGA Readout Board Upgrade**
  - **Clocking**
- **Summary**

High Energy Photon Source (HEPS)



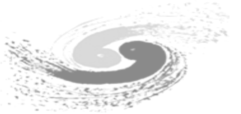
- Fourth-generation synchrotron light source
- Under construction at Huairou District, Beijing
  - Start the user operation in 2026
- Key-parameters for beam

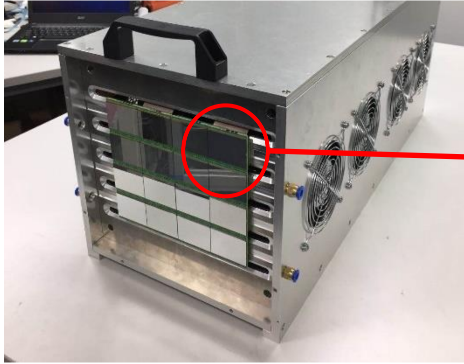
Parameters	Nominal
Beam energy	6.0 GeV
Emittance	better than 0.06nm×rad
Beam	Higher than 1×1022 phs/s/mm2/mrad2/0.1%BW
Spatial resolution	10 nm
Energy resolution	1 meV
Photon energy	Up to 300keV



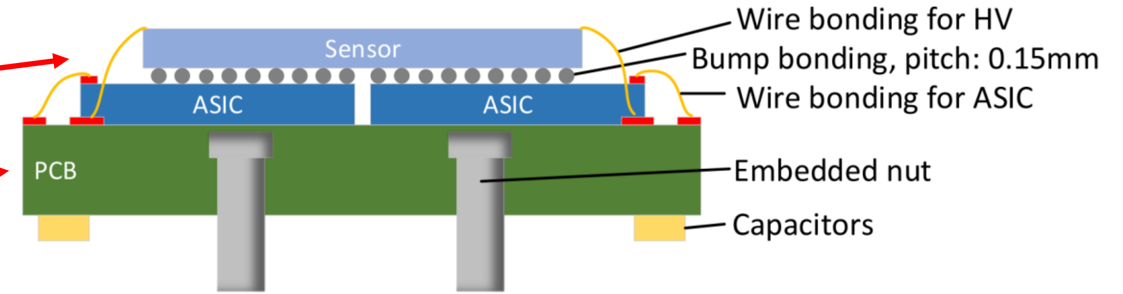
- HEPS Phase I plans 14 beamlines with the area array pixel detector in 2025
  - Detectable energy range: 8-20 keV
  - Spatial resolution: 140 μm
  - Total pixels: 6M, 2M, 1M, & 150K
  - Frame rate: Up to 2 kHz
- Ref: http://english.ihep.cas.cn/heps/index.html

Hybrid Pixel Detector

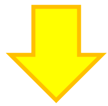


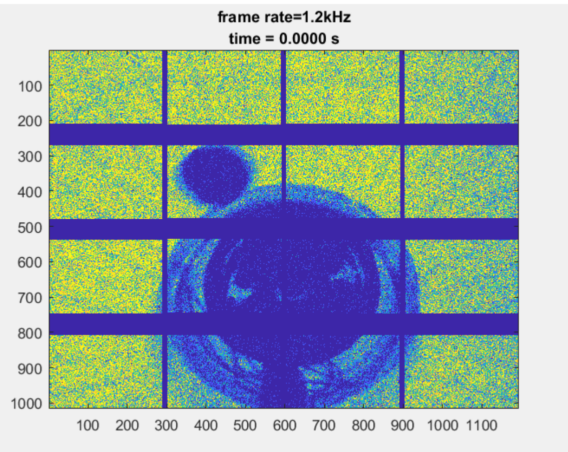


Front-end modules



Cross-section of the front-end modules



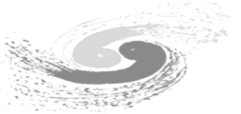


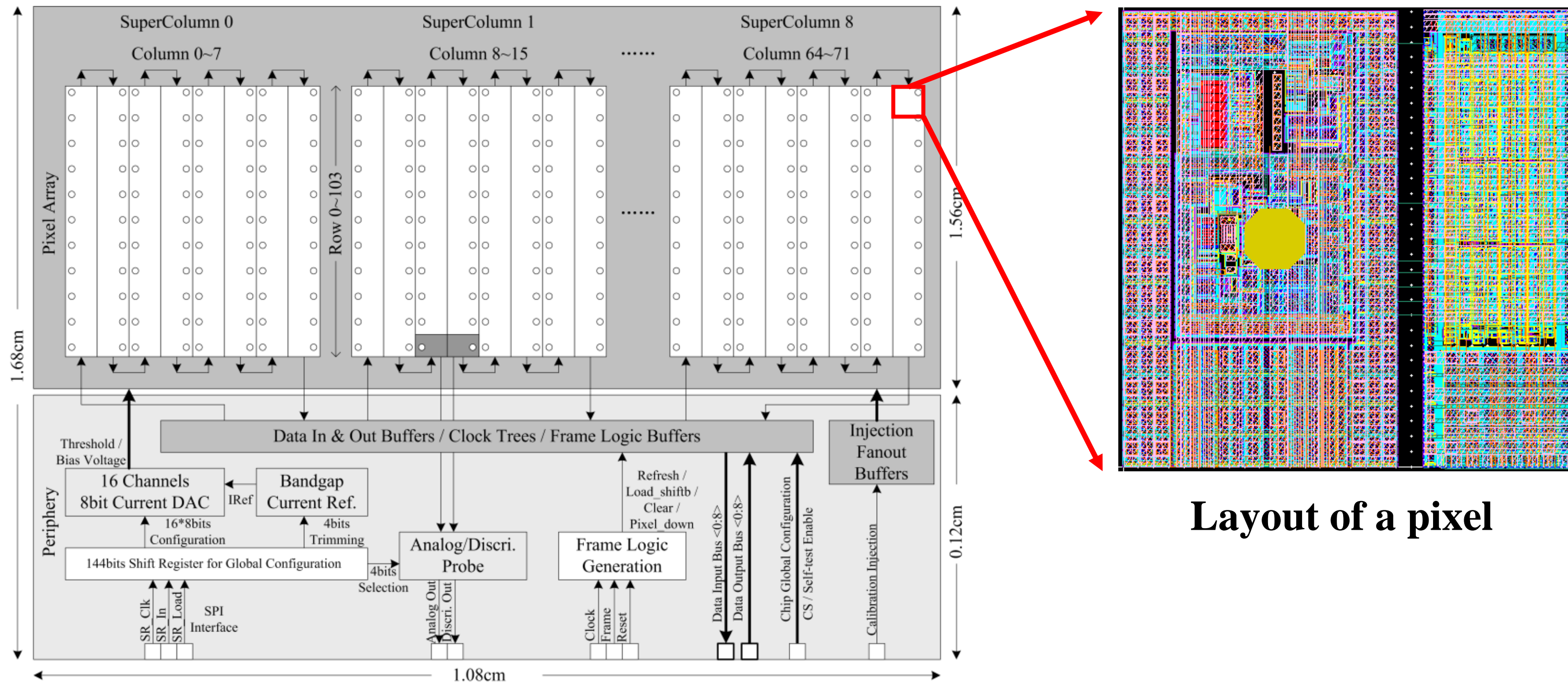
Dynamic image

- Image recorder
  - Assembled from multiple front-end modules

- Front-end modules
  - Sensor
    - An array of individual pixels arranged in a grid pattern
    - Convert the incident radiation into electrical signals
  - Readout ASIC
    - An array of individual pixels match with sensor
    - Amplify electrical signals and process to generate a digital image or data
  - Module hybridization
    - One sensor bump-bonded with multiple readout AISCs

Photon Counting Readout ASIC: BPIX



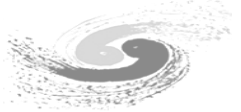


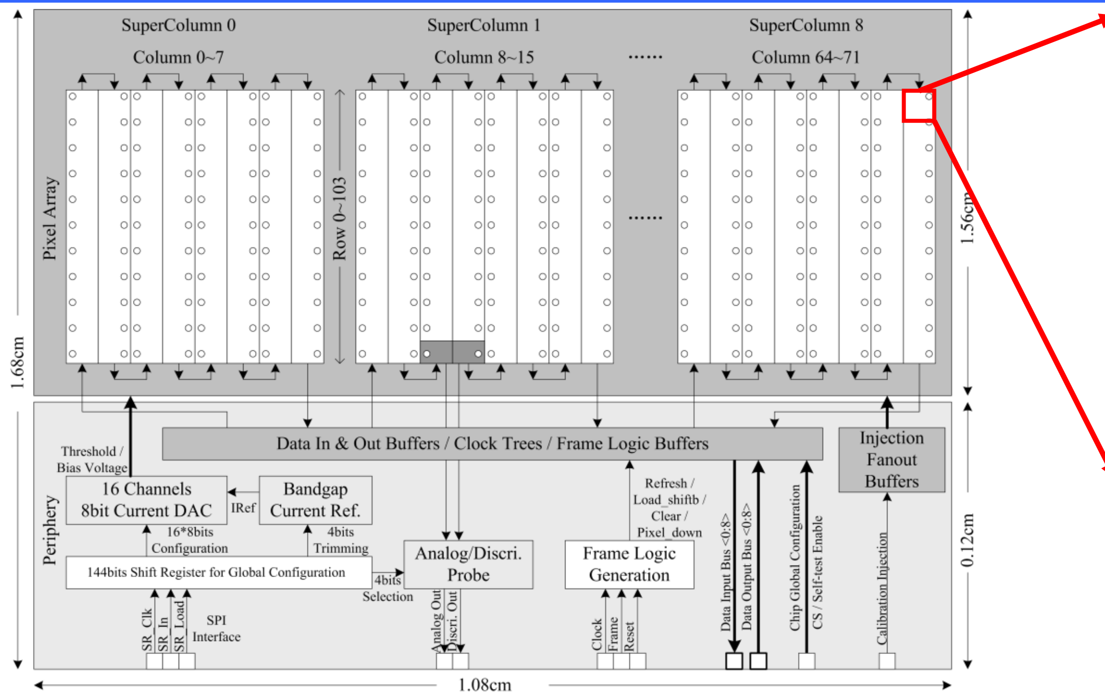
Layout of a pixel

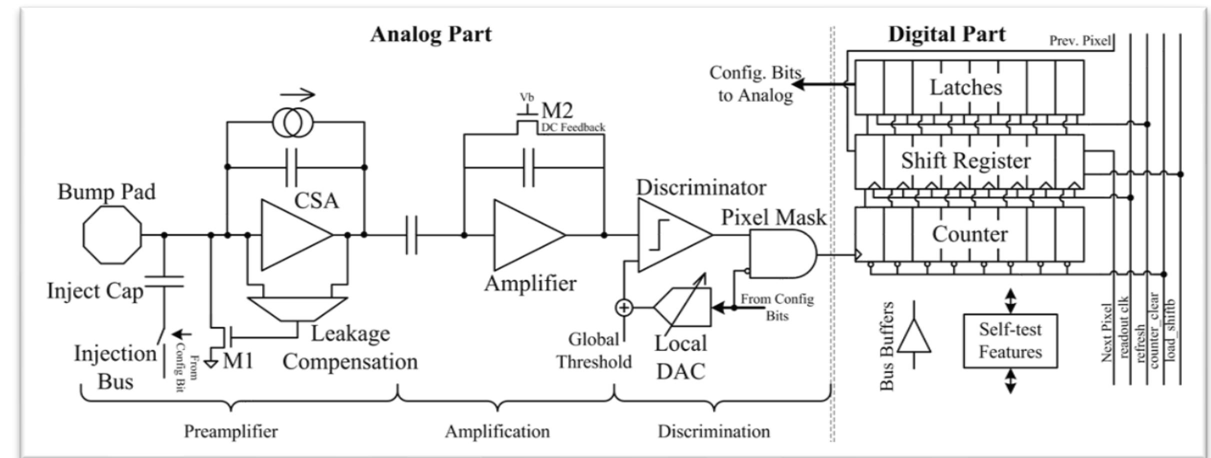
Chip architecture

- Pixel cells organized in array, connected in series, read out by shift chains
- Peripheral part
  - Config, control, data packaging & monitoring

Photon Counting Readout ASIC: BPIX







- Pixel cell:
  - Electrical signal amplified with a low noise amplifier, shaped through a shaper and then discriminated with an adjustable threshold
- Threshold setting:
  - Global DAC for the coarse threshold
  - In each pixel cell, local DAC for the fine threshold
- Once the amplified signal exceeds the threshold, the counter adds 1.

Photon Counting Readout ASIC: BPIX

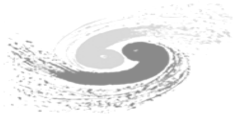
Specs	BPIX-20	BPIX-40
Pixel size	150 µm X 150 µm	140 µm X 140 µm
Pixel Array	104 X 72	128 X 96
Thresholds	1	2
Gain	Fixed	2 bits tunable
Counting rate	> 2 Mcps	> 2 Mcps @ Med gain
Frame rate	1.2 kHz continuous	2 kHz continuous
Counting Depth	20 bit	14 bit

BPIX photon counting chips

- CMOS 130nm, 1P8M

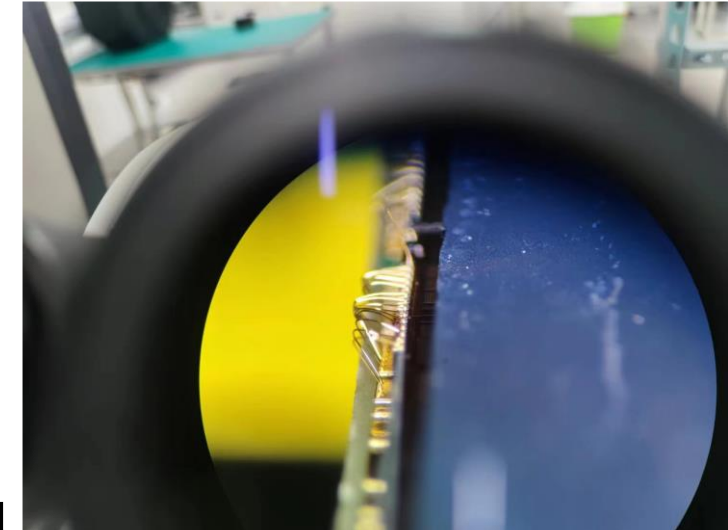
Probe Card Test – ATE (Automatic Test Equipment): Yield of a 12-inch wafer > 95%

Module Assembly Evolution

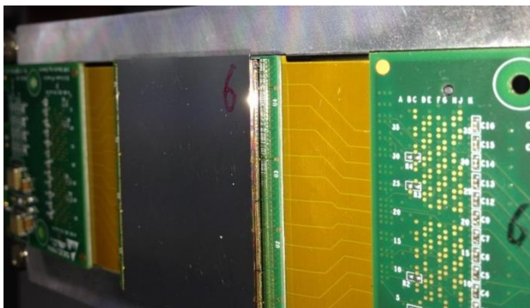


Module assembly was evolved in four generation of prototype systems:

- **Indium bump used for the 1st, nice yield but low productivity**
  - **Low temperature in the full product flow was an issue**
- **CuSn bump for the 2nd, high productivity for mass production, and high temperature compatible**
- **TSV (Through Silicon Via) features added in the 3rd to eliminate the wire bonding for ASIC (not for sensor), for smaller module assembly gaps**
  - **But found long-term stability problem**
- **Back to CuSn bump for 4th, but with ASIC pin map optimization and advanced wire-bonding, the non-detectable area is even better than the TSV version**

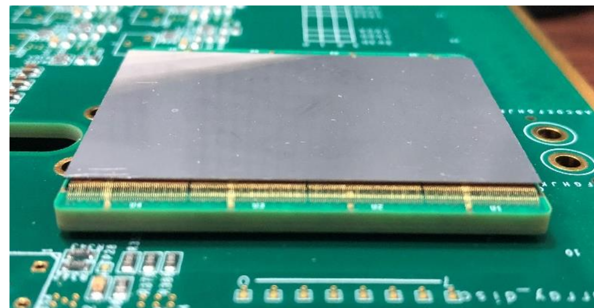


Advanced wire-bonding



Indium bump bonding module for the 1st prototype

J. Zhang *et al* 2017 *JINST* **12** C01041



CuSn bump bonding module for the 2th prototype

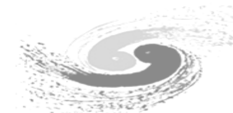
J. Zhang *et al* 2019 NIMA **958** 162488

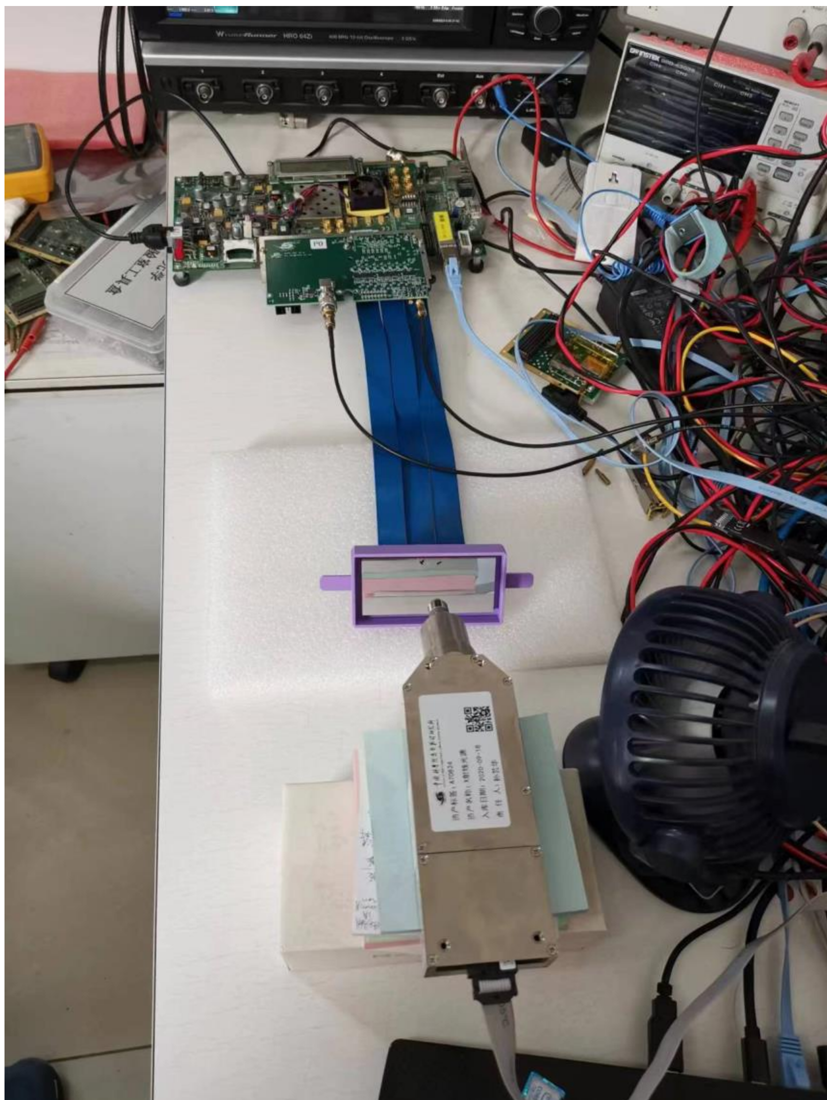
Bump bonding + TSV module for the 3rd prototype

J. Zhang *et al* 2020 NIMA **980** 164425

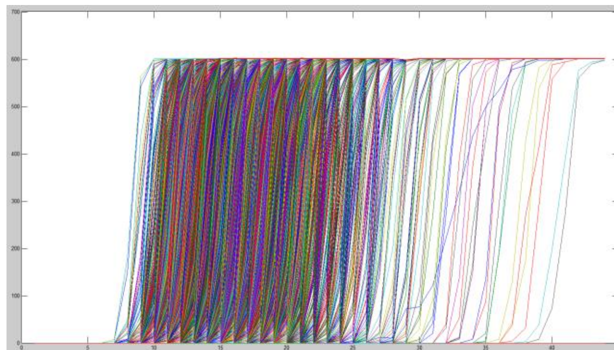
CuSn bump bonding module for the 4th prototype after ASIC pin map optimization

Single Module Test

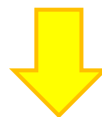


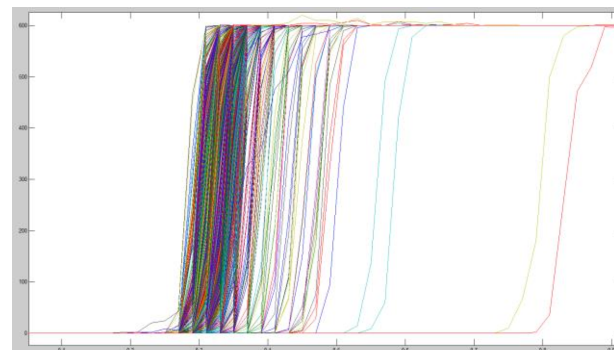


- **Single module passed the preliminary tests**
  - **All functions are as expected**
  - **Reliability tests in progress**



Threshold scan before calibration





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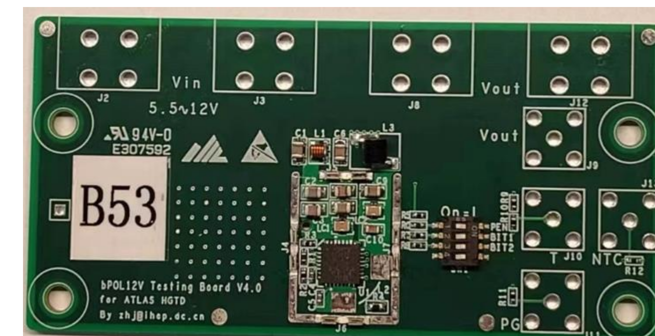
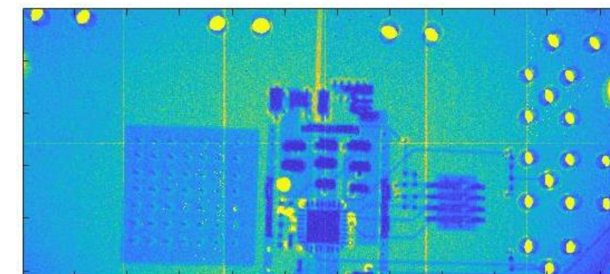
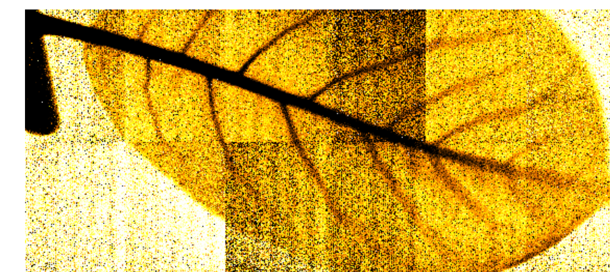


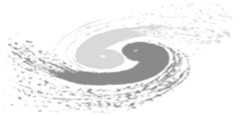
PCB for bPOL12v in ATLAS HGTD



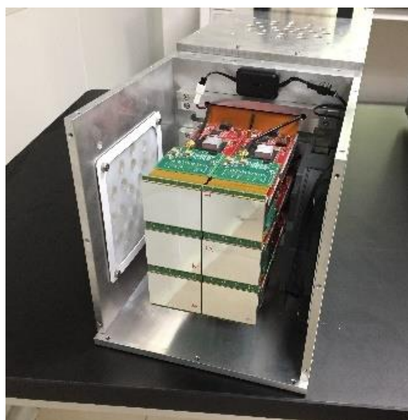


Preliminary X-ray image (uncalibrated)
A leaf exposed by an Au X-ray tube with 15 kV and 200 μA current for 0.3s

Prototype Systems Evolution

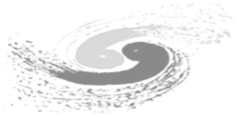


	1st BPIX（2015-2016）	2nd BPIX（2017-2018）	3rd BPIX（2019-2021）	4th BPIX（2022-now）
Modules	6	16	24	40
Pixels	360K	~1M	1.4M	6M
Assembly Scheme	Wire bonding & Rigid-flex PCB	Wire bonding & Rigid-flex PCB	Through Silicon Via (TSV) & Rigid-flex PCB with low CTE (coefficient of thermal expansion)	Advanced wire bonding & HTCC (High Temperature Co-Fired Ceramic)
Dead Area Occupancy	26.3%	26.3%	11.8%	~9.3%
FPGA Board	Spartan6 + SFP	Kintex7 + DDR3 + Molex Nano-Pitch I/O™ Cable	Kintex7 + DDR3 + Molex Nano-Pitch I/O™ Cable	UltraScale Kintex Plus + DDR4 + MicroTCA.4
DAQ Interface	1G Ethernet x12	1/10 G Ethernet x4	10G Ethernet x 4	100G Ethernet
Power	100W	370W	500W	<2500W



Under development

Prototype Systems Evolution



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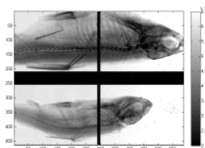
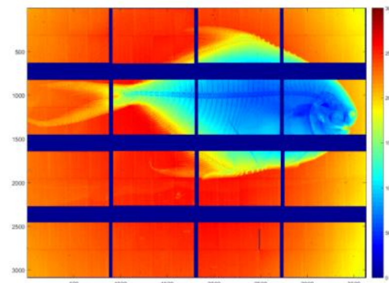
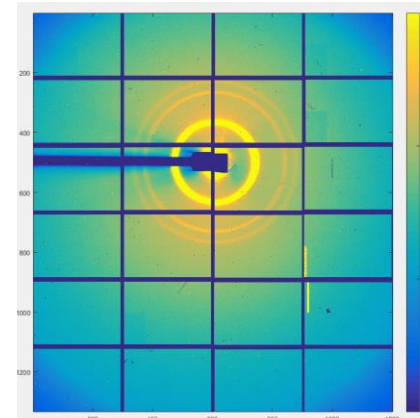
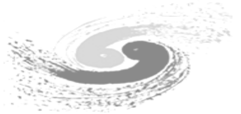






Electronics System Architecture



Readout Electronics
10GbE
N=20
Readout Electronics
10GbE
Network Switches
100GbE x2
High performance servers
In MicroTCA.4 Crates x4
1GbE
Control & monitor
FPGA accelerator cards x2

On-detector

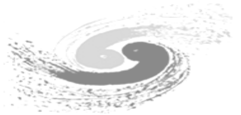
- **FPGA**
  - **Front-end Electronics Control**
  - **Clock Synchronization**
  - **Monitoring**
  - **Data Acquisition**

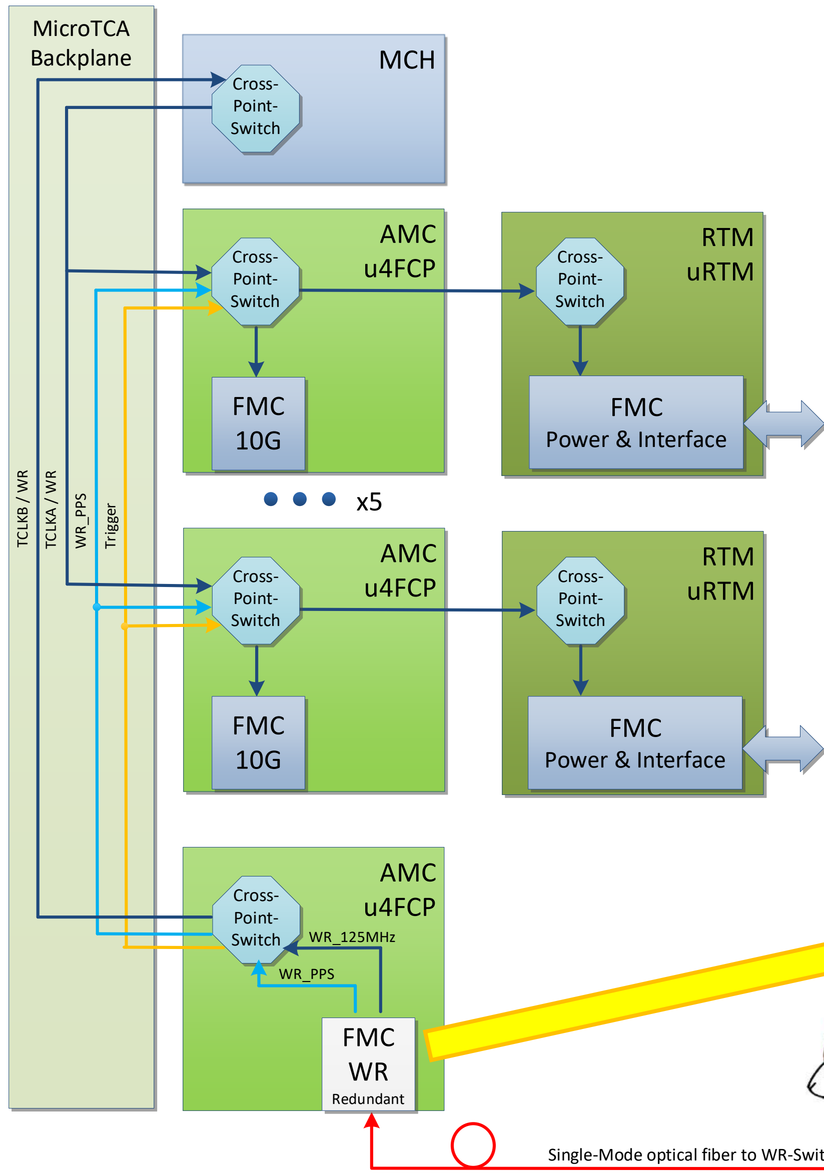
Off-detector

- **High-speed network**
- **High-speed storage**
- **High-performance computing**

- **FPGA**
  - **Data aggregation**
  - **Data sorting**
  - **Data compression**
  - **Real-time algorithm**

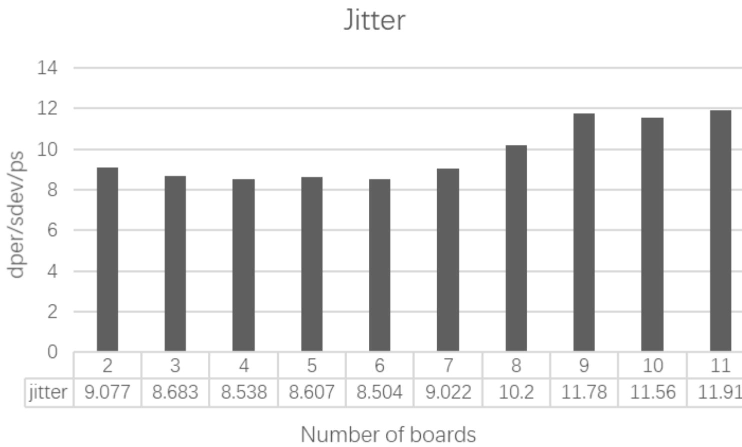
Clock distribution in MicroTCA



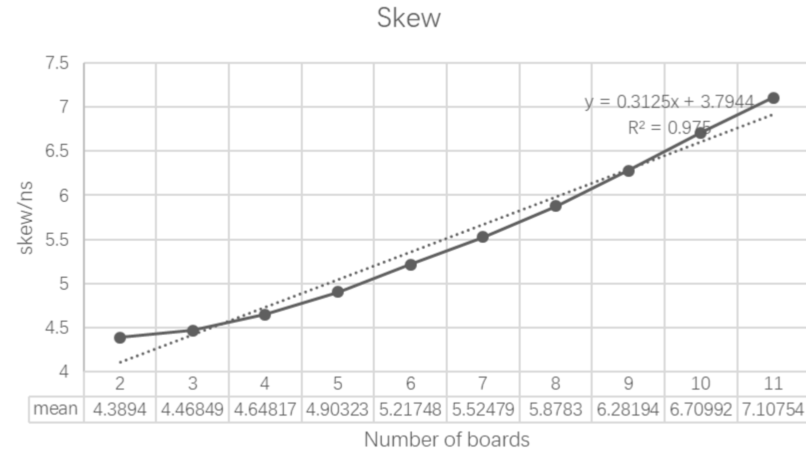


WR (white rabbit) clock synchronization

AMC with mini-WR fixed in slot 12, add more adjacent AMC boards



	2	3	4	5	6	7	8	9	10	11
jitter	9.077	8.683	8.538	8.607	8.504	9.022	10.2	11.78	11.56	11.91



	2	3	4	5	6	7	8	9	10	11
mean	4.3894	4.46849	4.64817	4.90323	5.21748	5.52479	5.8783	6.28194	6.70992	7.10754

Mini-WR FMC for System-level clock synchronization

Skew:

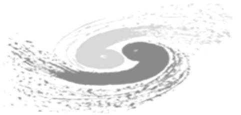
- **About 312 ps delay between adjacent slots**

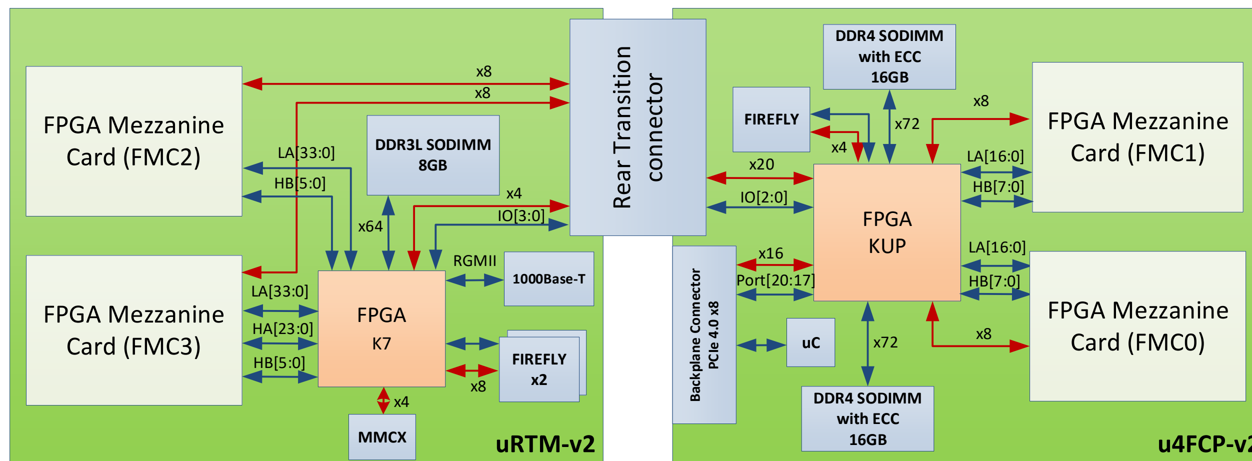
Jitter:

- **<12 ps**

Meet the BPIX requirements

FPGA board





- uRTM-v2
- u4FCP-v1

u4FCP & uRTM：

FPGA-based MicroTCA compatible AMC board

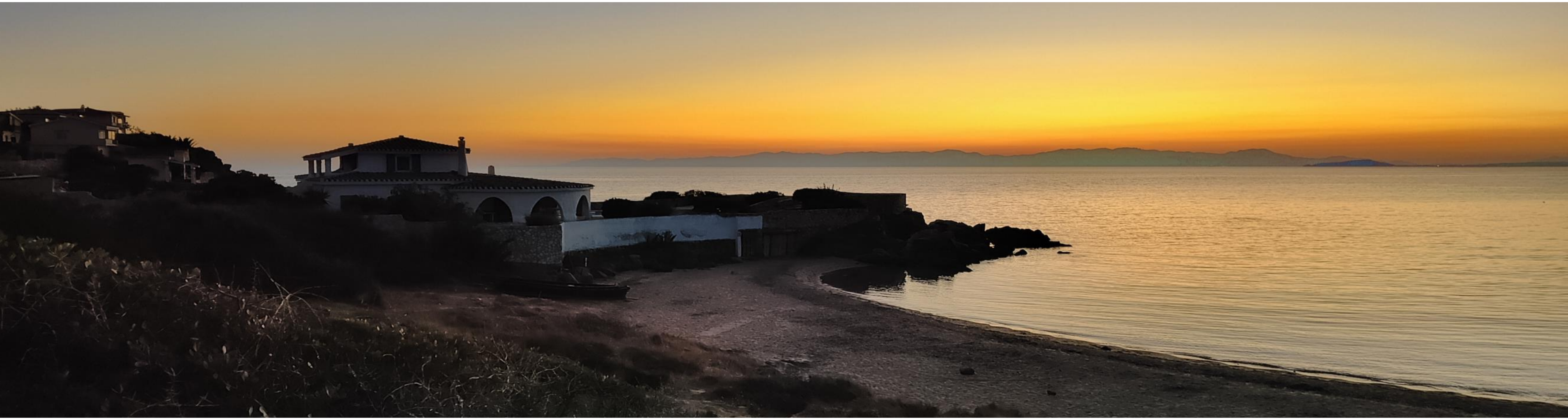
- For generic system control and data acquisition in HEP/HEPS experiments
- Conceived to serve a mid-sized system residing either
  - inside a **MicroTCA** crate or
  - **stand-alone** on desktop with high-speed optical links or Ethernet to PC
- HPC FMC sockets
  - Provide additional clock signals, user-specific I/O and high-speed transceivers that can be used to extend the connectivity as well as the I/O bandwidth
- The red lines are high-speed serial links connected to the gigabyte transceivers (GTY/GTH/GTX) of the FPGA. The blue lines are the general input/ outputs connected to the High Performance (HP), High Range (HR) or High Density (HD) banks of the FPGA.
- More details:
  - https://github.com/palzhj/u4FCPv2

Summary

HEPS-BPIX40

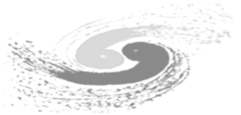
- An new hybrid pixel detector for the High Energy Photon Source

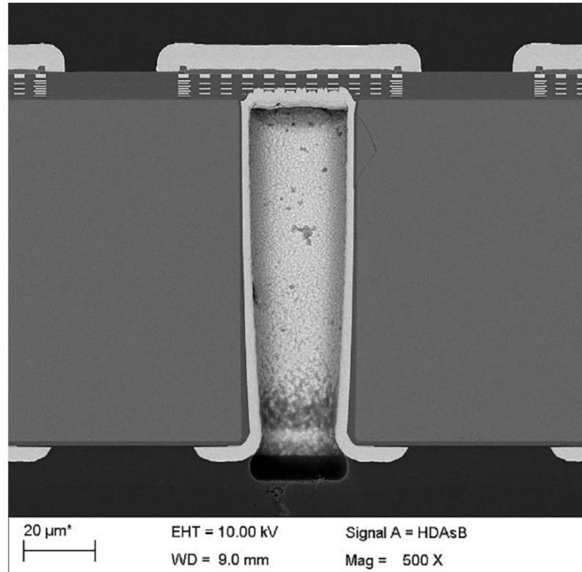
- Dual-threshold photon counting ASIC
  - Complete the engineering run and probe card test, yield > 95%
- Front-end module
  - Complete small batch assembly, pass the preliminary tests, under reliability tests
- 6M prototype system
  - Complete hardware design and production, firmware and software development in progress
  - Expected to be ready for beam testing by the end of this year



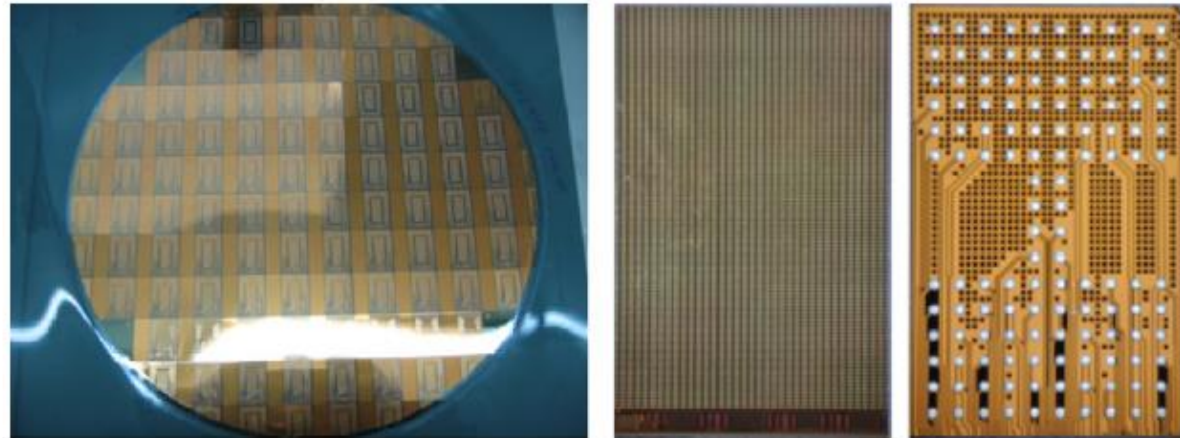
THANKS TO YOUR ATTENTION

Bump bonding & TSV features

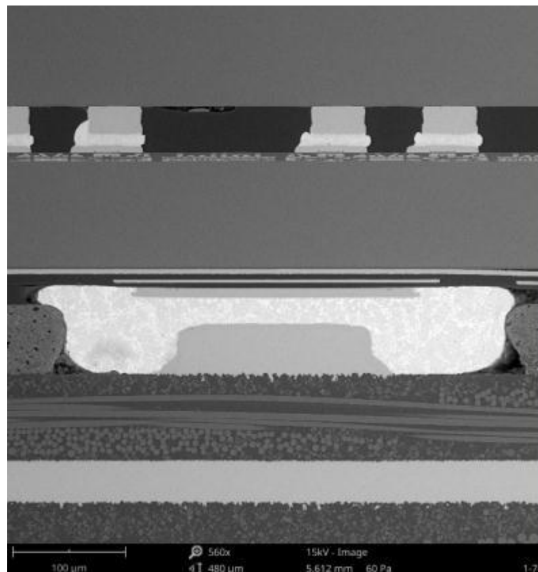




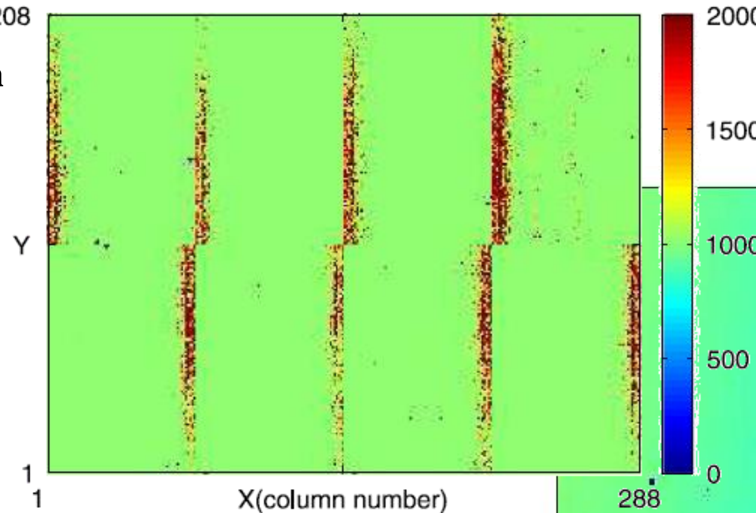
Cross-section view of a TSV connection



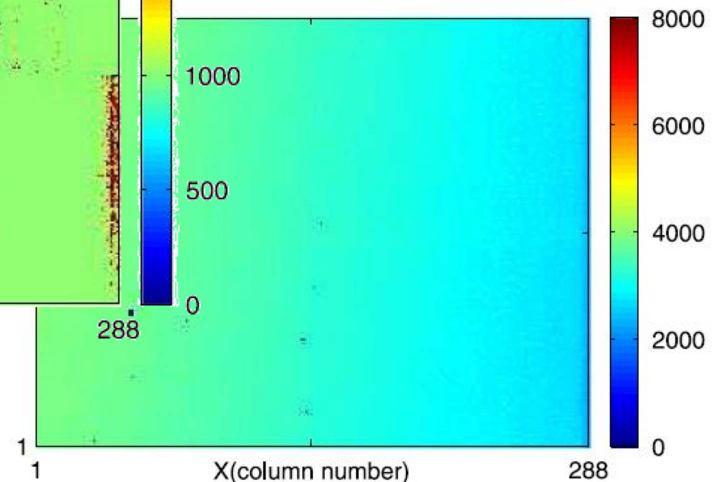
Wafer after TSV processed, top view with bumps, backside view with RDL



Cross-section view of a Bump Bonding +TSV 3D stack

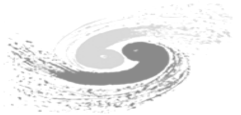


TSV with single-layer RDL



TSV with double-layer RDL

uFC Series Board



uFC v2
- Xilinx Kintex-7 28nm 7K325T
  - 0.32 Million System Logic
  - 840 DSP
- PCIe2.0 x4
- 8GB DDR3 800MHz SDRAM ECC
- (8+2)*10G High-Speed Serial Links

u4FC&P v1
- Kintex Ultrascale+ 16nm KU11P
  - 0.65 Million System Logic
  - 2928 DSP
- 4*PCIe4.0 x4 + PCIe4.0 x8
- 2*16GB DDR4 1200MHz SDRAM ECC
- 4*40G/100G High-Speed Serial Links

u4FC&P v2
- Kintex Ultrascale+ 16nm **KU15P**
  - 1.14 Million System Logic
  - 1968 DSP
- SAMTEC Firefly x3 + PCIe4.0 x8
- 2* 16GB DDR4 1200MHz SDRAM ECC
- 8*40G/100G High-Speed Serial Links

Name	Instance Specs					
	Status	FPGA	Memory	NVMe	PCIe BW	Network
uFC v2	Ready	7K325T	8GB	-	2 GB/s	10GbE
uFC&P v1	Ready	KU11P	2*16GB	4*(up to 4TB)	8 GB/s	40/100GbE
uFC&P v2	R&D	KU15P	2*16GB	-	8 GB/s	40/100GbE

Ref1: Zhang, J., et al. (2023). TNS **70(6): 935-940.**
Ref2: Zhang, J., et al. (2019). TNS **66(7): 1169-1173.**

FMC cards

- **AMC+RTM boards**
  - **With various FMC cards**

FPGA node

FPGA node

FPGA node

FPGA node

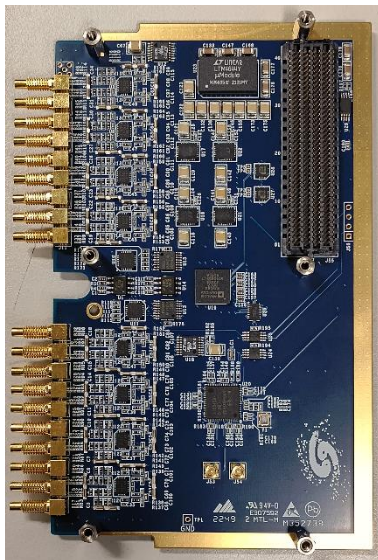
Mini-WR FMC

SFP+ x4

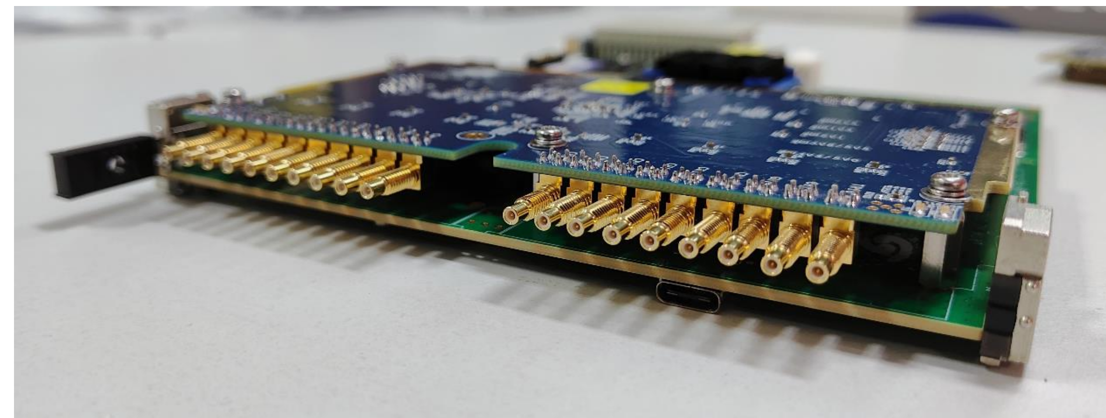
QSFP28 x2

QSFP28 x2

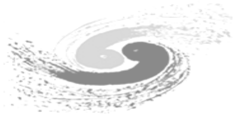
QSFP28 x2

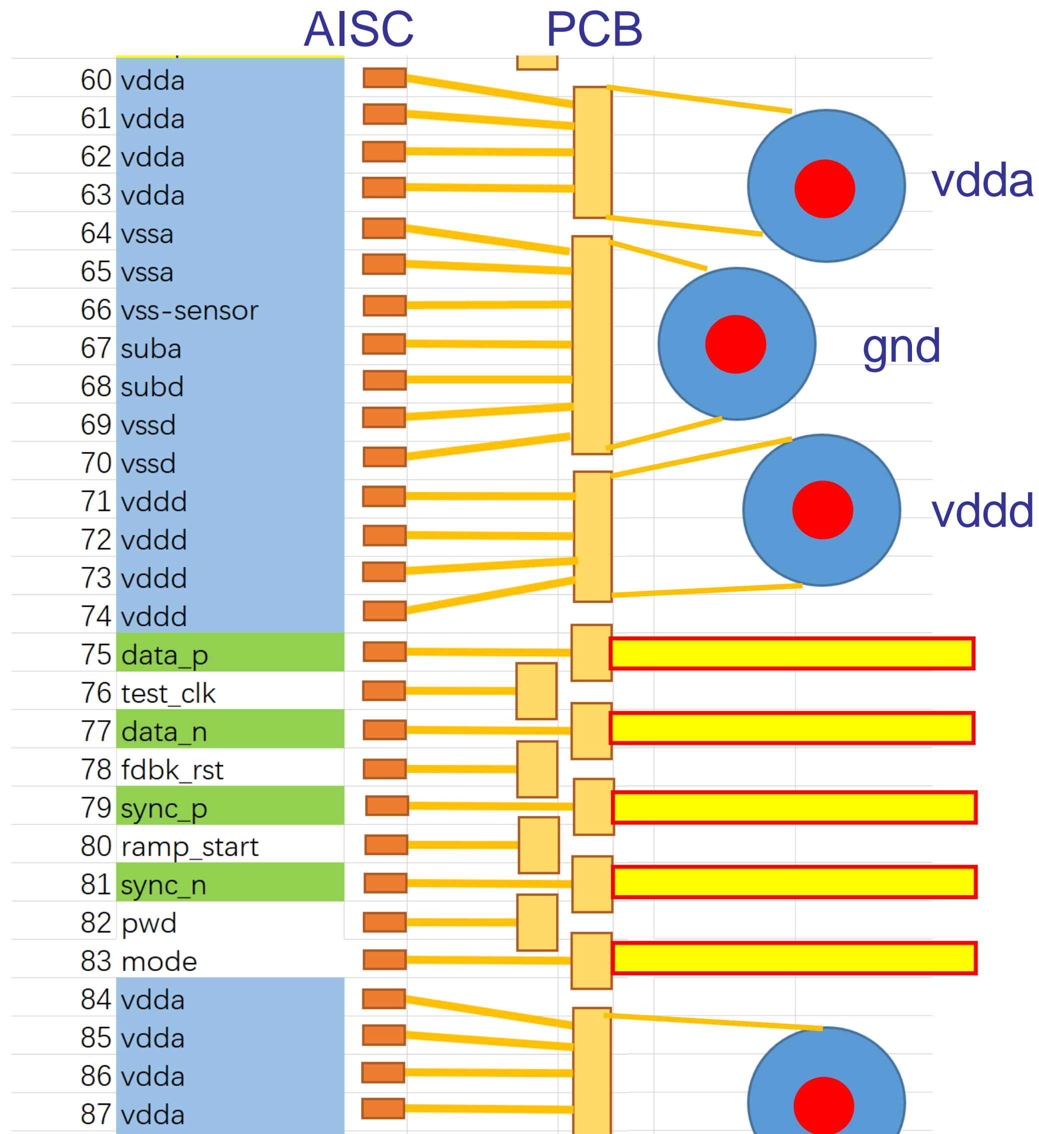


ADC FMC board
- 16 single-end channels
- 125 MHz analog bandwidth
- DC coupled analog input
- 12/16-bit Σ-Δ ADC
- Raw sample rate up to 2 GSps



ASIC pin map optimization

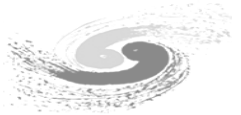




- **ASIC pin pitch: 100 um**
- **PCB pin pitch: 200 um**

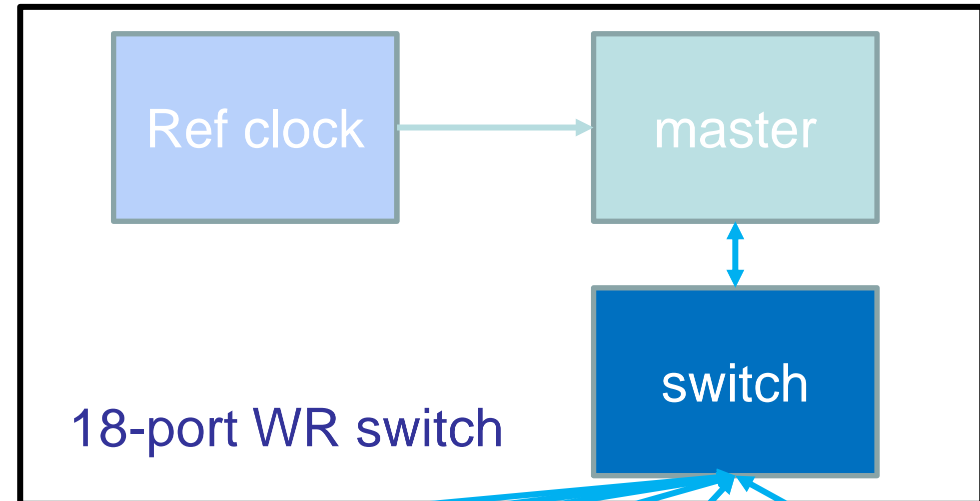
- **ASIC pin map optimization**
  - need to consider the fan-out limitation of the PCB
    - ➢ **PCB via diameter: 200 um (8 mil)**
    - ➢ **Via gap: 400 um (16 mil)**
  - Test pins and readout pins are interleaved
    - ➢ The test pin will not be used in the final product.

Clock redundancy consideration

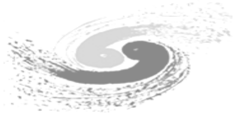


- **Due to the life limit of fiber optic transceivers, we plan to use a redundant WR clock**
  - Each uTCA crate has two WR slave nodes
  - Clock source selection
    - WR node report the loss of lock
    - DCS get the report, and configure the hardware to switch to the redundant node

The White Rabbit Project



FPGA Firmware



GbE PHY
RGMII
RTM FPGA
RBCP Register Space
RBCP to Wishbone bus
SiTCP
GMII
Ethernet Switch
GMII
PCS/PMA
RTM port
PCS/PMA
GMII
Ethernet Switch
GMII
PCS/PMA
AMC Port0
GbE
GMII
PCS/PMA
AMC Port1
GbE
Redundant modules
GMII
SiTCP
SPI master
I2C master
User application logic
USER FSM
Transmit FSM
Transmit FIFO
Receive FSM
Receive FIFO
GMII
Data Switch
Aurora
RTM port
Aurora
Data pre-processing
RBCP Register Space
RBCP to Wishbone bus
Fast control & Interlock
SPI master
I2C master
AMC Port17-20
MLVDS
SiTCP-XG
SFP+
FMC3
FMC2
FMC1
FMC0
DDR3
DDR4
AMC/FPGA

- **Config & monitor via UDP/IP**
- **Readout via TCP/IP**