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HEPS-BPIX40: the upgrade of the hybrid pixel detector for the High Energy Photon Source

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HEPS-BPIX40 is a new hybrid pixel detector for the High Energy Photon Source in China. It is a full upgrade from BPIX20, with a 128 x 96 pixel matrix and 140 μm x 140 μm pixel size. The circuit operates in single photon counting mode with dual thresholds and programmable gains. The tested frame rate is 2 kHz in continuous readout mode. A detector module covers 3.7 cm x 8.1 cm and consists of 2 x 6 chips. The full system will have 40 modules and approximately six million pixels. This paper presents the detector's design and test results.

Summary (500 words)

HEPS-BPIX is a series of hybrid pixel detectors that have been specifically designed for the High Energy Photon Source, which is currently under construction in Beijing, China. Over the past decade, three generations of prototype systems have been designed based on the former version of the BPIX20 chip. It includes a pixel matrix of 104 x 72 pixels, with a pixel size of 150 μm x 150 μm. After ten years of iteration, the demand for a full upgrade of the chip is increasing, especially in terms of periphery interface, pixel working mode, and module assembly enhancement.

We have developed the BPIX40 pixel chip as the successor to the BPIX20. It includes a pixel matrix of 128 x 96 pixels, measuring a pixel size of 140 μm x 140 μm. Dual threshold photon counting mode has been introduced for energy window discrimination, with each threshold having a counting depth of 14 bits, while the maximum counting rate can reach 2 Mcps per pixel. The measured equivalent noise was about 79 e- for the bare die, compared with 112 e- after bump bonding, using the S-curve method. Meanwhile, the non-uniformity before and after threshold equalization were 402 e- and 102 e-, respectively.

The chip was designed using CMOS 130 nm 1P8M technology on 12-inch wafers, with a manufacturing yield tested to be better than 93%. Two rows of six chips are to be bumped with a 320-μm thick Si PIN sensor to form a detector module, which covers an area of 3.7 cm x 8.1 cm. In order to minimize the assembly gap between modules, the height of all the periphery circuits has been compressed to less than 600 μm. This way, the dead zone between modules is only determined by the width of the sensor guard ring and the clearance required by wire bonding. Thus, the reliability of module fabrication is greatly enhanced compared to the TSV (through silicon via) technology used in our former systems.

96 columns of the chip were grouped into 12 super columns, each comprising 8 columns with a single readout chain implemented by a shift register. The outputs of all super columns were concentrated into a high-speed serializer and then transmitted off-chip at a data rate of 702 Mbps. At this speed, the frame rate of the chip is about 2 kHz, and deadtimeless continuous readout is supported by the systems for all modules. For the targeted 6M pixel system, the estimated maximum data rate will reach 332 Gbps at this frame rate, which poses a significant challenge for both the backend electronics and the data acquisition system.

Currently, preliminary tests have verified the module and chip design. X-ray imaging results have been obtained by a module (uncalibrated). More detailed results for the full system design will be presented in this paper.

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