SciFi Front-End Electronics: Calibration and Results on detector performance

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On behalf of SciFi Collaboration
TWEPP 2023

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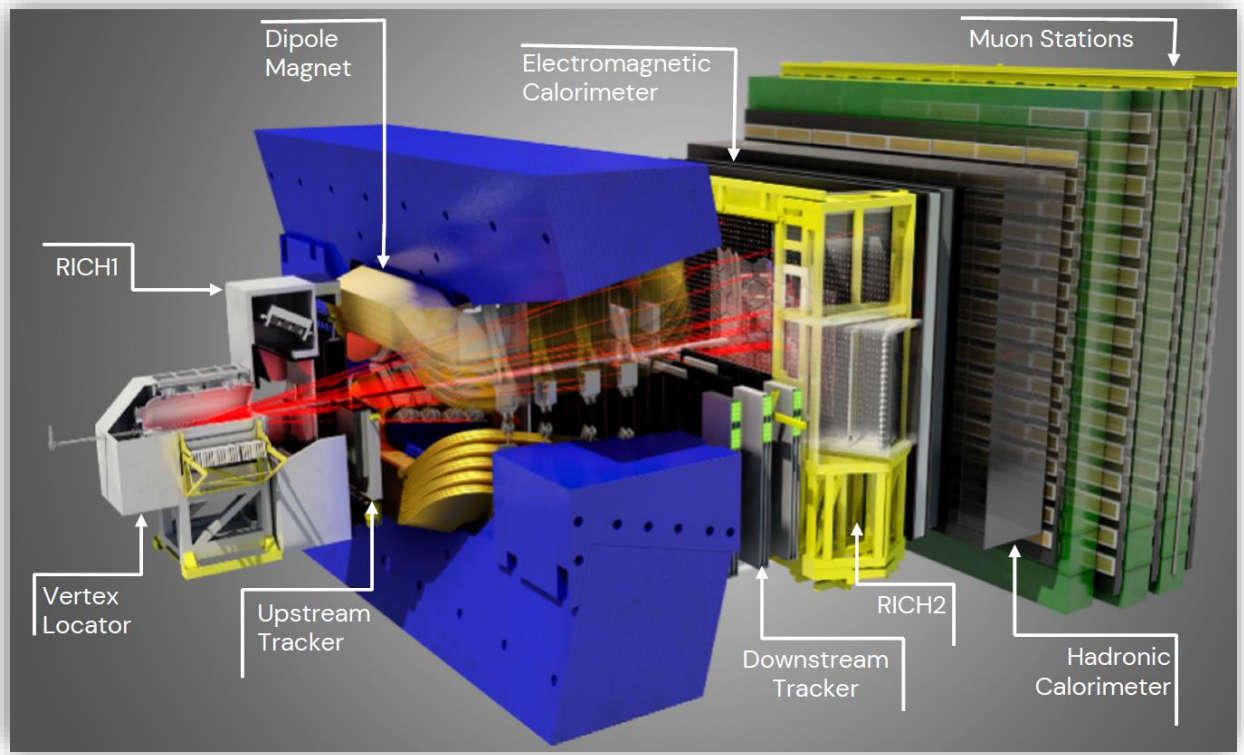
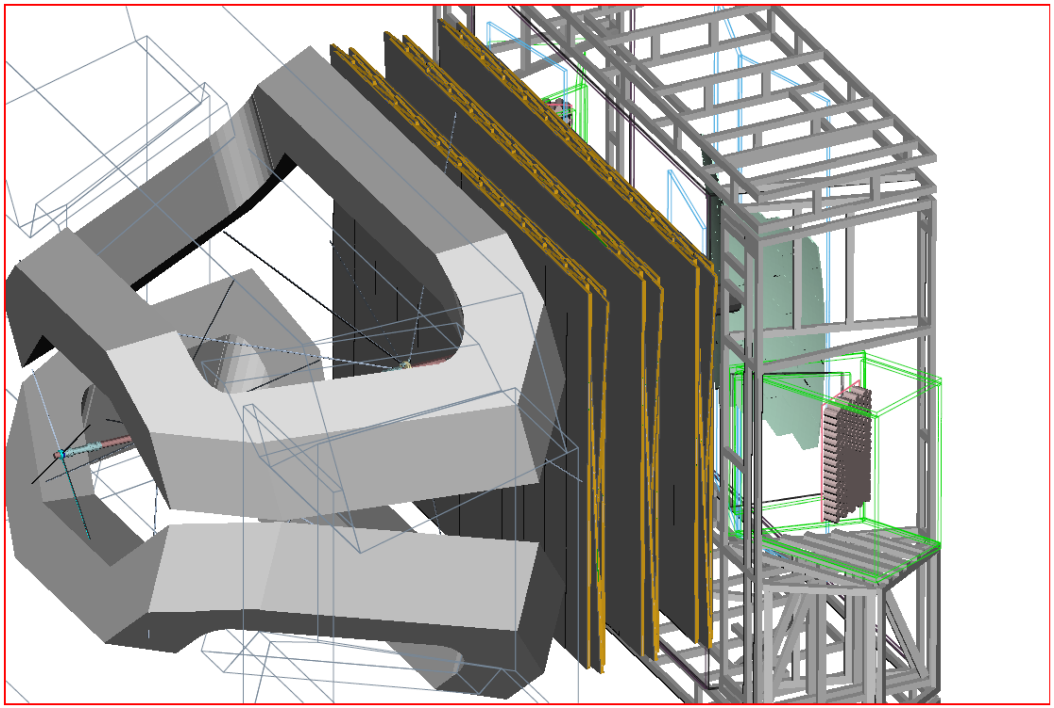
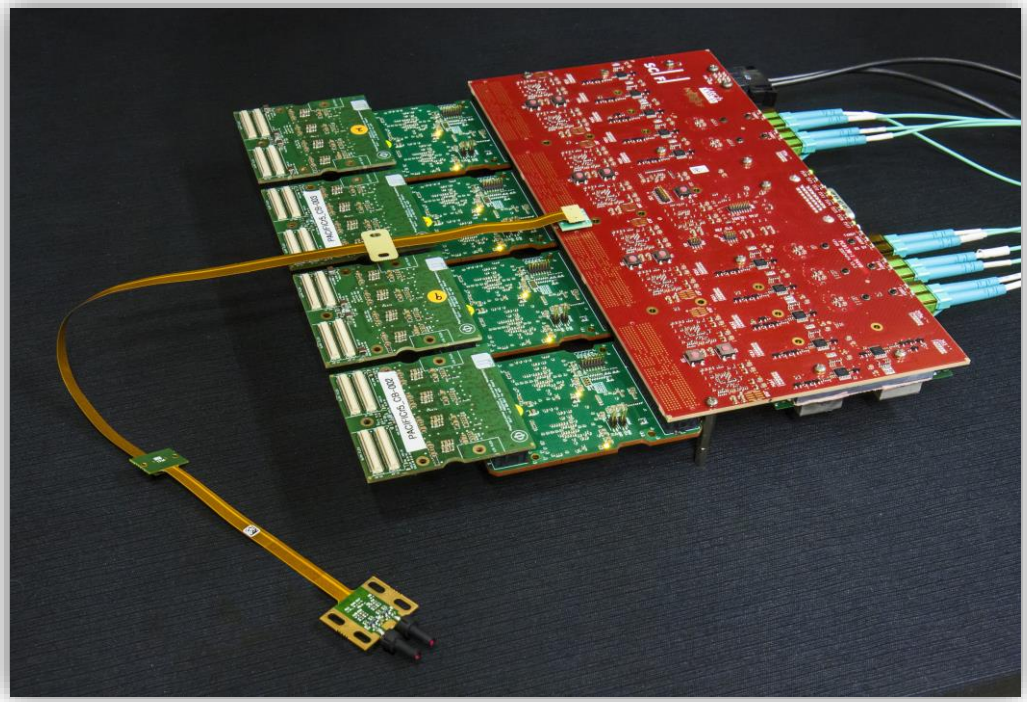
- The LHCb Experiment:
  - Single-arm forward spectrometer
  - LHC Run 1 + 2 (2011-2018): Collected > 9 fb-1
- LHCb Upgrade I: New detector readout and full software trigger at 40 MHz to cope with 5 x higher instantaneous luminosity



- The SciFi Tracker:
  - 12 layers, grouped in 3 stations:
    - 4 stereo layers per station (0°,+5°,-5°, 0°)
    - Covered area: 340 m^2, using > 10.000 km of 250µm Ø Scintillating Fiber
    - Total of 524'288 readout channels, grouped in 4'096x 4.8 Gbps Data Links



- SciFi Tracker Front-End Electronics:
  - 1 HalfROB = 1 Master Board + 4 Cluster Boards + 4 Pacific Boards + Light Inj. System;
  - Master Board = Data Transmission, Power Distribution, TFC Distribution.
  - Cluster Board = Zero Suppression (10'240 to 4'800 Mbps) and Data Encoding;
  - Pacific Board = SiPM biasing + Analog Readout + Digitization for 256 SiPM channels.



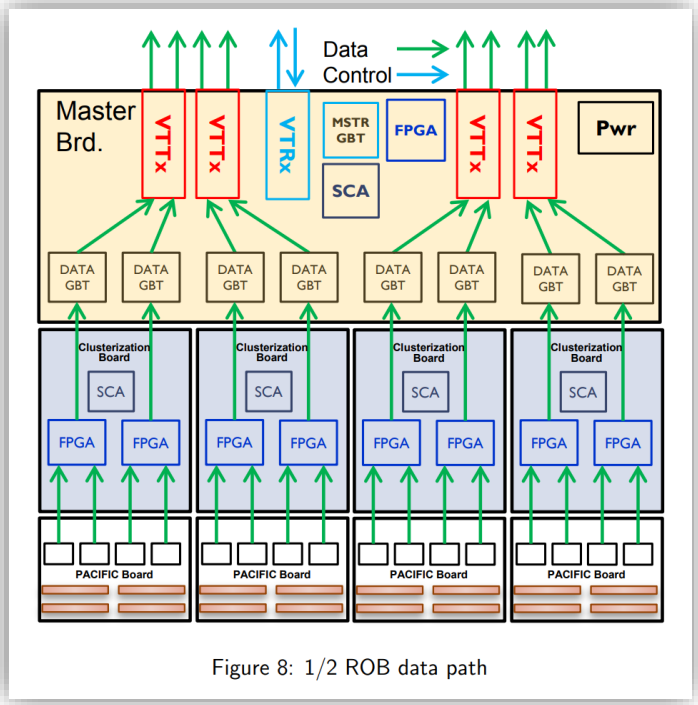


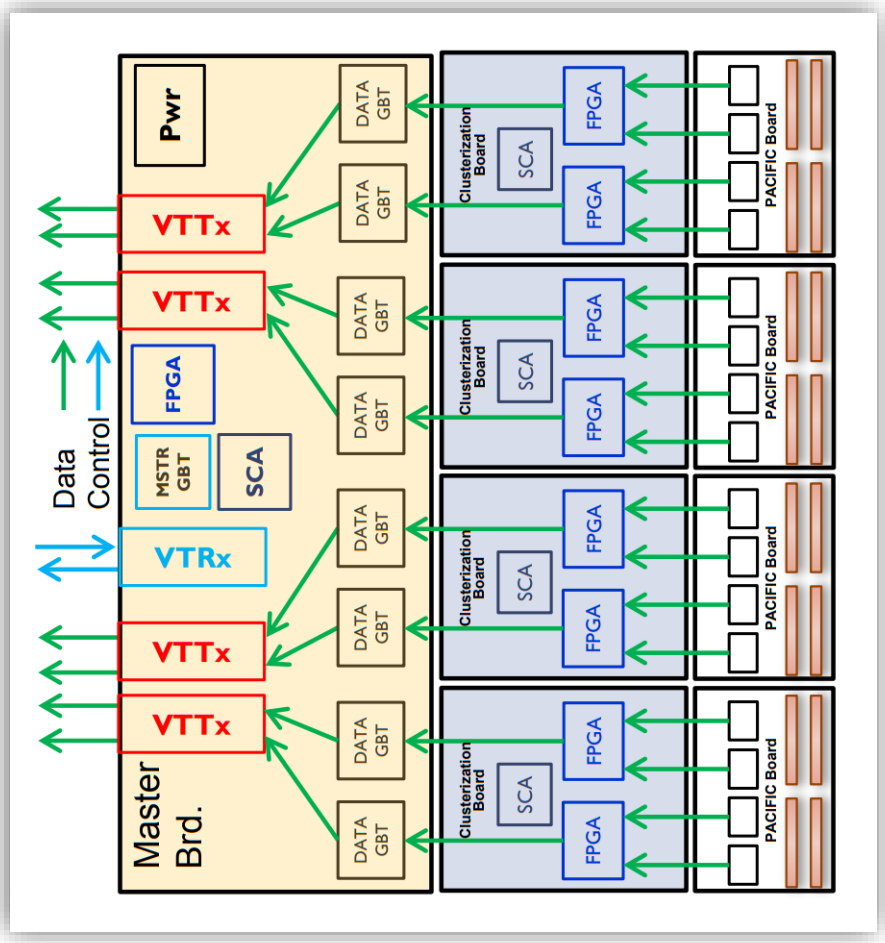
Figure 8: 1/2 ROB data path

- SciFi FEE Key Components:
  - 13x **FeastMP** DC-DC: Supply of 3v3, 2v5, 1v5, and 1v2.
  - 9x **GBTx** ASIC: Control & Data Links
  - 1x **VTRx**: 1 Bidirectional Control Link
  - 4x **VTTx**: 8 Output Data Links
  - 5x **GBT-SCA**: Wide range of multi purpose slow control interfaces

  } CERN Ecosystem

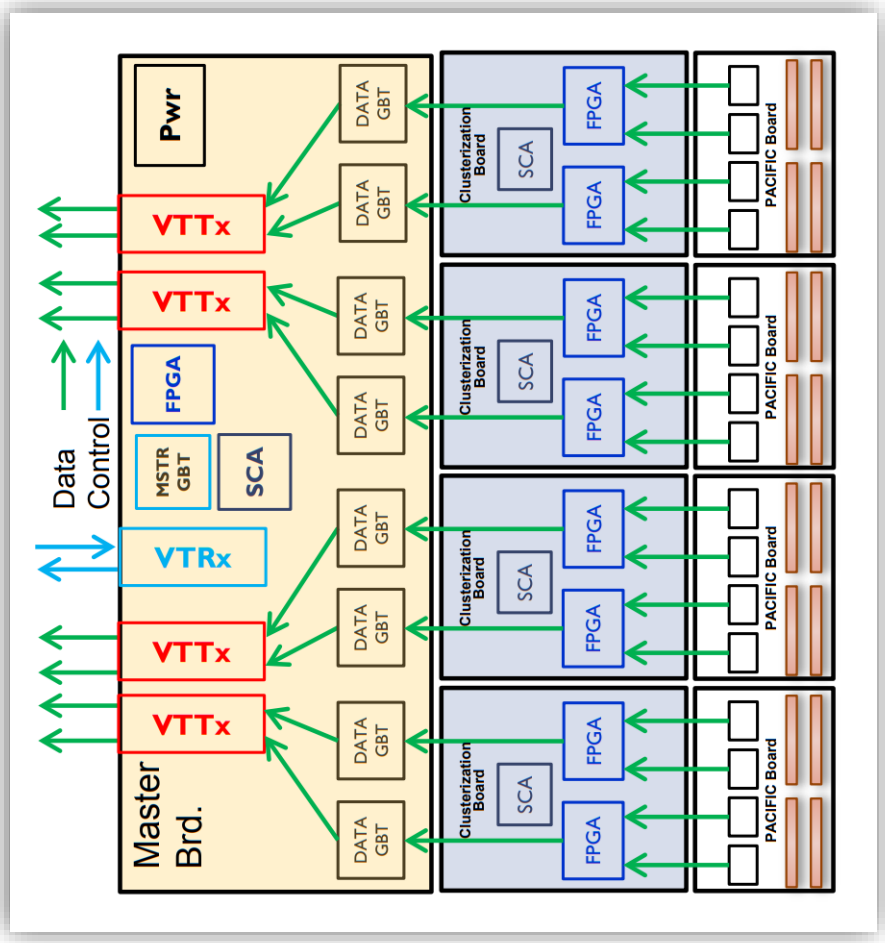
  - 1x MicroSemi **Igloo2** M2GL005 FPGA: FEE Management (**Housekeeping**)
  - 8x MicroSemi **Igloo2** M2GL090T FPGA: **Clusterization** and Data Encoding
  - 16x **PACIFIC**: Custom-Made 64 channel current mode input SiPM Readout ASIC.

- 1 Front-End Box (FEB) = 2 FEE D.U. (HalfROB)
  1 FEB = 2048-ch (1024-ch x2)
- 256 Front-End Boxes to cover 524'288-ch
- 4'096 Data Links at 4.8 Gbps = 19.7 Tbps

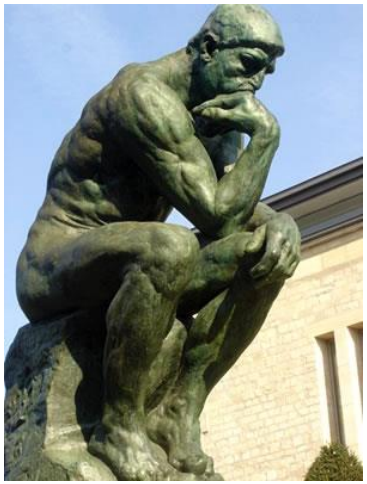


- SciFi FEE: Key Parameters to Adjust:
  - Infrastructure:
    - 4608x TX Optical Link Settings;
    - 4608x GBT Chipset Configuration;
    - 512x Housekeeping FPGA Config.;
    - 29k7 Clock Lines Phase Tuning.
  - Data Encoder, at CB FPGA:
    - 4096x Data Format Selection (FF/FV);
    - 16k4 Test Pattern Injection Points;
    - 524k Channel Masking.
  - Readout ASIC (PACIFIC):
    - 4096x Input Gain and Offset;
    - 49k PZ Shaper Settings;
    - 1M05 Integrator Trimming;
    - 1M57 Threshold Levels.

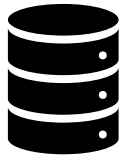
And (much) others...



How to manage all parameters of Half Million Channels ???

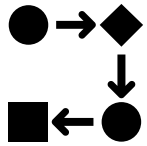


- SciFi Database Tables:



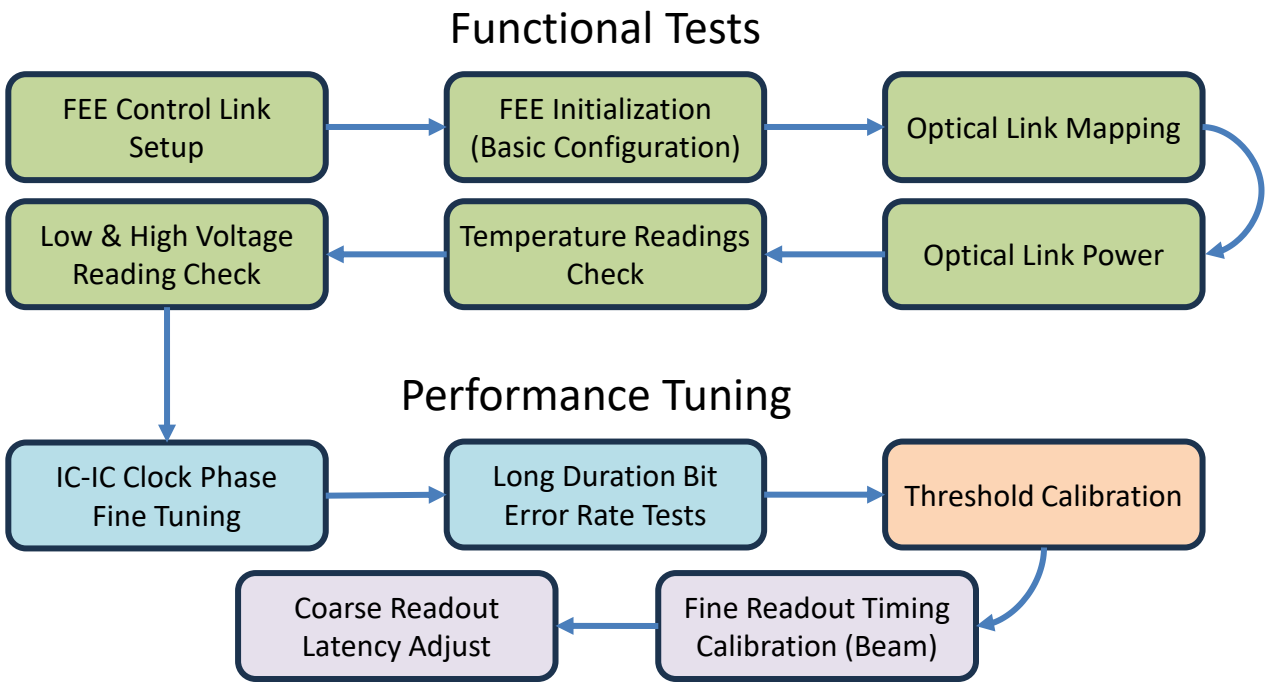
1. **Geographical:** Where detector elements are located;
2. **Run-Parameters:** Run-Dependent Detector Settings;
3. **Components tables:** Information about specific components;
4. **PACIFIC Configuration:** PACIFIC settings (like gain an PZ shaper);
5. **Calibration Runs:** Log of all the Calibration RUNs taken, storing its conditions (like SiPM Overvoltage and Temperature).
6. **Calibration Results:** Holds the results of calibration runs.
7. **Recipe Creation Table:** Keeps track of every recipe created.

- SciFi Calibration Software:

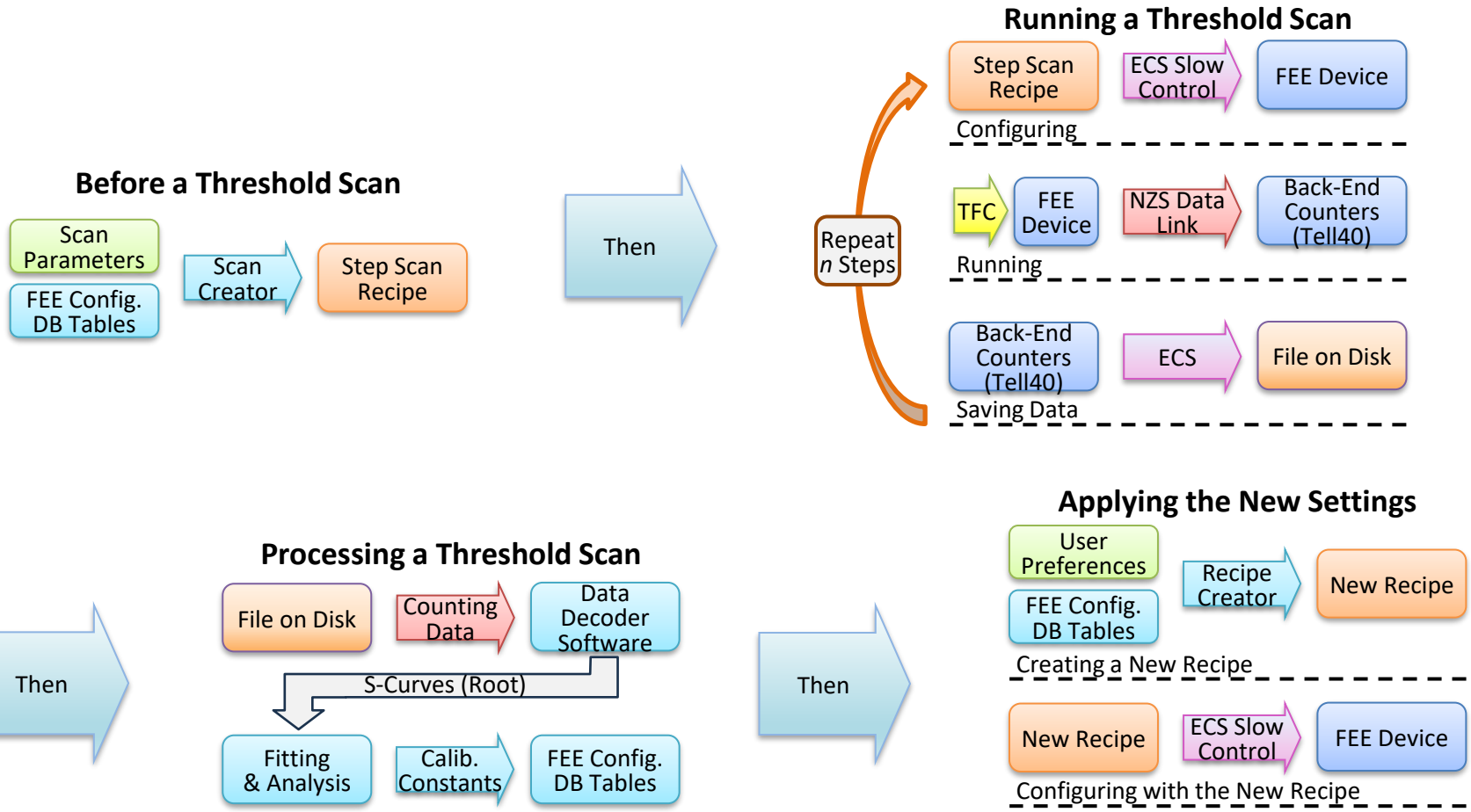


1. **Threshold Scan Software Toolbox:**
   Counter Data Decoding + Fitting + Analysis;
2. **Timing Scans Software Toolbox:**
   For IC-IC and Readout fine/coarse timing tune;

- Commissioning roadmap:
  - Sequence of checks and calibration procedures to integrate a FEE Device on the System;
    - Checks to ensure quality of Optical Links, SiPM Connection, Geographical Mapping…
    - Calibration to compensate Manufacture Tolerances, Cabling, SiPM, aging…



- Workflow for Calibration Scans:
  Threshold Scan (with Light Injection) as illustration
- Similar structure for Timing Scans



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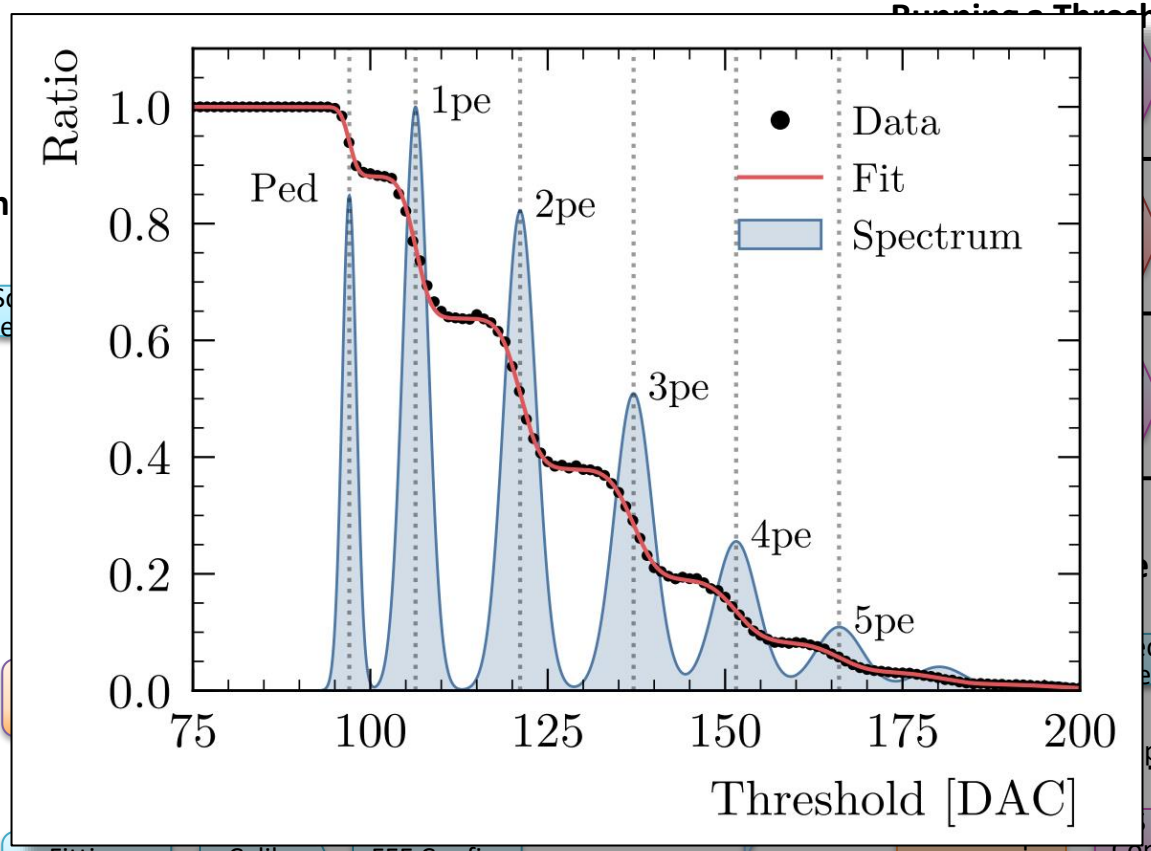
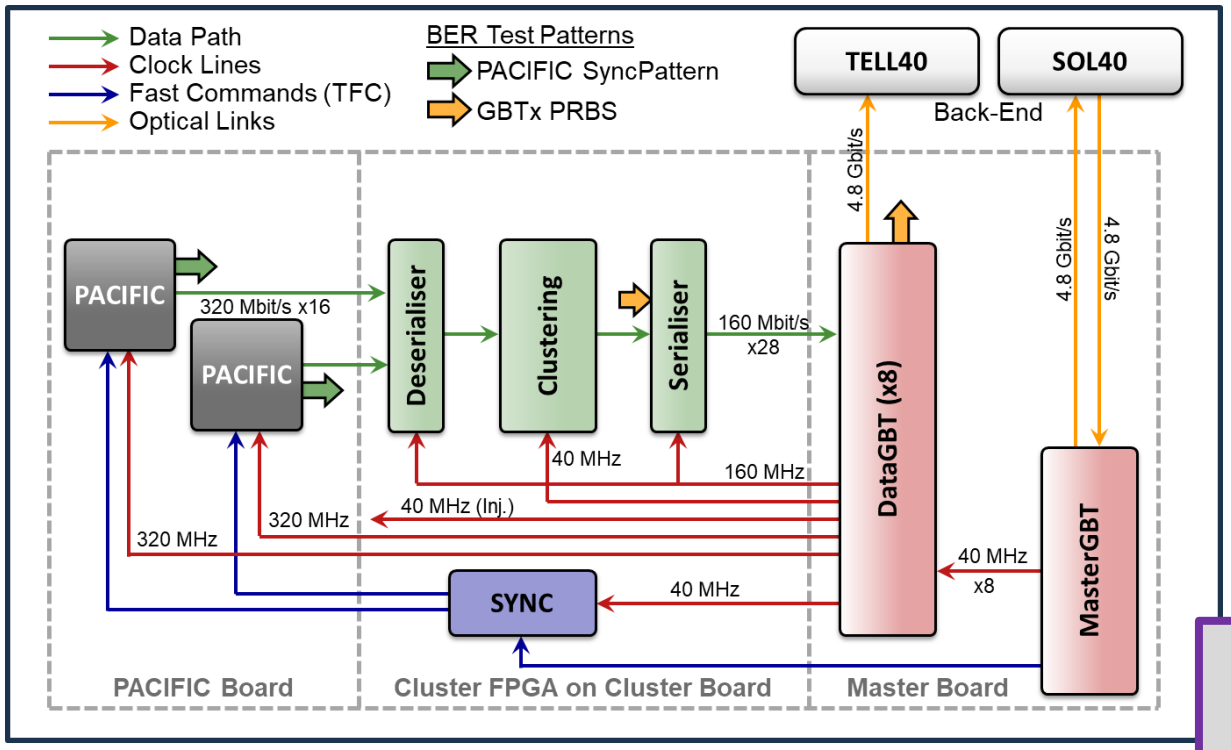
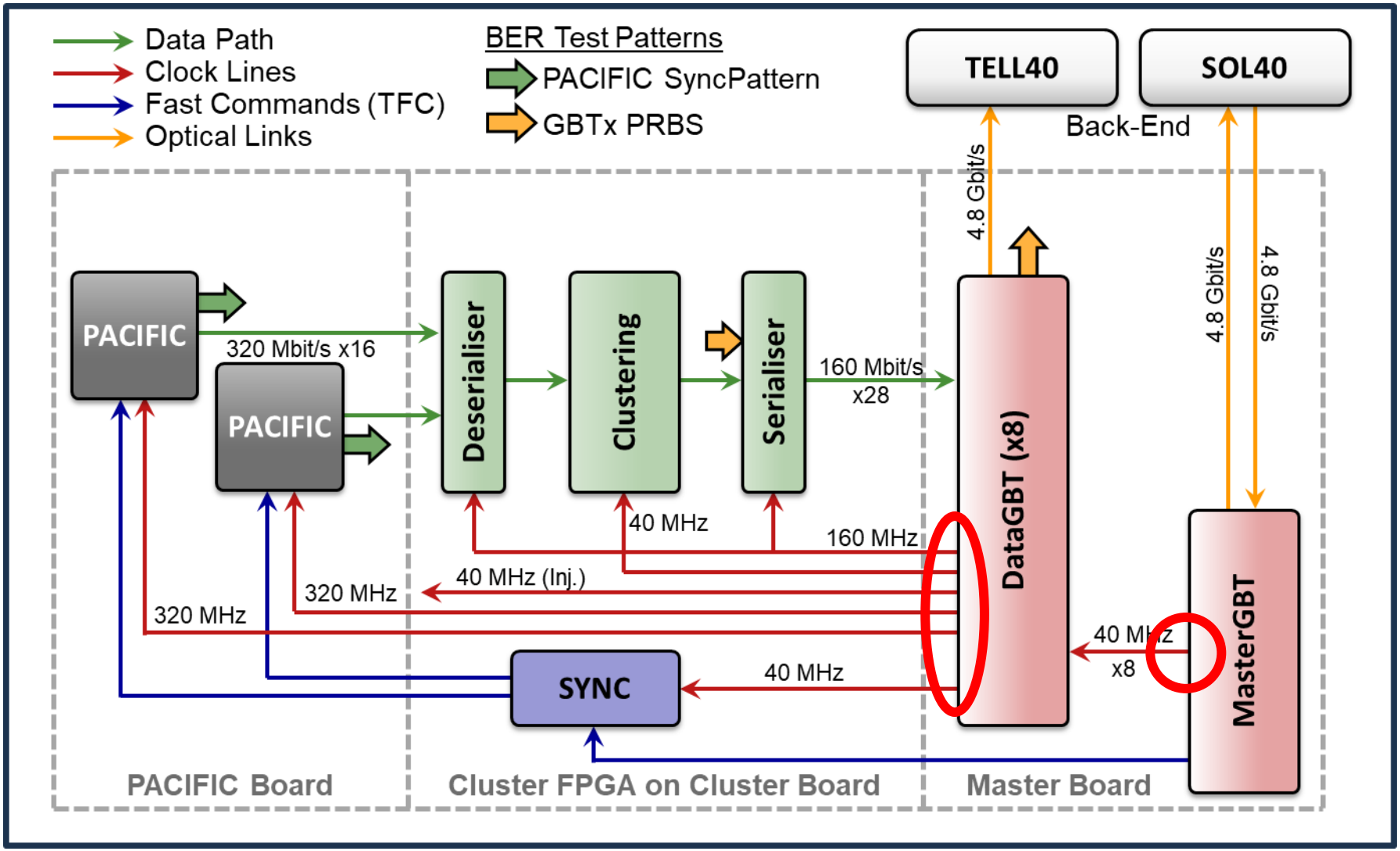


Sample from C-Frame commissioning

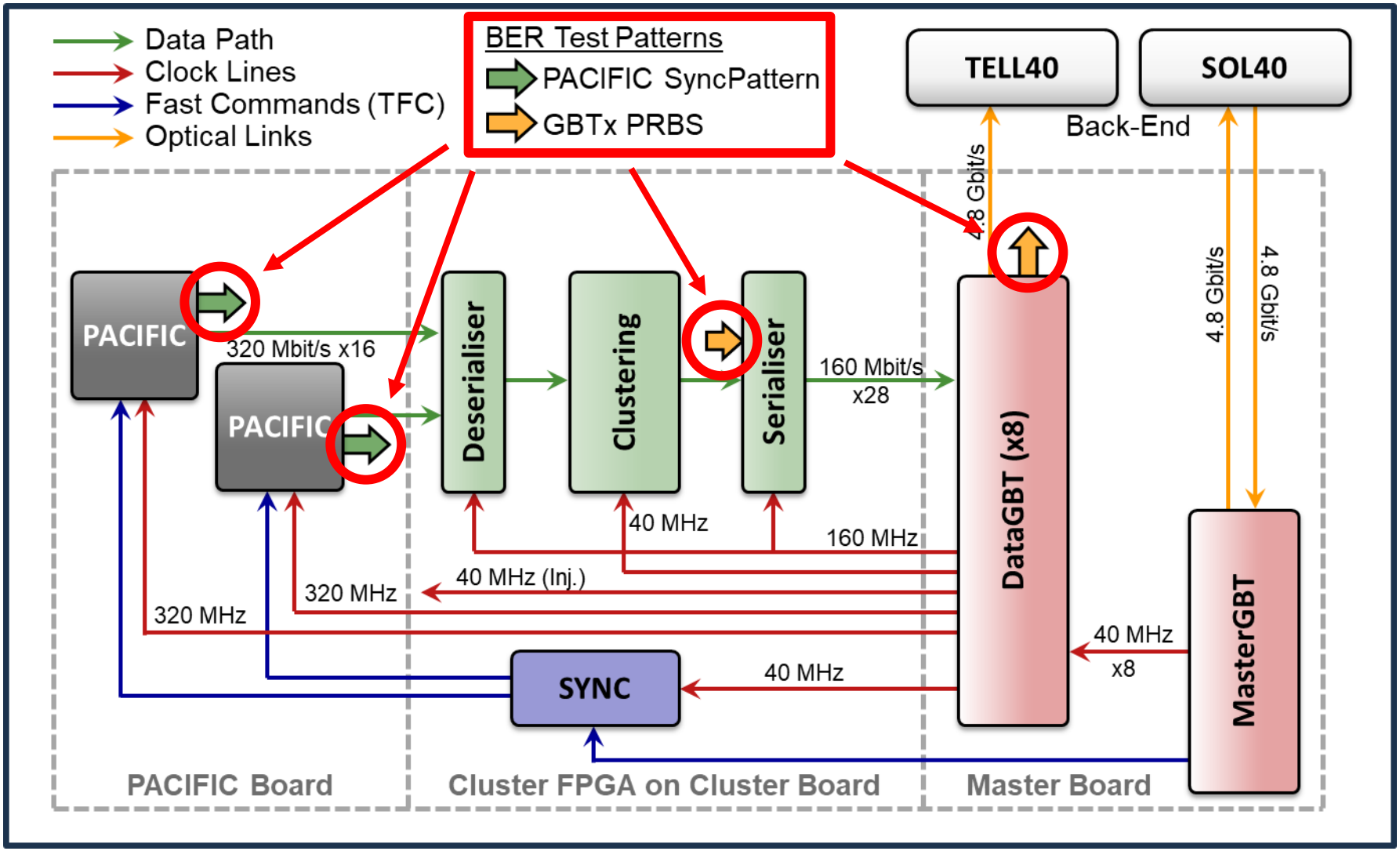
- Timing alignment toolbox:
  - A complex ecosystem: Each HalfROB has 58x Adjustable Phase Clock Paths (29k7 in SciFi);
    - IC-IC Clocks must meet Setup/Hold time requirements to ensure good data transmission;
    - Readout Clock (beam-relative) must be optimal for Physics Data Taking;



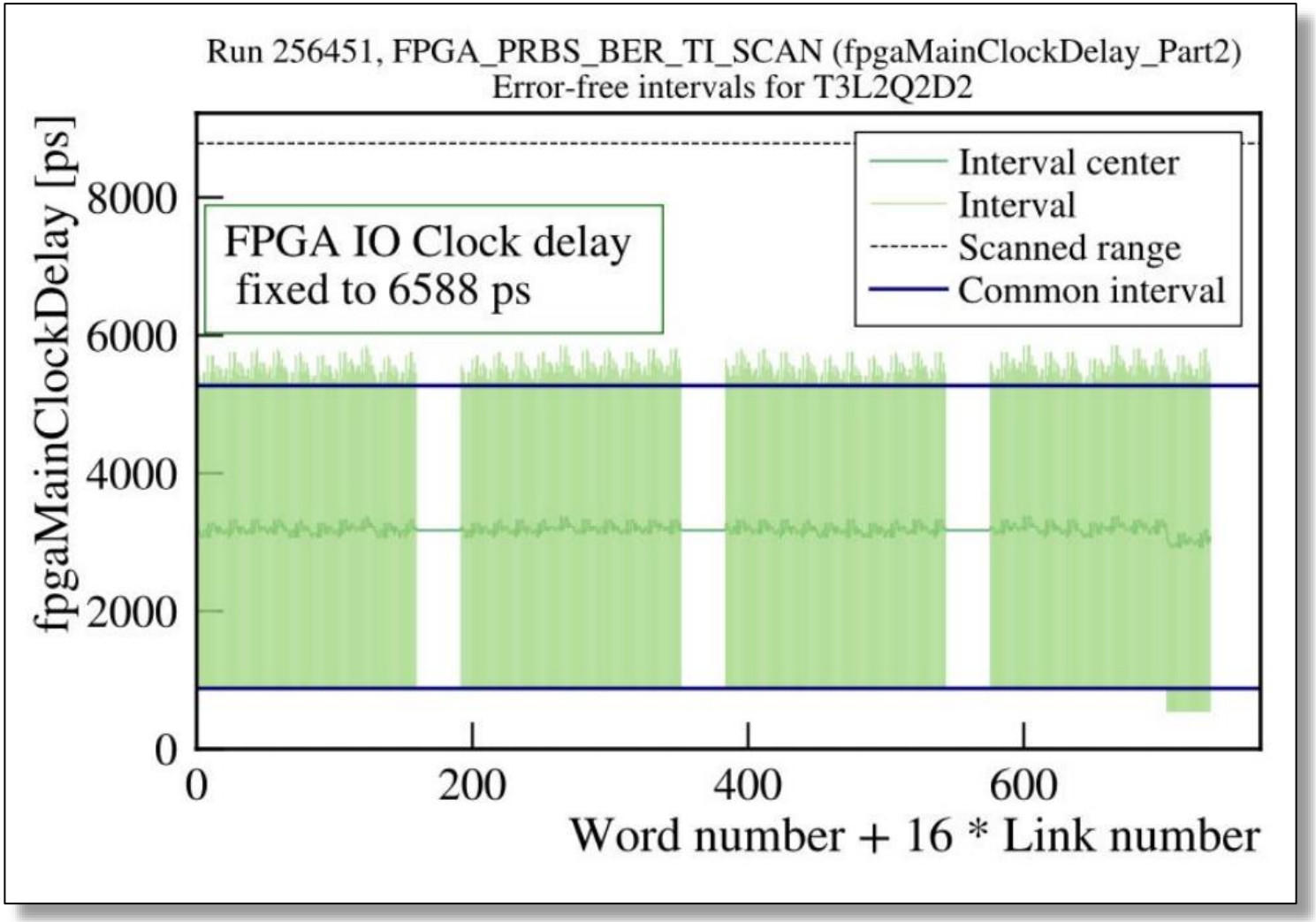
x8
(per HalfROB)
(+ 2 LIS Clk)



Multiple Phase-Adjustable Clock Lines (Based on GBTx PLL/DLL)



IC-IC Phase Tune based on Error-Free BER Phase Scan

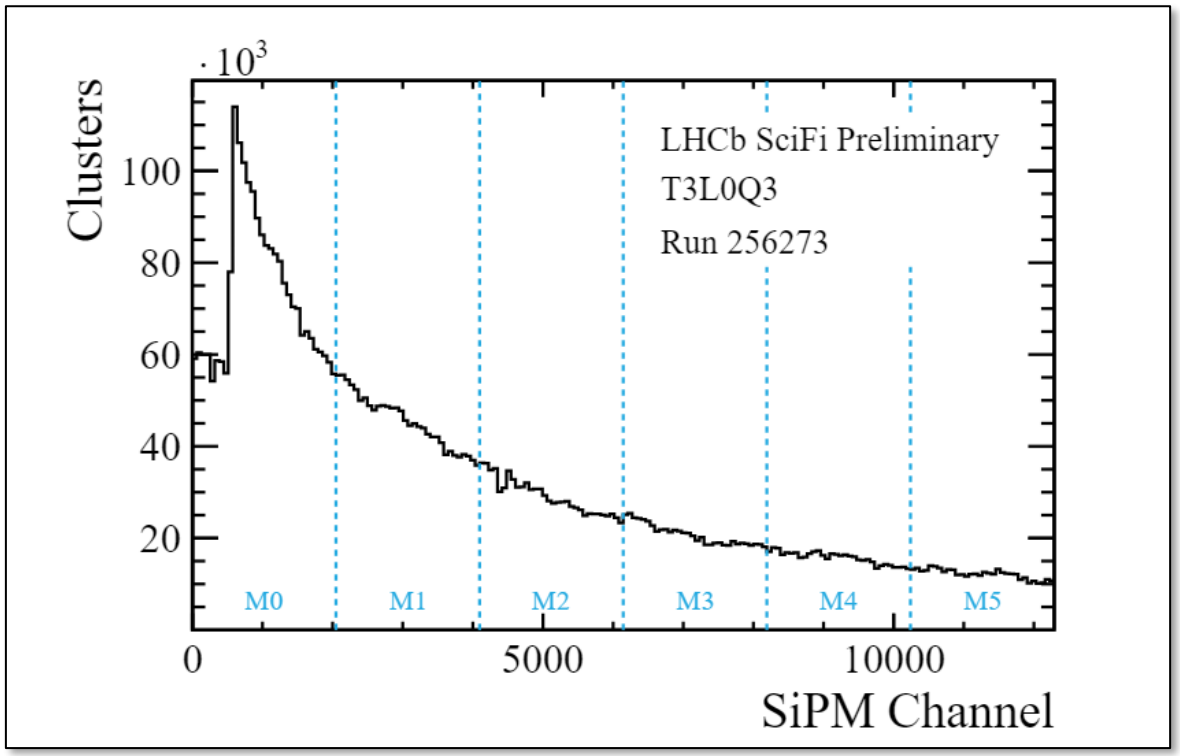


Sample from SciFi commissioning

– Results on Detector Performance –

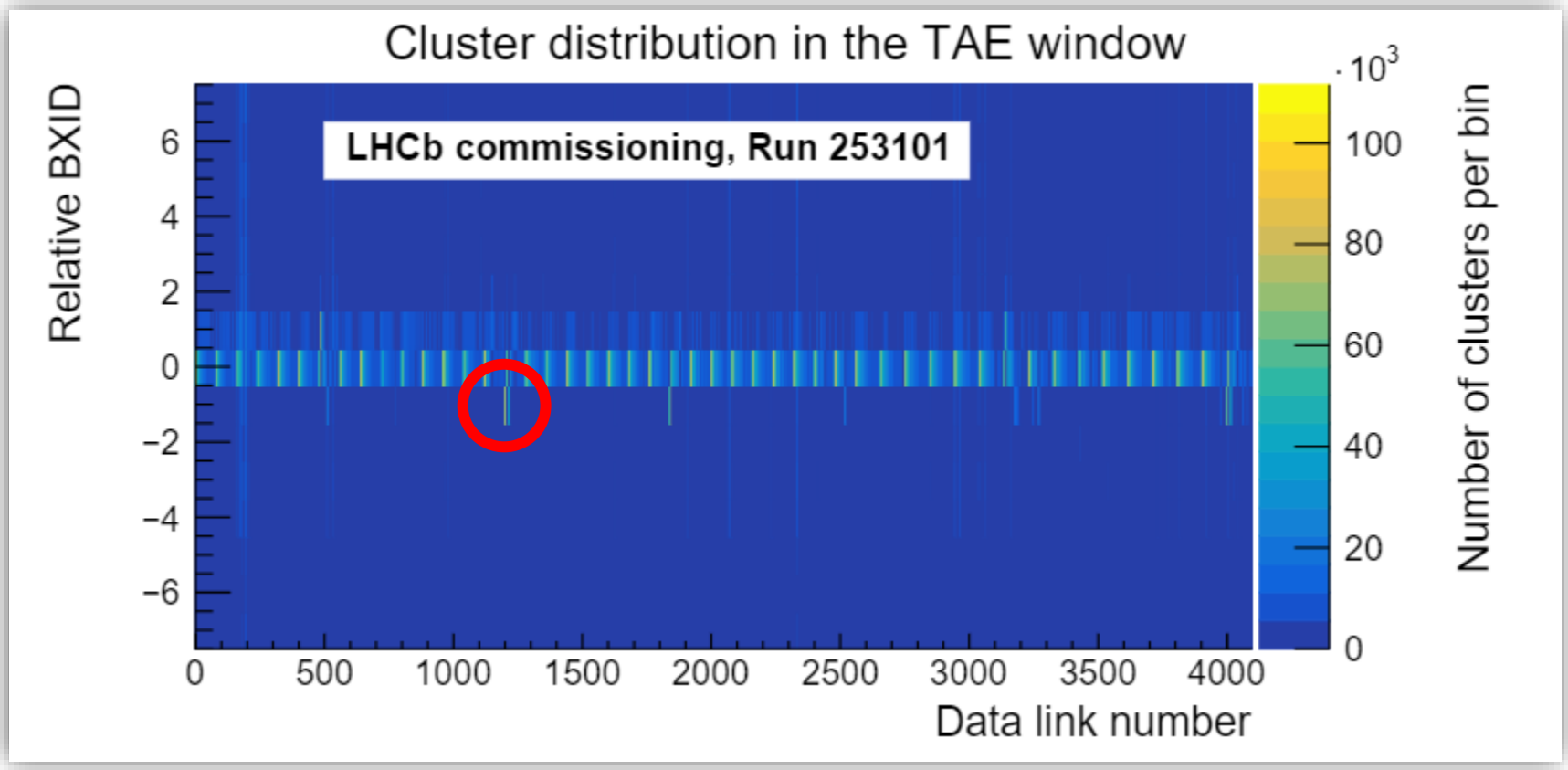
- Number of clusters as a function of the SiPM channel position:
  - Expected Occupancy Figure

LHCb-FIGURE-2023-013



- Number of clusters observed in Time Alignment Events (TAE) as a function of data link (sipm):
  - Overview plot to display detector's timing calibration;
    - Useful tool to spot out-of-timing links (one is highlighted);
  - Each column is one Data Link: The "atomic" device unit for time calibration.

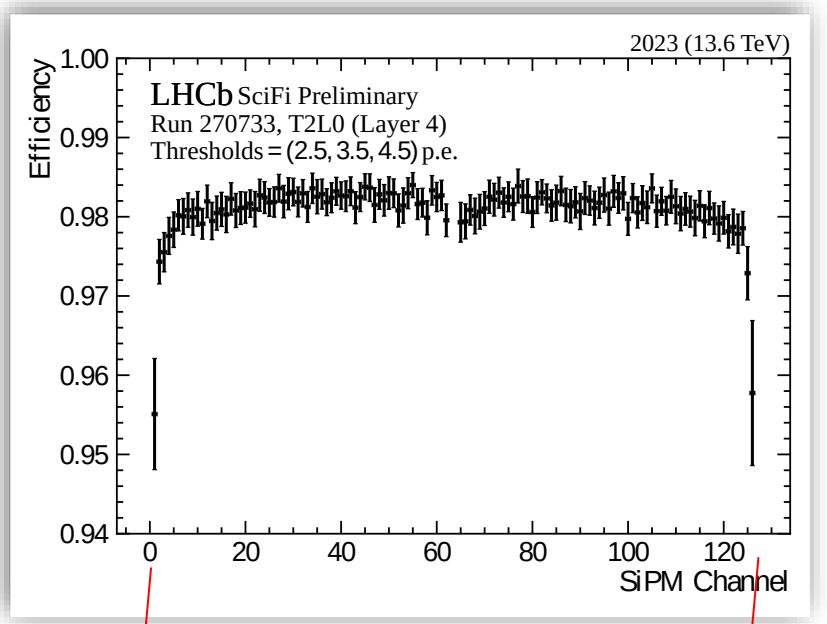
LHCb-FIGURE-2022-017

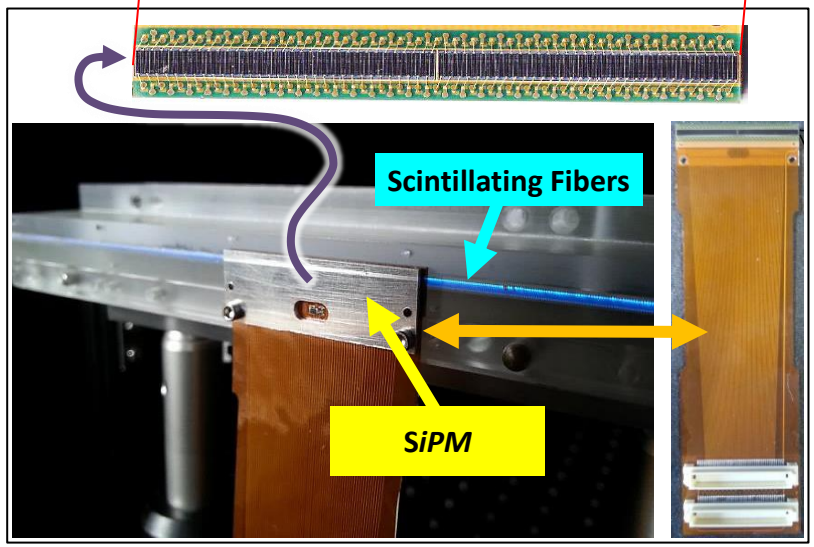


SciFi Hit Efficiency:

- Plot is from 2023-07-16:
  - Eff. > 98% on Fibre Mat central zone;
  - (Expected) Loss on edges and SiPM Die junction: Physical assembly;
- Not yet final performance:
  - Commissioning on going.

LHCb-FIGURE-2023-021





➢ **To conclude:**

✓ Front-End Electronic Devices are assembled, tested, installed and operational:

- FEE Design is functional;
- FEE FPGA Firmware (HK + CB) are released, tested and stable.

✓ SciFi Tracker is completely integrated to LHCb systems:

- Continuously operating for Global Experiment Data Taking;

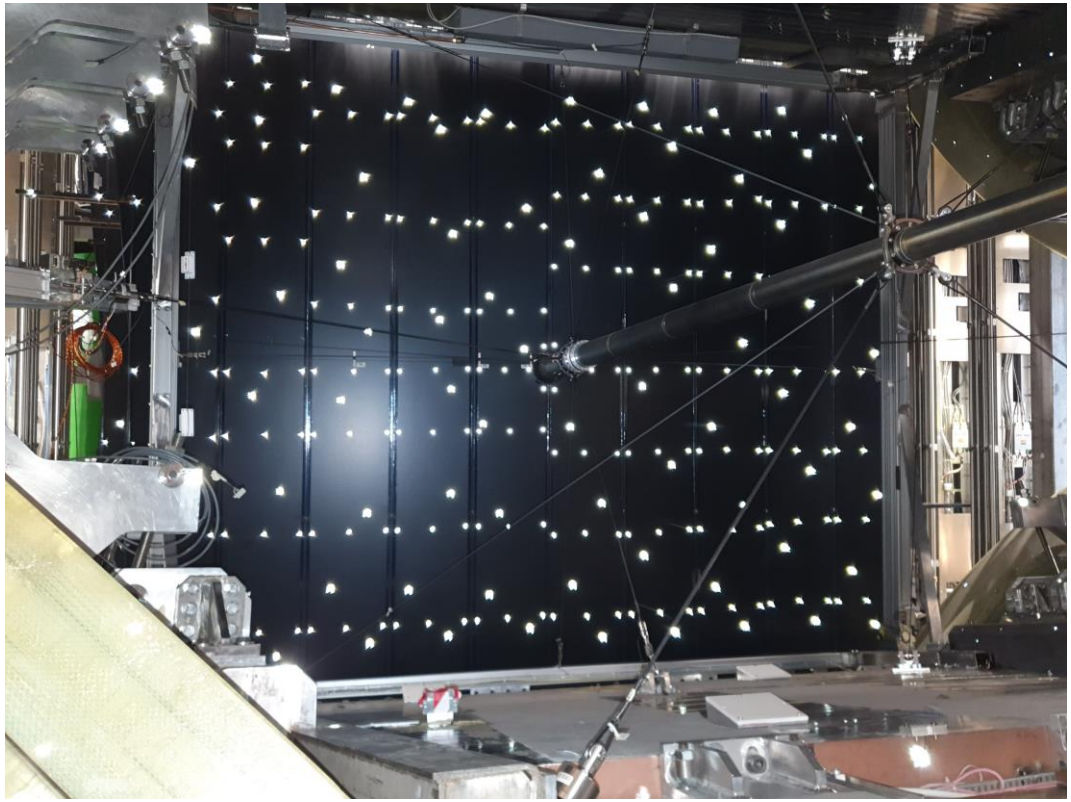
✓ Calibration methodology is implemented and works;

✓ Detector is operating well within the required performance:

- Still some room for improvement;
- Final commissioning activities are well under way.

Thank You for Your Attention !

Questions / Comments ?



SciFi fully closed around the Beam Pipe: Our Detector is there…