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Real time data processing with FPGAs at LHCb

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During the LHC Run-3 the LHCb software trigger is expected to reconstruct events at an average rate of 30 MHz. In view of future runs at even higher luminosities, LHCb established a testbed for new heterogeneous computing solutions for real-time event reconstruction within the current DAQ infrastructure. The most advanced of these sois a highly-parallelized custom tracking processor ("Artificial Retina"), implemented in state of the art FPGA devices connected by fast serial links. We describe the status of the development of a life-size demonstrator system for the reconstruction of pixel tracking detectors, that will run on real data during Run-3.

Summary (500 words)

With the slowdown of Moore's law, HEP experiments are looking at heterogeneous computing solutions as a way to face ever-increasing data flows and complexity. LHCb is on the frontier of these developments due to its specific physics needs, calling for the full software reconstruction of events in real-time at the LHC average rate of 30 MHz (40 Tb/s), already in the next physics run that started in 2022. LHCb has already adopted a GPU-based solution for HLT1 for the next run, and is further researching solution for its future Upgrade-II, with a significant increase of luminosity by a factor 5÷10. To this purpose, a coprocessor testbed has been established, to allow parasitical testing of new processing solutions in realistic DAQ conditions during the current run.

One such solution under development is a highly-parallelized custom tracking processor ("Artificial Retina"). The "Artificial Retina"architecture takes advantage of FPGAs parallel computational capabilities, by distributing the processing of each event over an array of FPGA cards, interconnected by a high-bandwidth (˜15 Tb/s) optical network. This is expected to allow operation in real-time at the full LHC collision rate, with no need for time-multiplexing or extra buffering thanks to its brief latency (<1 µs).

This level of performance has never been attained before in a complex track-reconstruction task, and achieving it opens the door to early reconstruction of track primitives transparently during detector readout. These data can be used as seeds by the High Level Trigger (HLT1/HLT2) to find tracks and perform trigger decisions with much lower computational effort than possible by starting from the raw detector data. This can free an important fraction of computing power of the conventional event-processing farm, allowing more powerful and faster reconstruction at higher luminosities than otherwise possible. Implementation of this technology could enhance the physics potential of LHCb already from the following physics run (Run-4), by expanding its trigger capability with the inclusion of long-lived tracks in the HLT1 decision.

In this talk we describe the results obtained from a realistic demonstrator for a high-throughput reconstruction of tracking detectors, operated parasitically on real LHCb data from Run 3 in a purposedly built testbed facility. This demonstrator is based on a extremely parallel, 'artificial retina' architecture, implemented in commercial, PCIe-hosted FPGA cards interconnected by fast optical links, and encompasses a sizable fraction of the LHCb VELO pixel detector. The implications of the results in view of potential applications in HEP are discussed.

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