A full-function Global Common Module (GCM) prototype for ATLAS Phase-II upgrade

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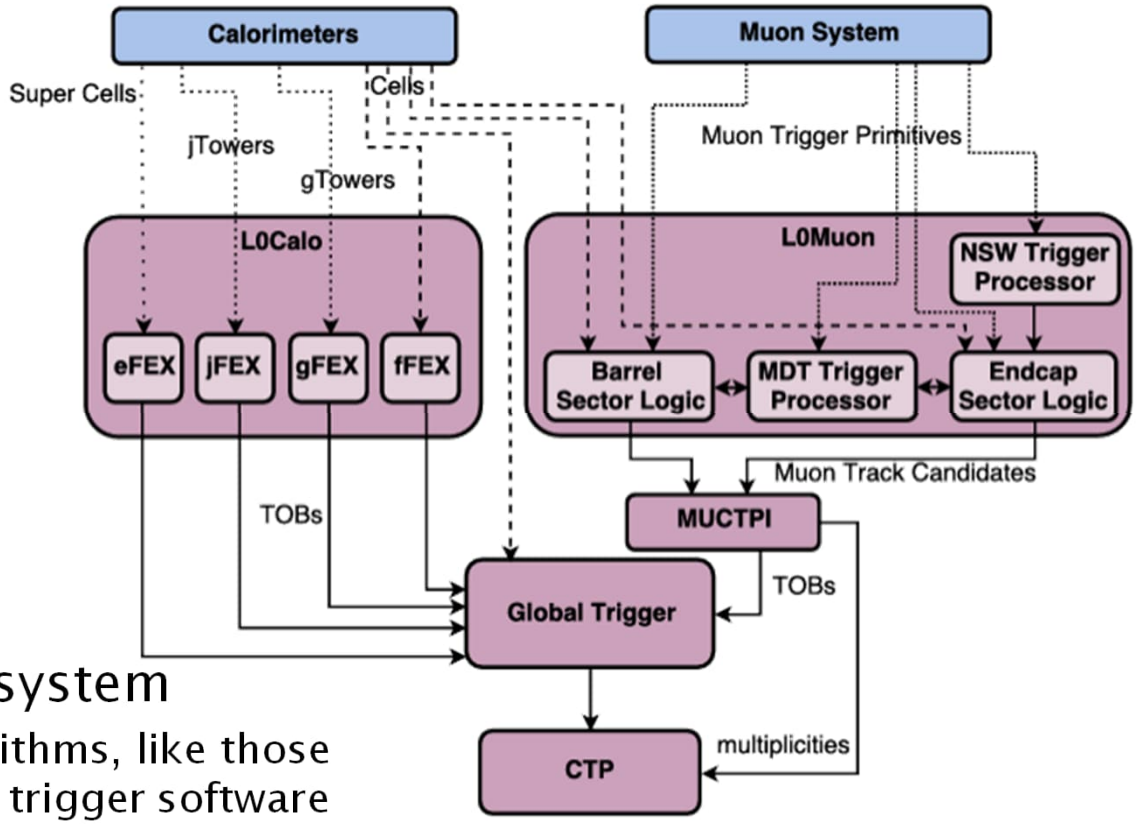
On behalf of the ATLAS Collaboration

Outline

- Introduction
  - ATLAS Phase-II Trigger architecture
- Global Common Module (GCM) full-function prototype
  - Technology choices
  - Challenges and design methodology
  - Power simulation
  - Signal simulation
  - Thermal simulation
- Summary

Introduction

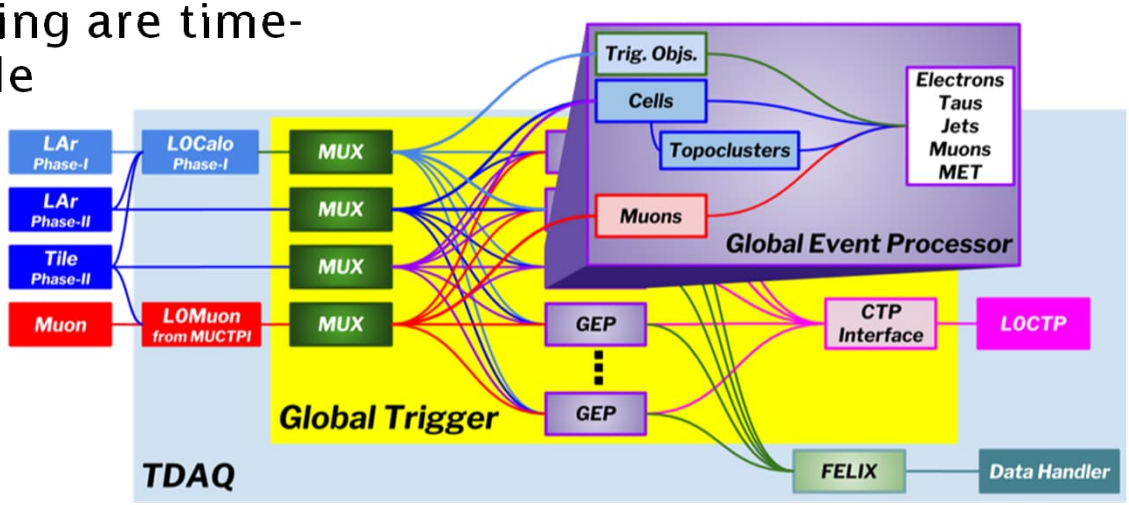
- Phase-II Upgrade parameters
  - HL-LHC luminosity
    - 5~7.5 × 10^{34} $cm^{-2}s^{-1}$
    - Pileup μ ~200
  - Multi-level trigger
    - First level (L0)
      - Trigger rate 1MHz
      - Latency rate 10μs



- TDAQ Strategy
  - New Global Trigger subsystem
    - Performing complex algorithms, like those used in Phase-1 high-level trigger software
      - Full granularity calorimeter data
      - Full event on single node

Global Trigger Architecture

- Data for a single Bunch Crossing are time-multiplexed onto a single node

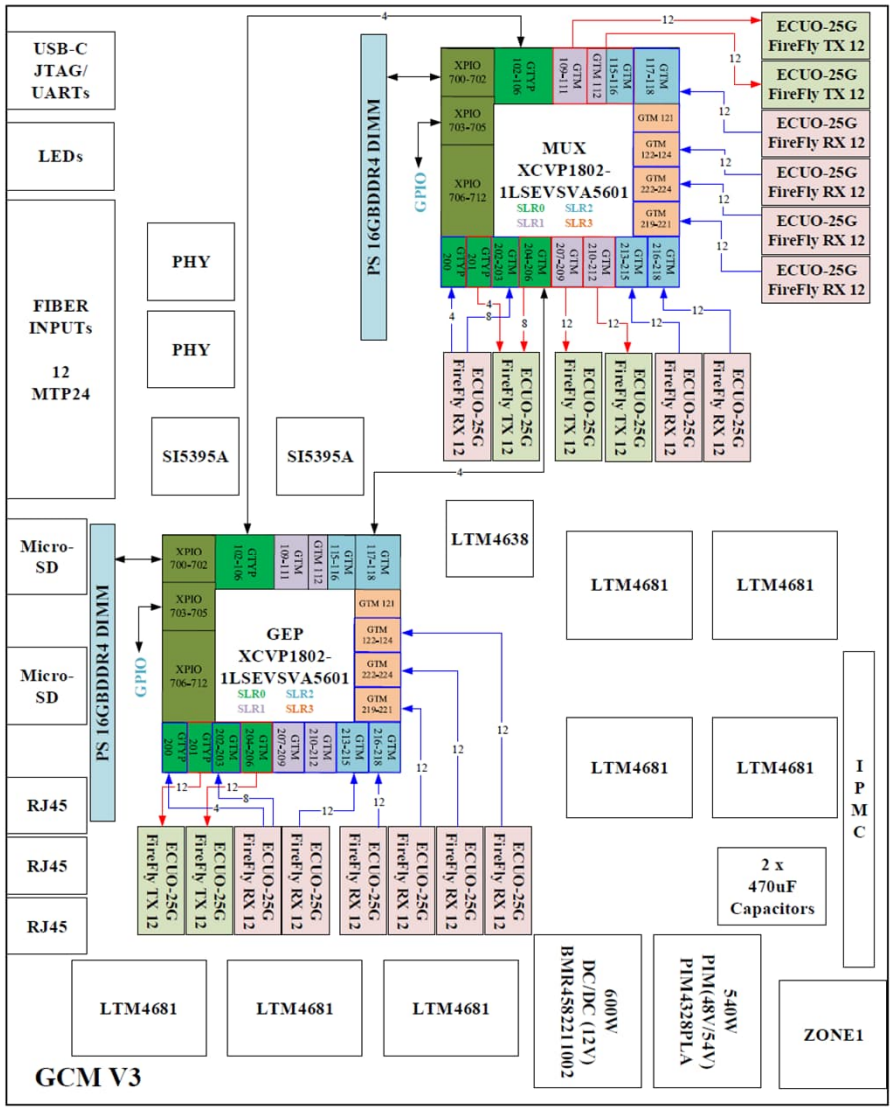


- Three functional layers
  - Multiplexing Processor (MUX)
    - ~56 nodes
  - Global Event Processor (GEP)
    - ~49 nodes
  - Global Central Trigger Processor Interface (gCTPi)
    - 1 node

- One hardware platform for all three functional layers
  - Global Common Module (GCM)
    - Simplify firmware/software development
      - Sharing the common infrastructure
    - Simplify the long-term maintenance
      - Reducing the number of spare modules needed

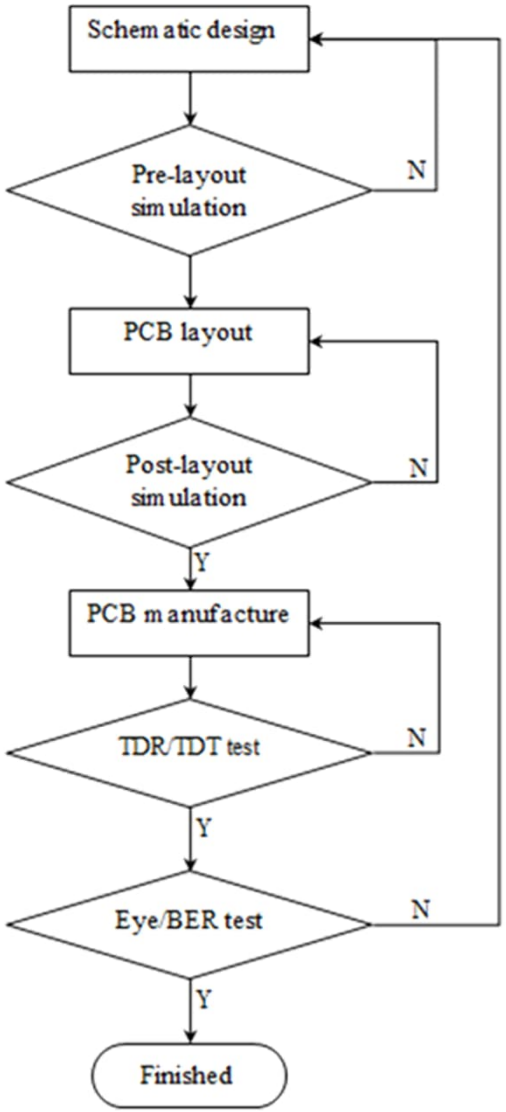
GCM Technology Choices

- Platform
  - ATCA front board
    - 1 MUX node + 1 GEP node per board
- FPGA
  - Versal Premium adaptive SoC VP1802 for MUX node
  - Versal Premium adaptive SoC VP1802 for GEP/gCTPi node
  - VSVA5601 package
    - 75x75, 0.92mm pitch
    - Minimizing crosstalk
- Optics
  - 20 Firefly 28G parallel optical engines
    - 12 ch/optical engine
- PCB
  - 26 layers
  - Via-in-pad
  - Backdrill



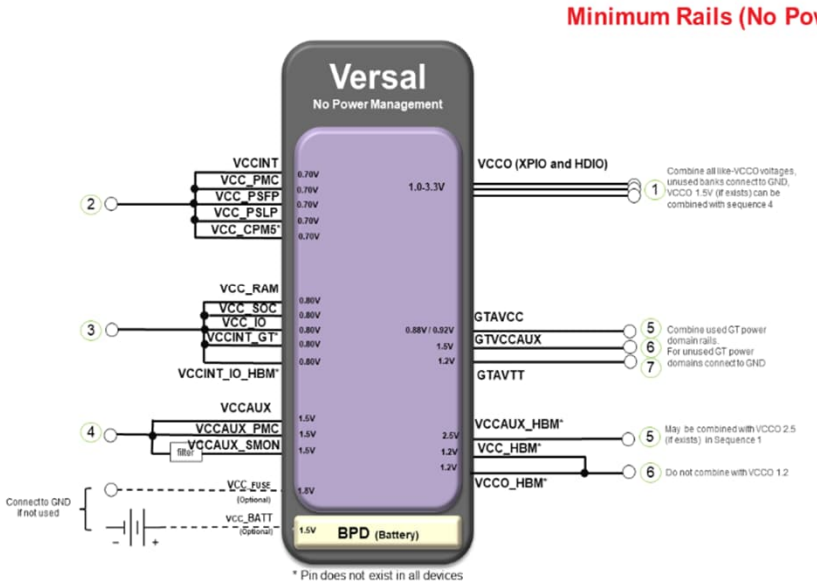
Challenges and Design Methodology

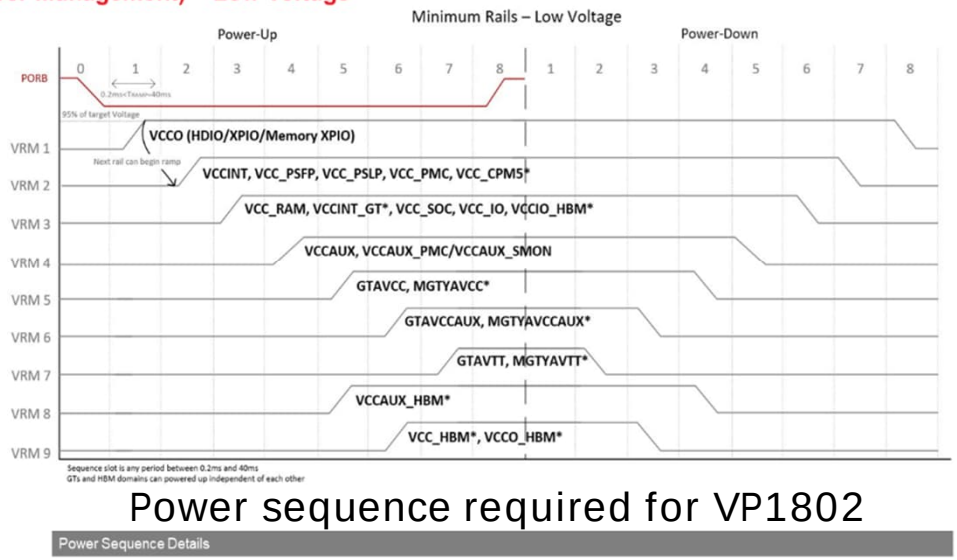
- High-speed, high-power and high-density complex PCB design
  - Signal integrity
    - 25+Gbps
  - Power integrity
    - 400 W
  - Thermal integrity
    - VP1802 ~80 ° C
    - Firefly ~50 ° C
- Simulation integrated into design flow
- Design for test
  - Integrated PCB test coupon
  - Special test launch points



Power Design Challenges

- Each adaptive SoC VP1802
  - Minimum of 9 power rails
- GCM with two adaptive SoC VP1802
  - ~20 power rails in total





Power sequence required for VP1802

Power Sequence Details

Adaptive SoC VP1802 Power Estimation

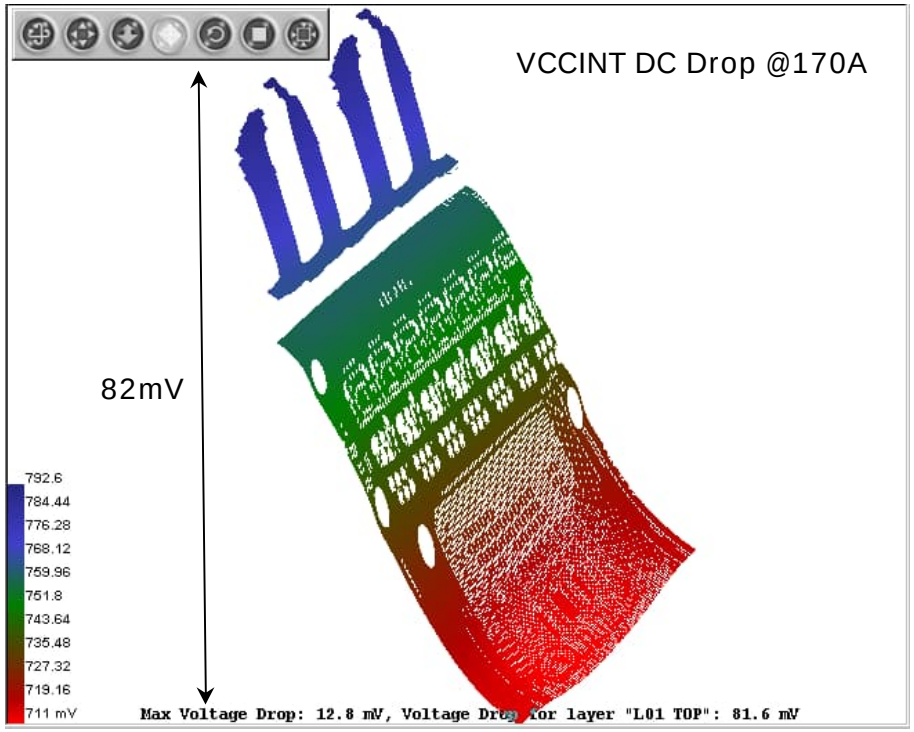
- Current Best Estimate (CBE) for a GEP node is 107W
  - Maximum Expected Value (MEV) is 131W
  - Maximum Possible Value (MPV) is 165W
- GCM hardware is targeted to MPV power value
  - Maximum GEP node VCCINT (0.7V) current ~170A
- 26-layer PCB
  - 4 power planes with a total thickness of 6 oz.
  - 12 GND planes with a total thickness of 7 oz.

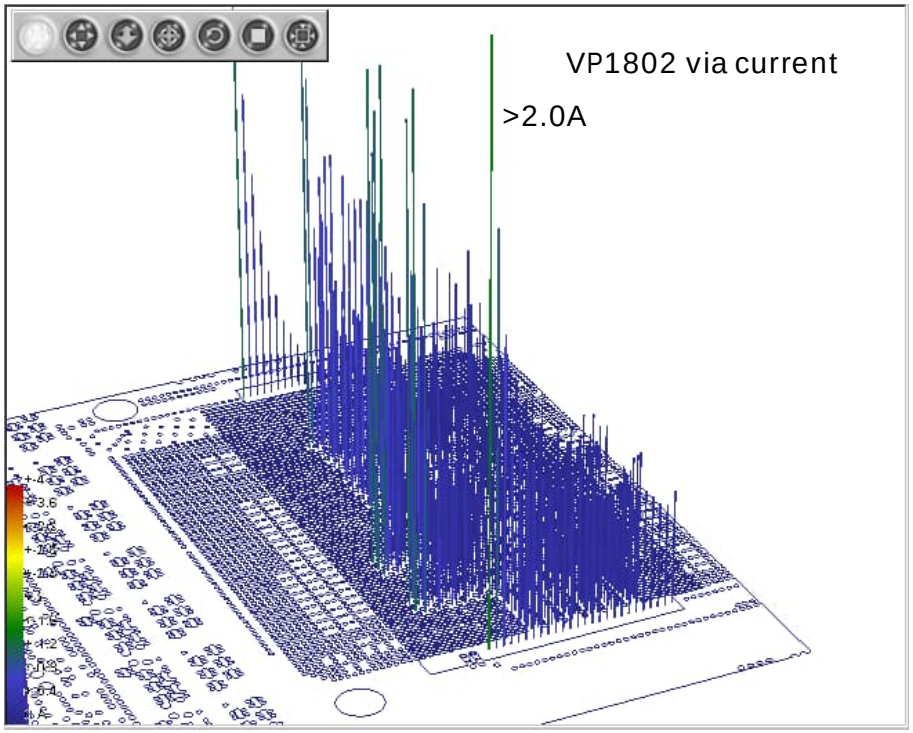
A. 26-Layers Stackup Proposal for ATLAS GCM Prototype V3

Description							Vias					
Layer	Copper (oz)	Layer	50Ω SE	93Ω DIFF (Stripline)	93Ω DIFF (Stripline)	100Ω DIFF	Trough	Backdrill L26-L23	Backdrill L26-L21	Backdrill L26-L19	Backdrill L26-L17	Backdrill L26-L12
L1	0.5	TOP	8	4.6-3.9-4.6		4-4-4						
L2	0.5	GND										
L3	1	PWR1										
L4	0.5	GND										
L5	0.5	SIG1	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L6	0.5	GND										
L7	0.5	SIG2	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L8	0.5	GND										
L9	0.5	SIG3	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L10	0.5	GND										
L11	0.5	SIG4	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L12	1	GND										
L13	2	PWR2										
L14	2	PWR3										
L15	1	GND										
L16	0.5	SIG5	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L17	0.5	GND										
L18	0.5	SIG6	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L19	0.5	GND										
L20	0.5	SIG7	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L21	0.5	GND										
L22	0.5	SIG8	4	3.6-4.9-3.6	3.4-4.1-3.4	3.5-4.5-3.5						
L23	0.5	GND										
L24	1	PWR4										
L25	0.5	GND										
L26	0.5	BOT	8	4.6-3.9-4.6		4-4-4						
Thickness (mil)												
L1-L26		<102 mil										

GCM Power Simulation

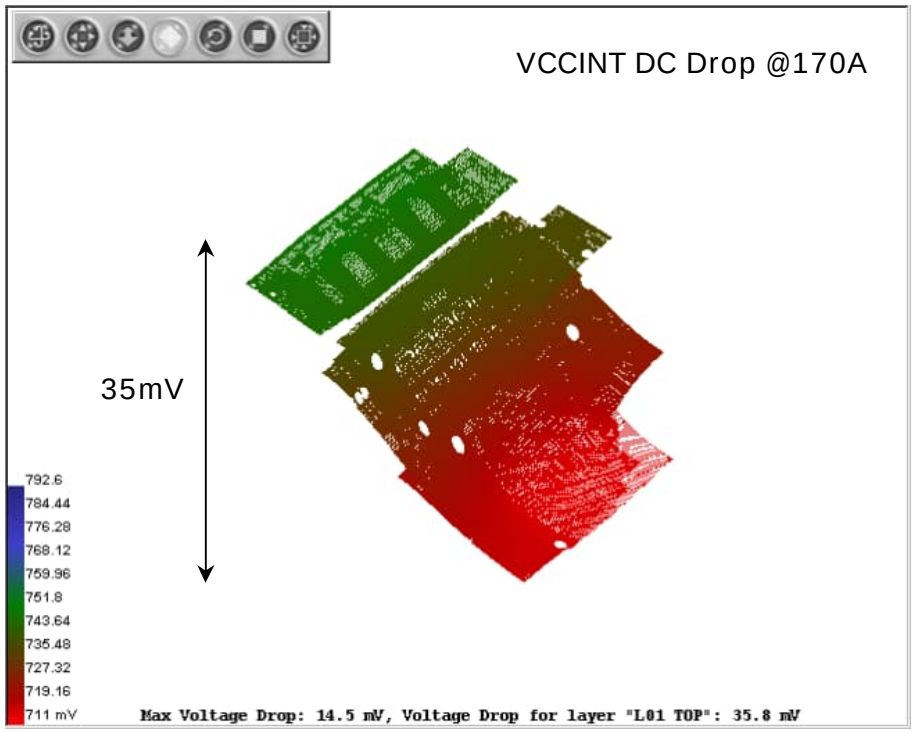
- Initial VCCINT layout
  - Excessive DC voltage drop
    - PCB copper itself consumes16 W – too hot
  - Via current spikes
    - Long term stability issue

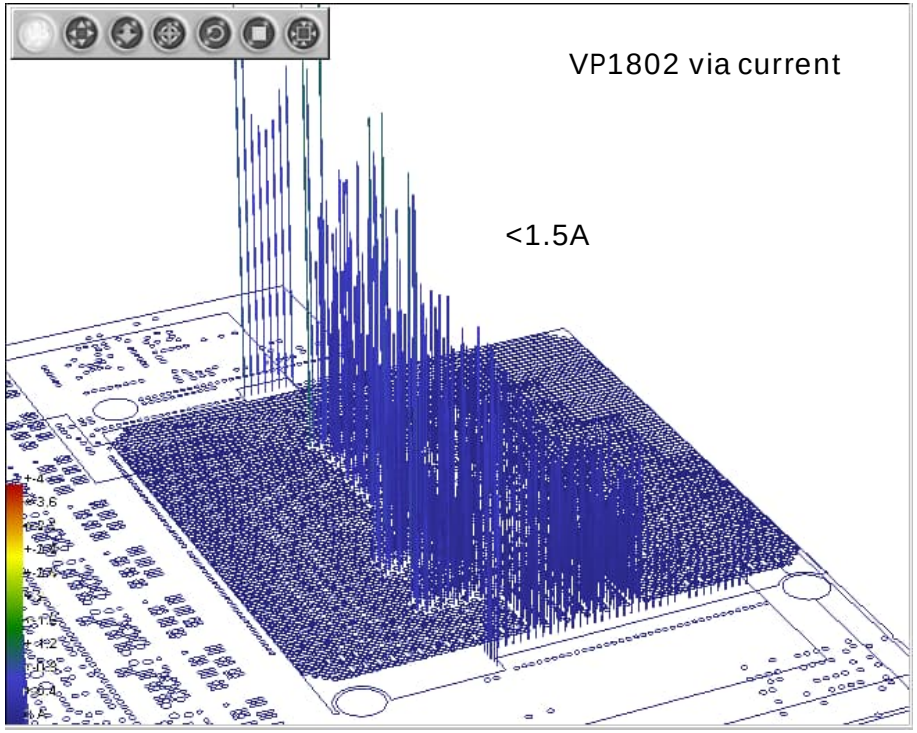




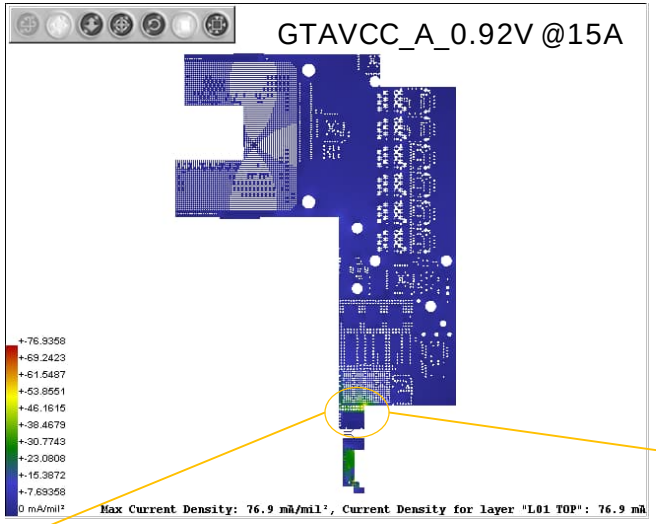
GCM Power Simulation

- Post-optimization
  - Strategic copper fills in signal layers
    - DC voltage drop on VCCINT much reduced
    - PCB copper power consumption is halved
    - Via current spikes are suppressed

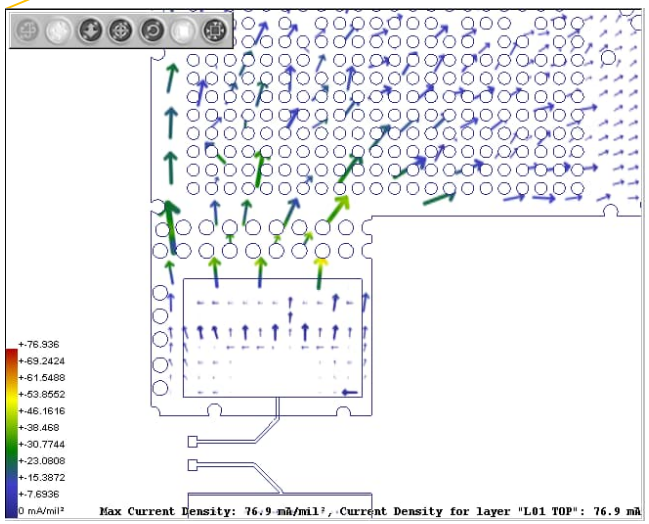




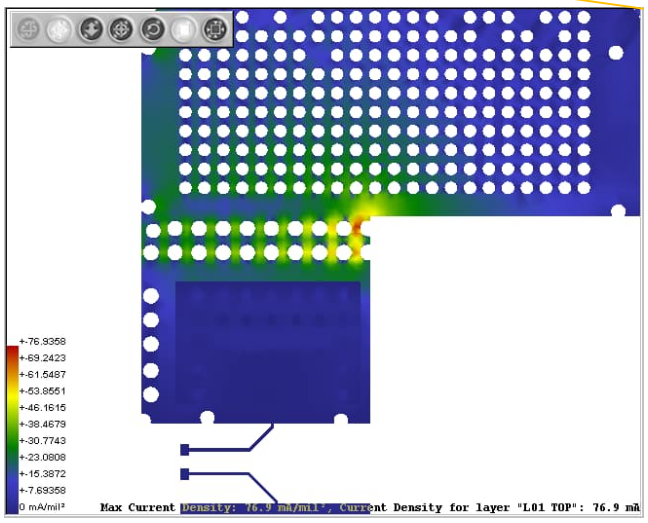
GCM Power Simulation



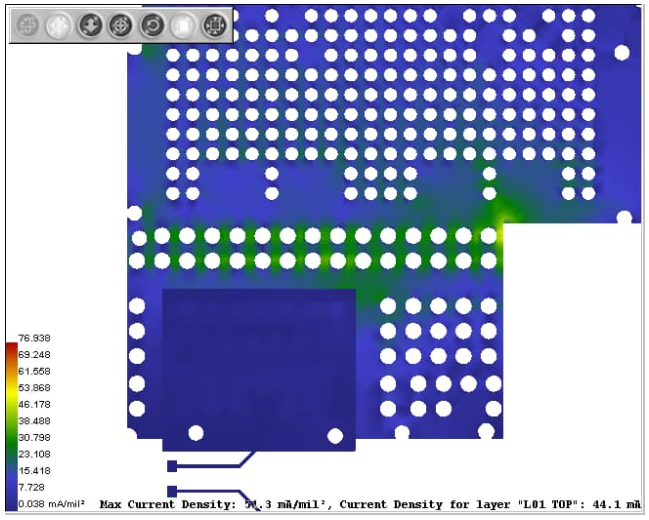
- Smaller current power rail could also have problem
  - GTAVCC_A hotspot
    - Highly perforated power plane
    - Long term stability issue



Current vectors before optimization



Current density before optimization

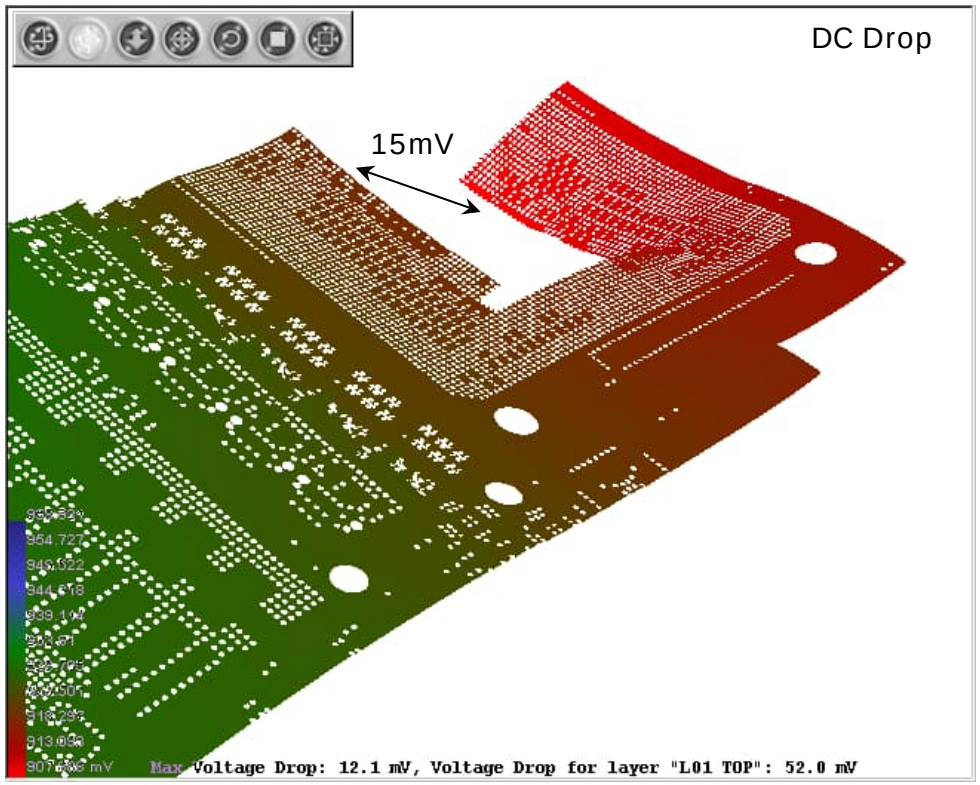


Current density after optimization
Hotspot removed!

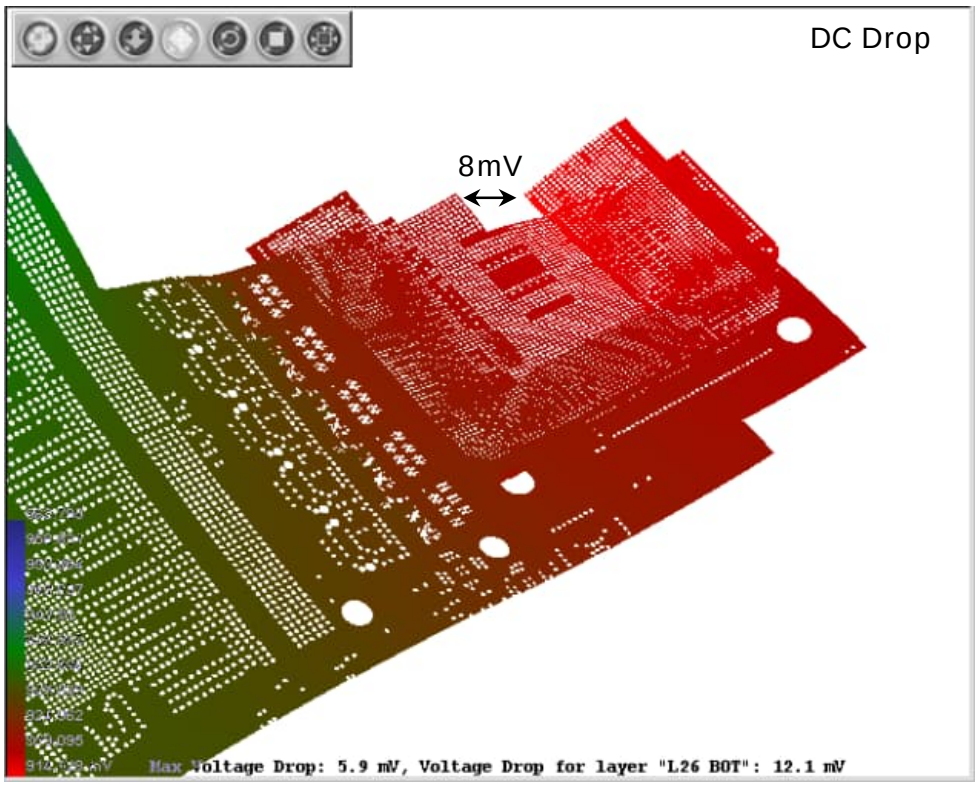
GCM Power Simulation

- Smaller current power rail could also have problem
  - GTAVCC_B excessive voltage offset between banks

GTAVCC_B_0.92V @15A



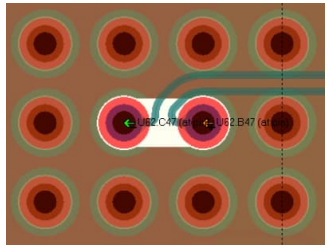
Before optimization

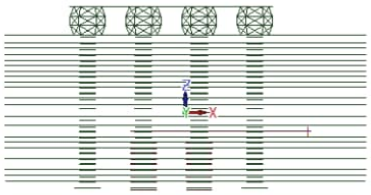


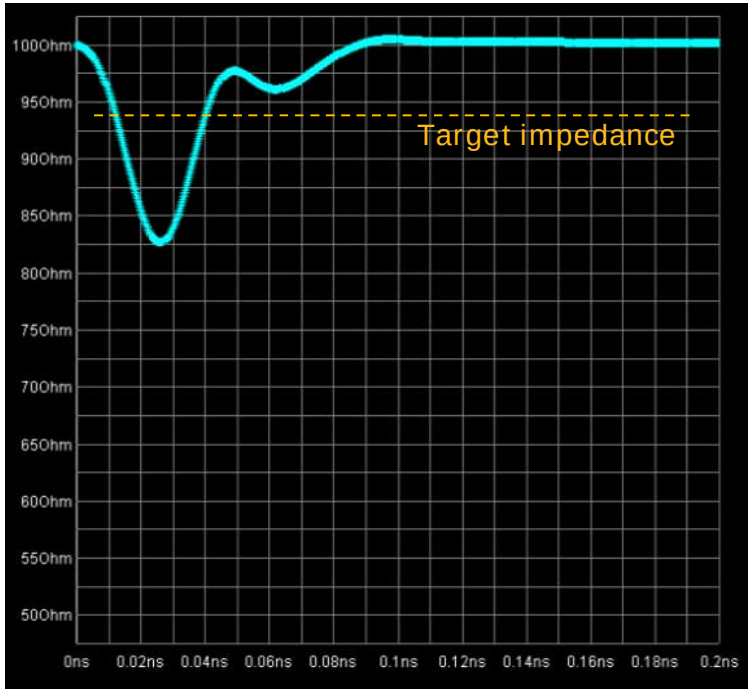
After optimization

GCM Signal Simulation

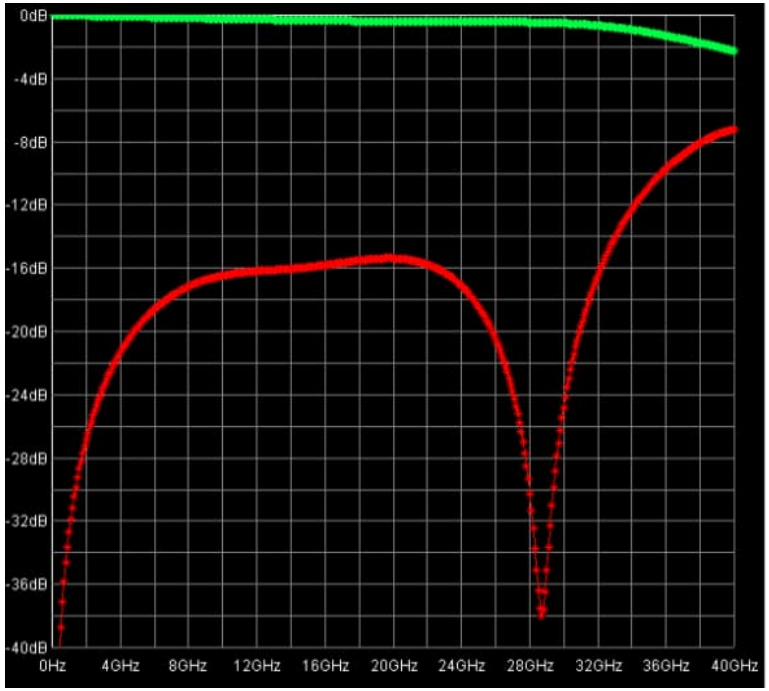
- FPGA BGA breakout optimization
  - Via-in-pad + 22mil dog-bone antipad + backdrill
  - Target differential impedance for Xilinx MGT is 93ohm







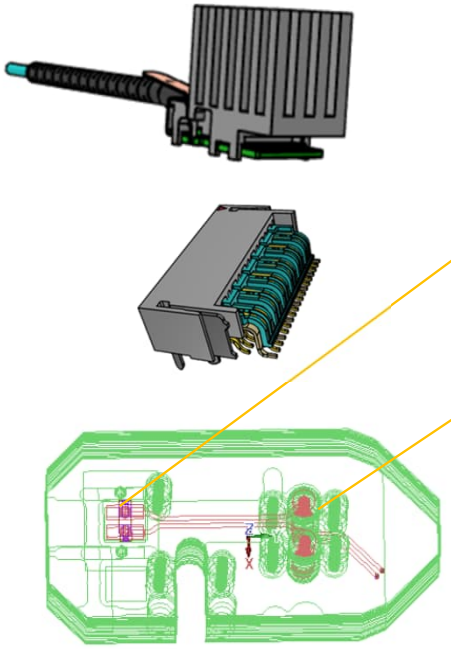
Differential via TDR response to Tr=20ps
Minimum impedance ~83 ohm

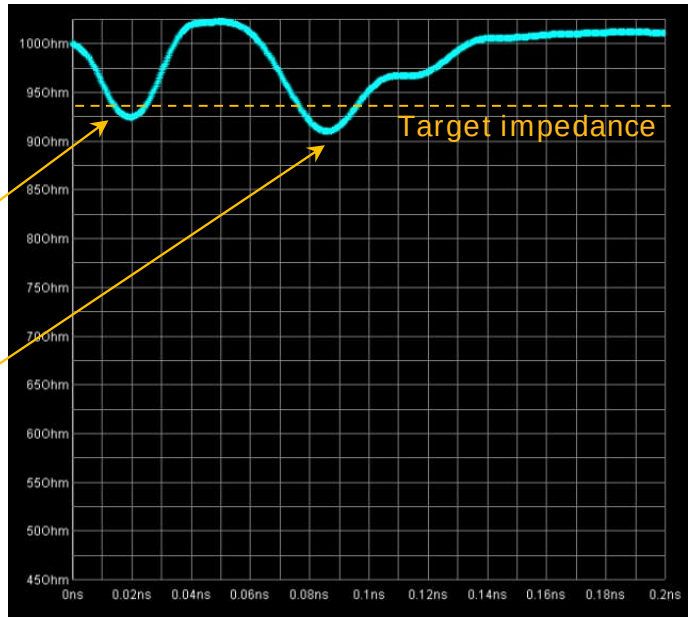


Differential via S-parameters insertion loss SDD21 and return loss SDD11

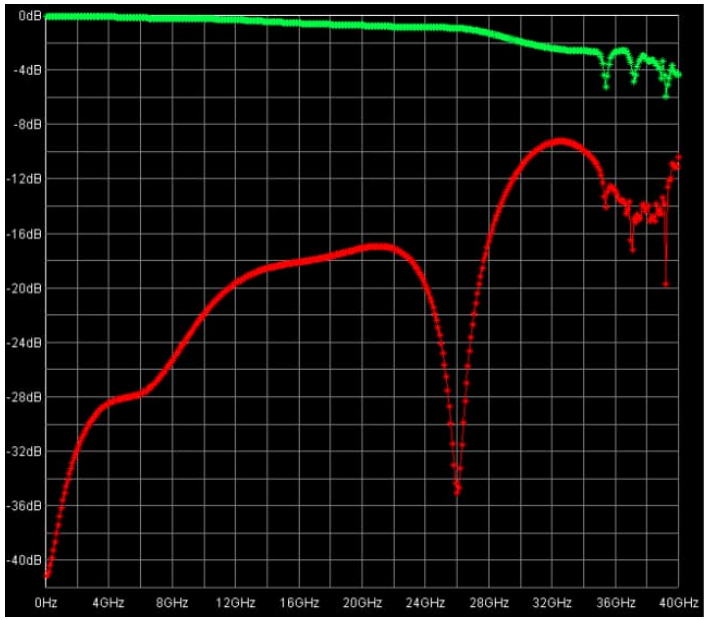
GCM Signal Simulation

- Firefly breakout optimization
  - SMA pads
    - Cutout in the underlying plane to reduce capacitance
  - Differential via configuration
    - 40mil separation, 32mil anti-pad, backdrill + 4 GND vias





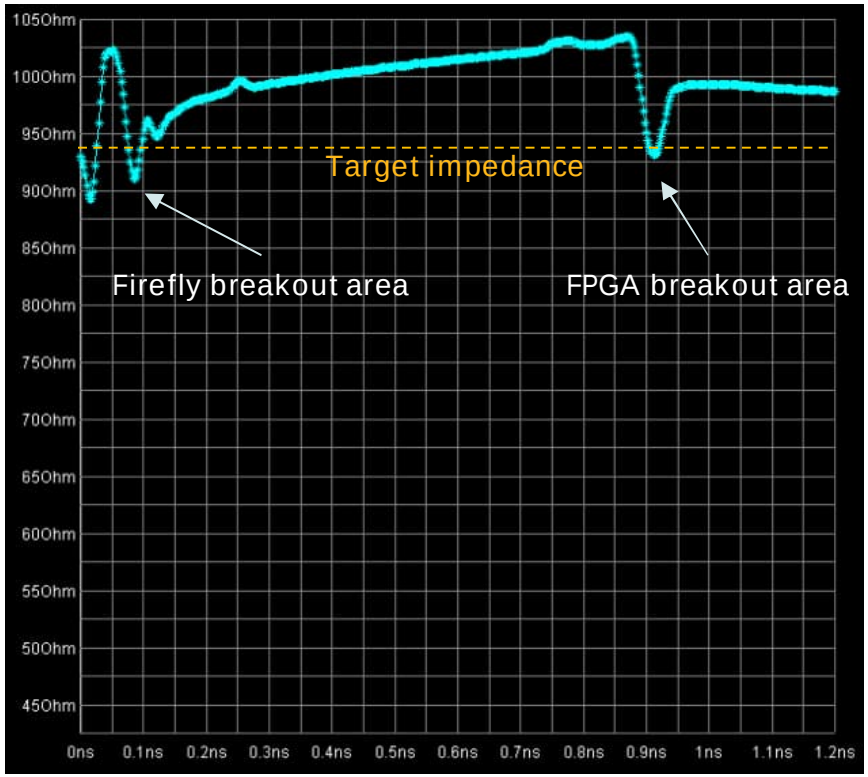
Differential TDR response to Tr=20ps
Firefly diff SMA pads min impedance ~92.5 ohm
Diff via min impedance ~91 ohm



Differential via S-parameters insertion loss SDD21 and return loss SDD11

GCM Signal Simulation

- Typical 25G channel performance
  - Impedance control very well over 3-D structures
  - Insertion loss curve smooth roll-off

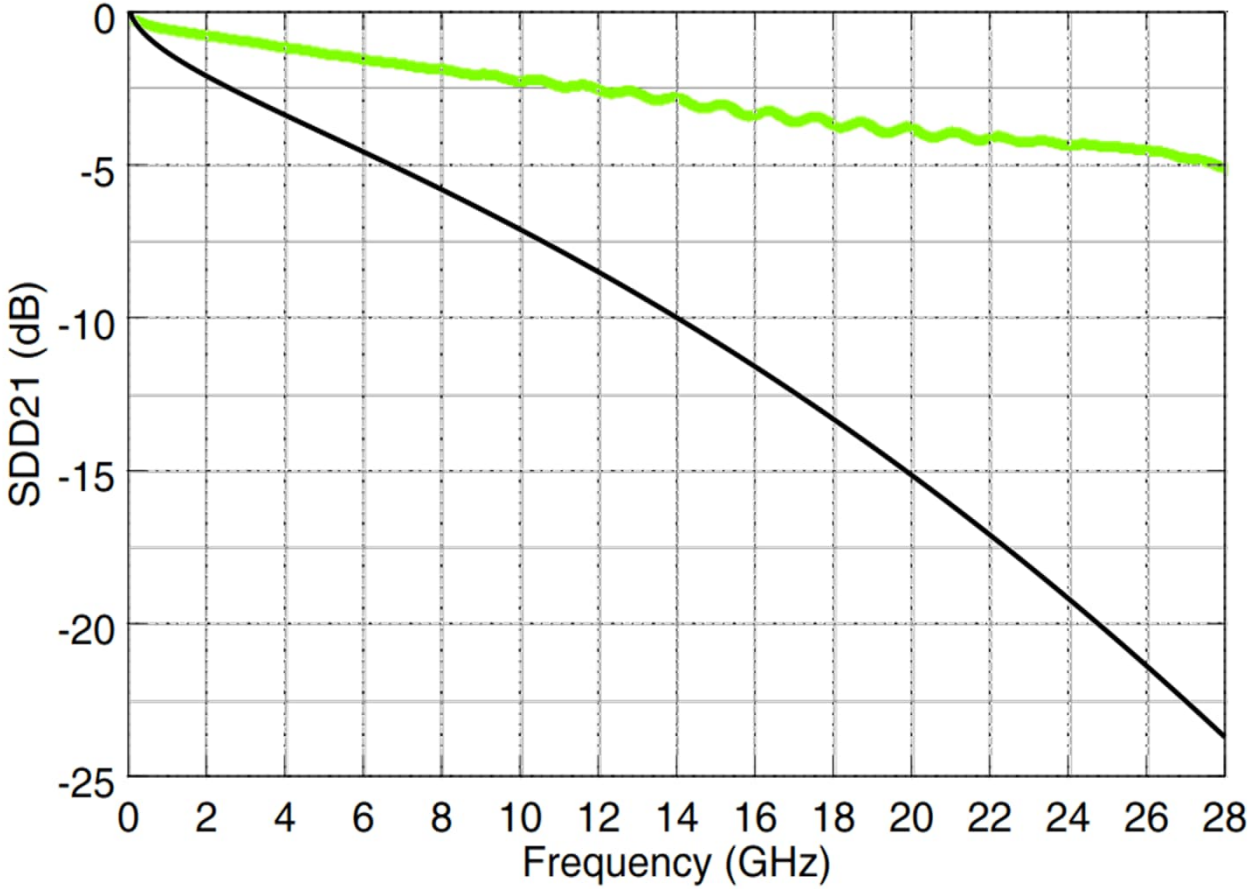


Differential TDR response to Tr=20ps

Differential via S-parameters SDD21 and SDD11

GCM Signal Simulation

- Typical 25G channel performance
  - Comparing to Industry standard CEI-28G-VSR
    - Used by both AMD (Xilinx) and Firefly



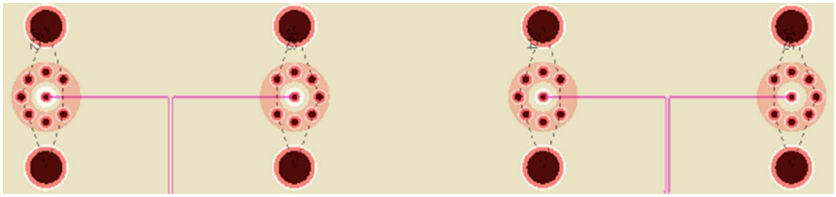
Green: GCM typical 25G channel SDD21

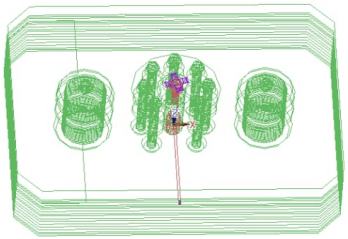
Black: OIF-CEI-04.0 recommended minimum SDD21 of the VSR channel (for fb = 28 GHz)

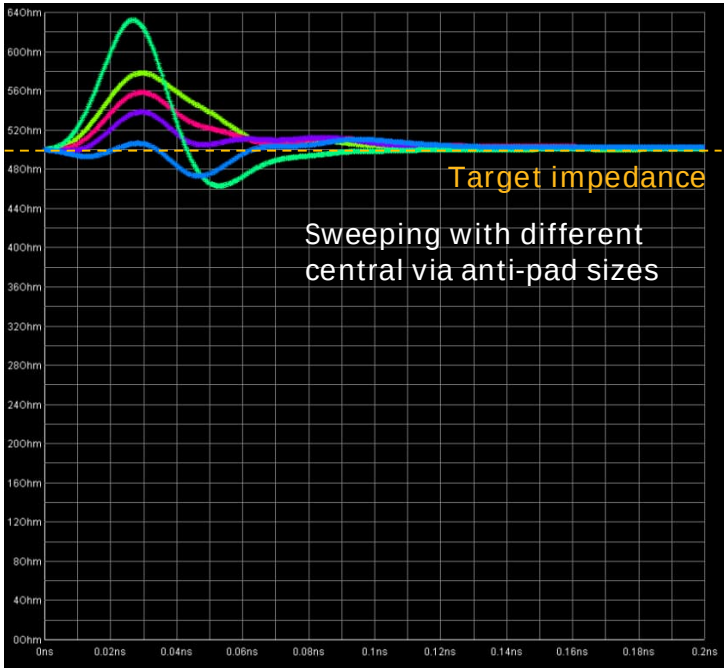
$$H(f) = 0.3144 - 8.1\sqrt{\frac{f}{f_b}} - 2.38\frac{f}{f_b} - 13.56\left(\frac{f}{f_b}\right)^2$$

GCM Signal Simulation

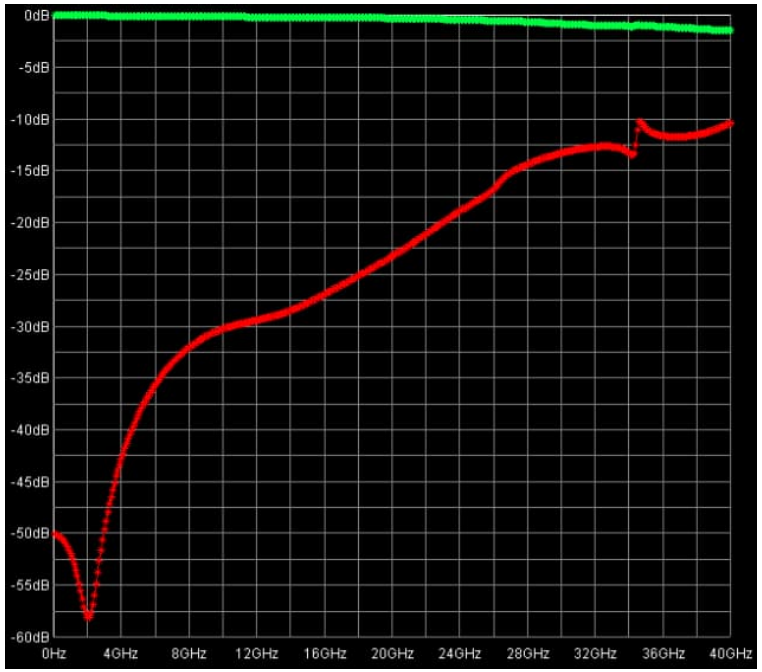
- Special connector launch design for 25G link test
  - Good performance to 40GHz







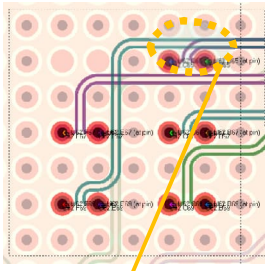
2.4mm Connector Launch TDR response to Tr=20ps
Minimum impedance ~47.5 ohm

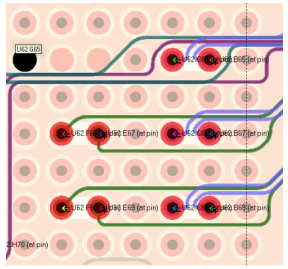


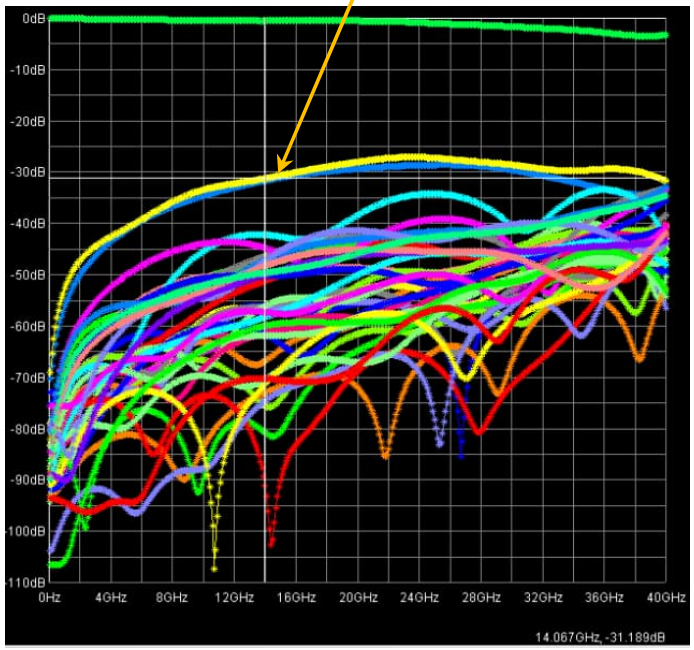
2.4mm Connector Launch S-parameters
insertion loss SD21 and return loss SD11

GCM Signal Simulation

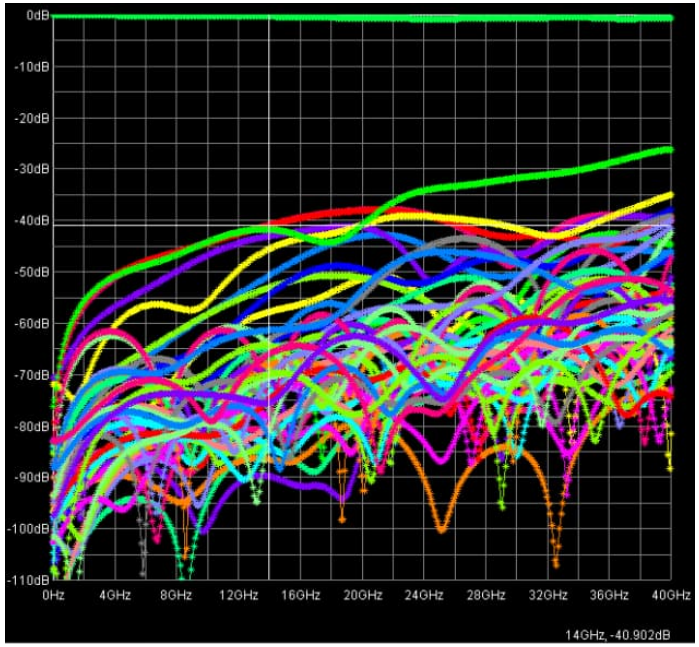
- Xilinx Crosstalk Requirement for CEI-28G-VSR
  - Rx-Rx
    - < -40dB
- GCM Rx-Rx
  - Majority
    - < -42dB
  - But one
    - ~32dB
  - Optimization
    - Swapping routing layers







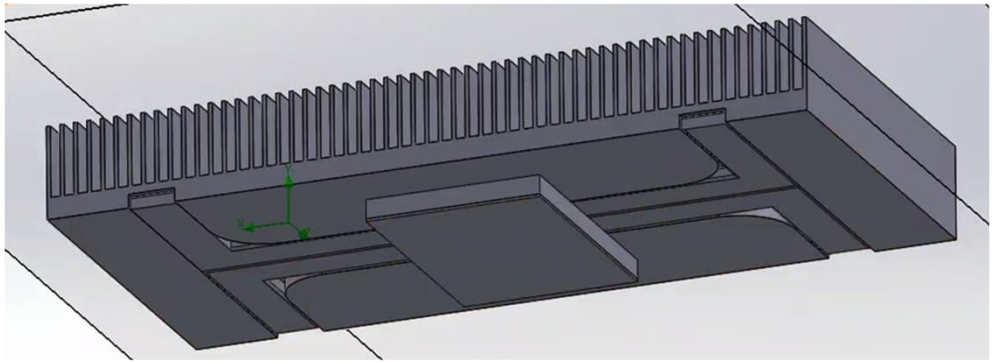
Before optimization



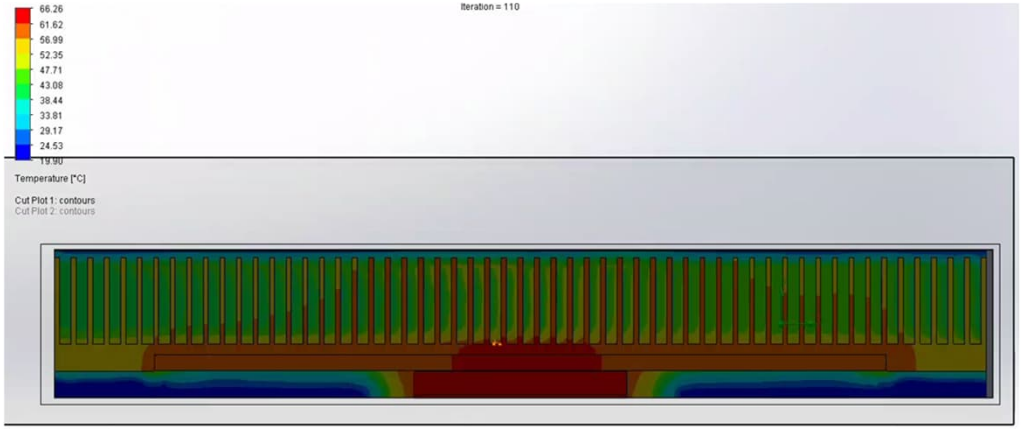
After optimization

GCM Thermal Simulation

- Heatsink design and simulation are outsourced
  - VP1802, 130mm x 70 mm x 17 mm on-board space reserved



Provided by Radian

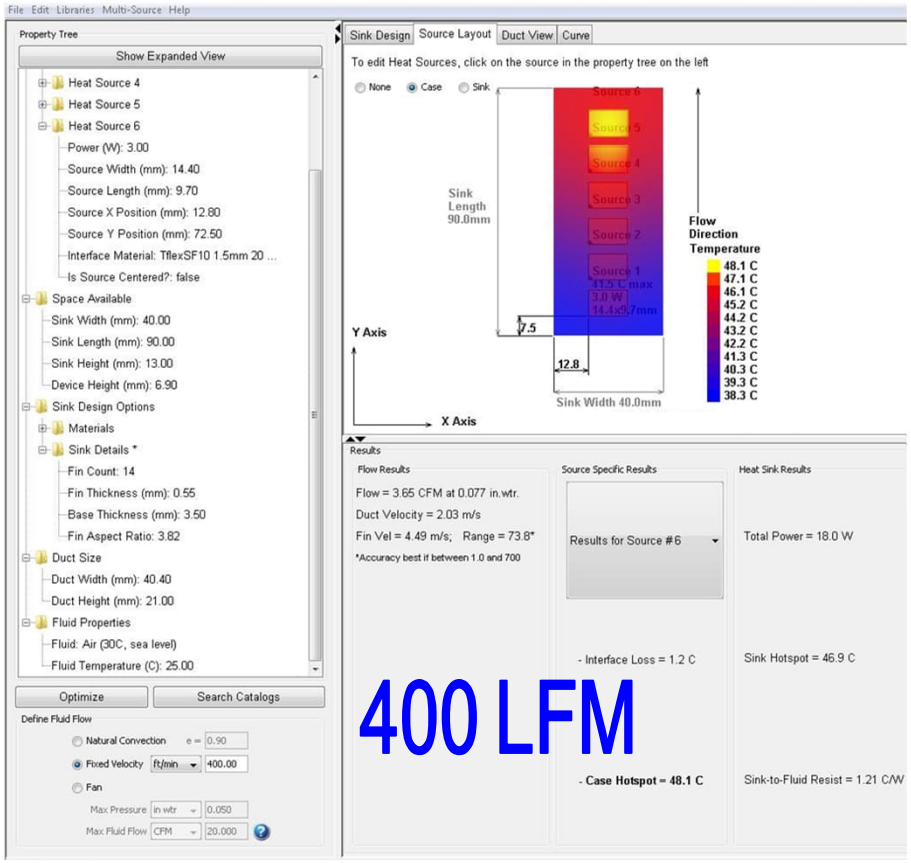


- Heatsink design with embedded heat pipe
- Air flow: 500LFM
- Case temperature: 66 ℃ @ 160W
- Thermal resistance: ~0.29 ℃/W

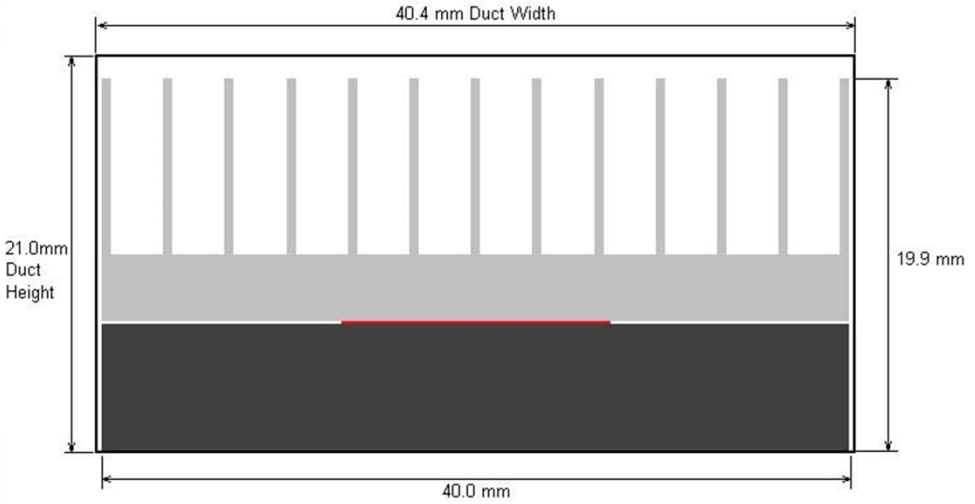
nVent SCHROFF ATCA shelf
maximum air flow > 700LFM

GCM Thermal Simulation

- Heatsink design and simulation are outsourced
  - Firefly optical engine, vertical block



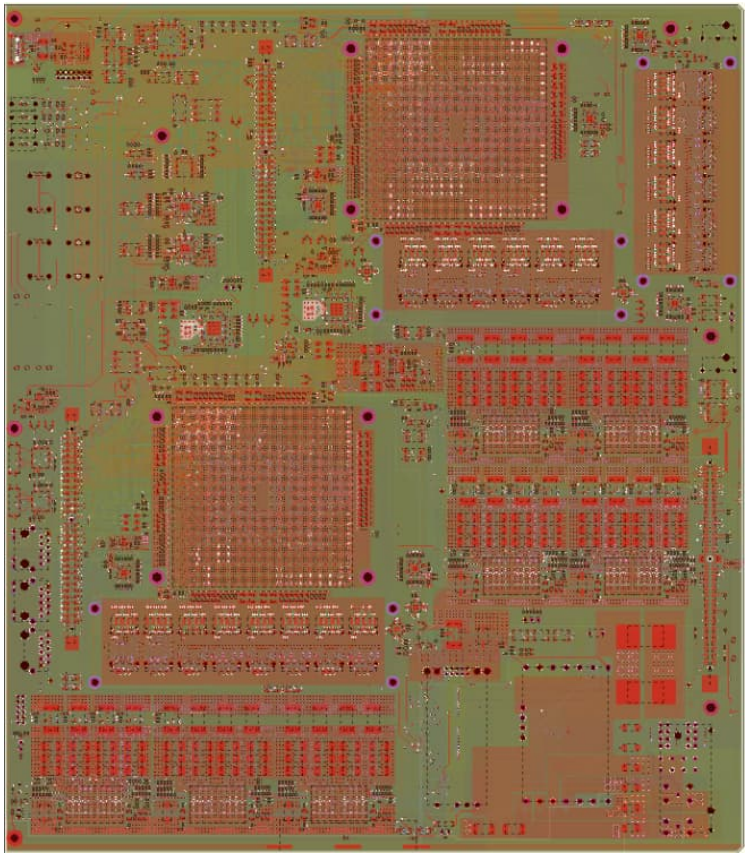
Provided by Alpha Novatech



- 6 FFs in vertical row, It is OK to meet 50 ℃ target with 40mm x 90mm x 13mm heatsink.

Summary

- A full-function GCM prototype has been designed for the new Global Trigger of ATLAS Phase-II Upgrade.
  - A high-speed, high power and high density ATCA front board.
- A systematic methodology has been adopted during this GCM design process to achieve simultaneously
  - Signal Integrity
  - Power Integrity
  - Thermal Integrity
- The Preliminary Design Review of this design is scheduled at end of Oct 2023.



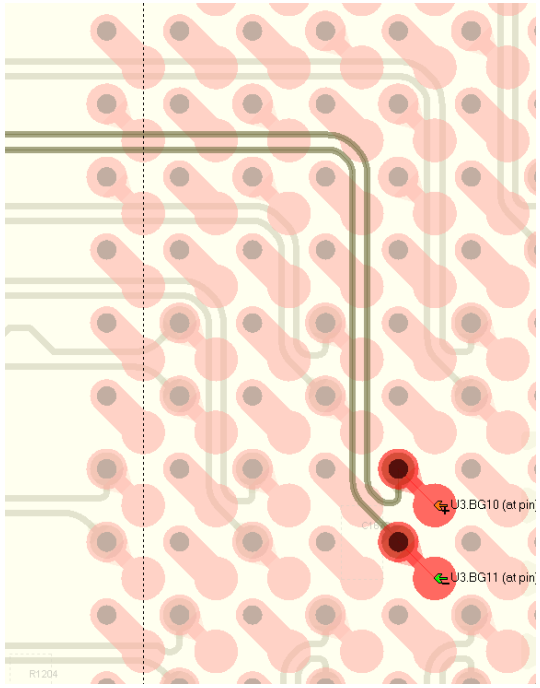
Backup

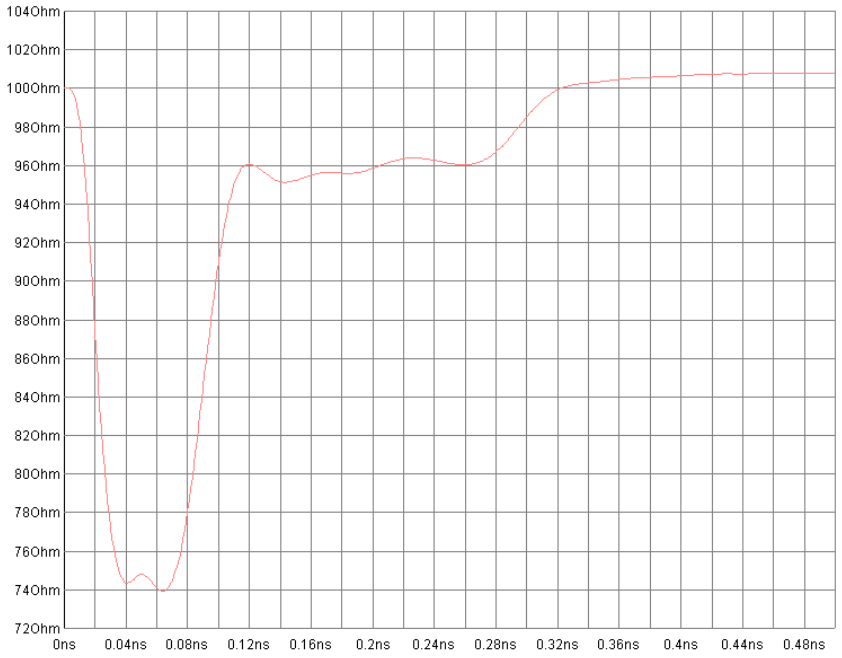
VP1802 Power Estimation

PDM Estimation	Node	Logic	BRAM18	URAM	DSP	Clock	Toggle Rate	GTM TX	GTM RX	GTY TX	GTY RX	Total Power (W)	Junction T with Hgh Profile Heatsink (about 0.4 C/W)
XCVP1802-1LSVC4072E (0.7V) CBE	MUX25G	1.0M / 30%	2965 / 30%	0/ 0%	0/ 0%	240MHz	12.50%	48 @ 25.78125Gb/s	48 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	62	44.4 C
	MUX10G	1.0M / 30%	2965 / 30%	0/ 0%	0/ 0%	240MHz	12.50%	48 @ 25.78125Gb/s	72 @ 12.8Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	70	47.8 C
	GEP	1.7M / 50%	4950 / 50%	1275 / 50%	7176 / 50%	240MHz	12.50%	1 @ 25.78125Gb/s	72 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	107	62.4 C
XCVP1802-1LSVC4072E (0.7V) MEV	MUX25G	1.0M / 30%	2965 / 30%	0/ 0%	0/ 0%	320MHz	12.50%	48 @ 25.78125Gb/s	48 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	73	48.6 C
	MUX10G	1.0M / 30%	2965 / 30%	0/ 0%	0/ 0%	320MHz	12.50%	48 @ 25.78125Gb/s	72 @ 12.8Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	81	51.9 C
	GEP	1.7M / 50%	4950 / 50%	1275 / 50%	7176 / 50%	320MHz	12.50%	1 @ 25.78125Gb/s	72 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	131	71.8 C
XCVP1802-1LSVC4072E (0.7V) MPV	MUX25G	1.7M / 50%	4950 / 50%	0/ 0%	0/ 0%	320MHz	12.50%	48 @ 25.78125Gb/s	48 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	106	62.1 C
	MUX10G	1.7M / 50%	4950 / 50%	0/ 0%	0/ 0%	320MHz	12.50%	48 @ 25.78125Gb/s	72 @ 12.8Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	108	62.8 C
	GEP	2.3M / 70%	6917 / 70%	1785 / 70%	10051 / 70%	320MHz	12.50%	1 @ 25.78125Gb/s	72 @ 25.78125Gb/s	4 @ 25.78125Gb/s	4 @ 25.78125Gb/s	165	86.0 C

- For all three type of Nodes, the GT links are the same in CBE, MEV and MPV. The differences are the clock frequency and resource usage.
  - CBE for GEP is about 107 W. (50% resources @ 240 MHz).
  - MEV for GEP is about 131 W. (50% resources @ 320 MHz).
  - MPV for GEP is about 165 W. (70% resources @ 320 MHz).

Traditional FPGA break-out pattern

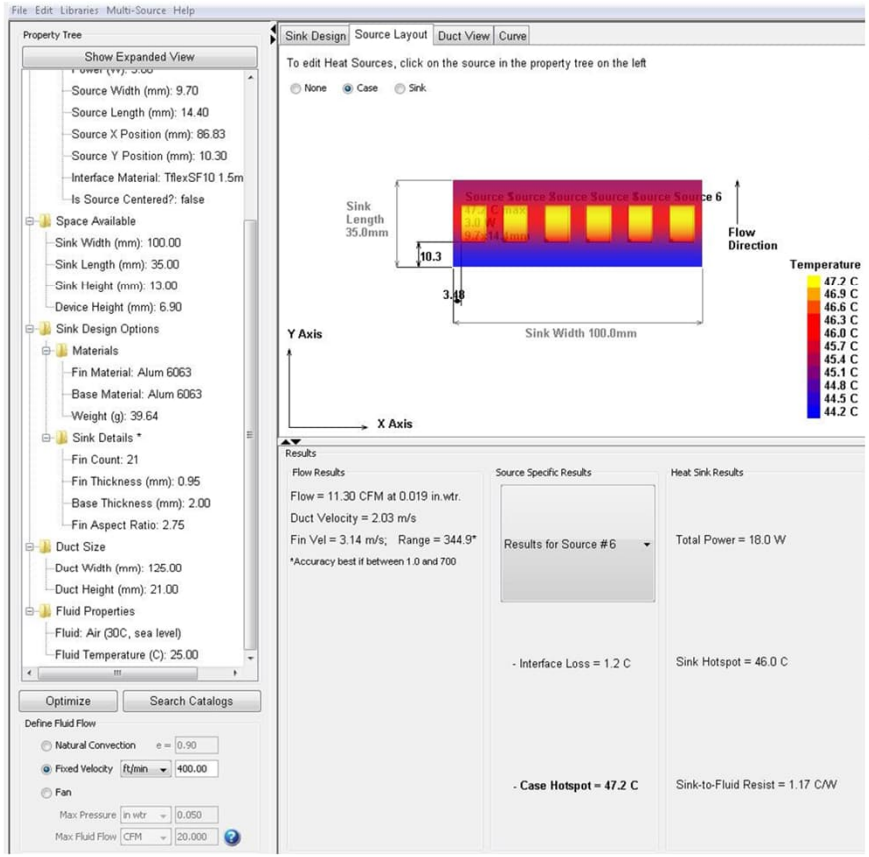




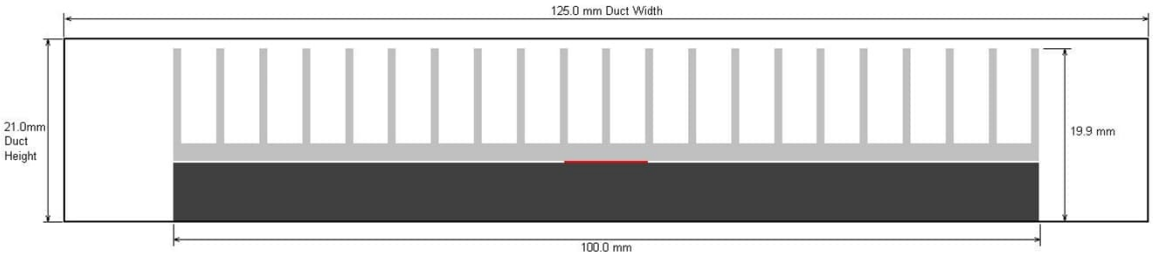
Simulated TDR response

GCM Thermal Simulation

- Heatsink design and simulation are outsourced
  - Firefly, horizontal block



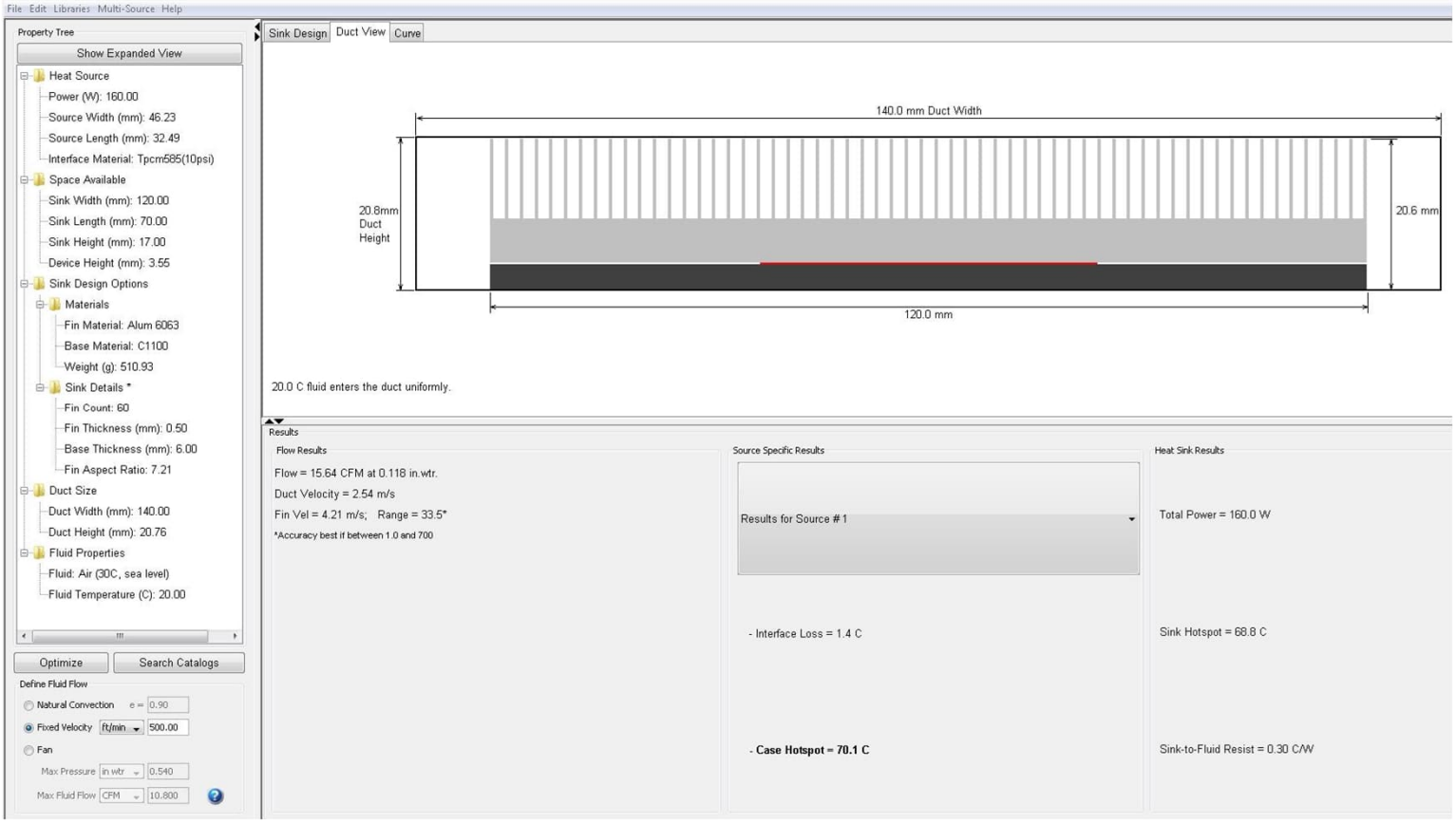
Provided by Alpha Novatech



- With 100mmx35mmx13mm heatsink, 6 modules horizontal group can meet 50 °C target under 400 LFM airflow.
- High performance gap pad material that can be used to compensate for the tolerance stack up from the multiple devices

GCM Thermal Simulation

- Heatsink design and simulation are outsourced
  - VP1802, 130mm x 70 mm x 17 mm on-board space reserved



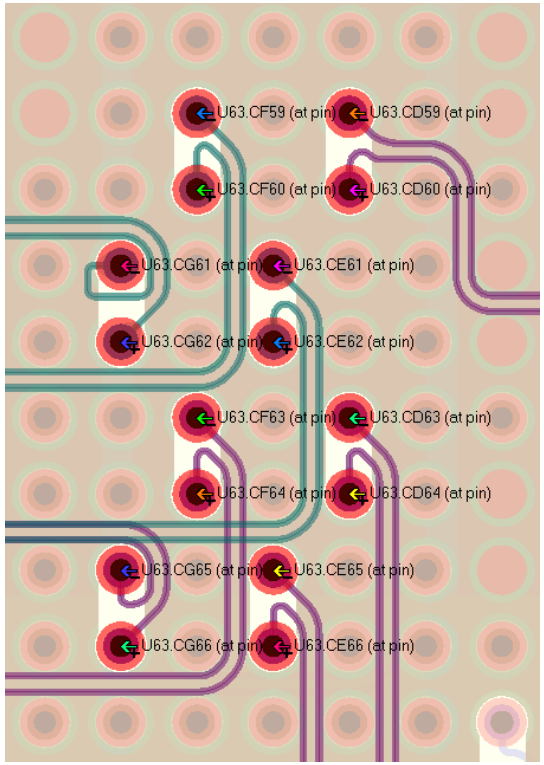
Provided by Alpha Novatech

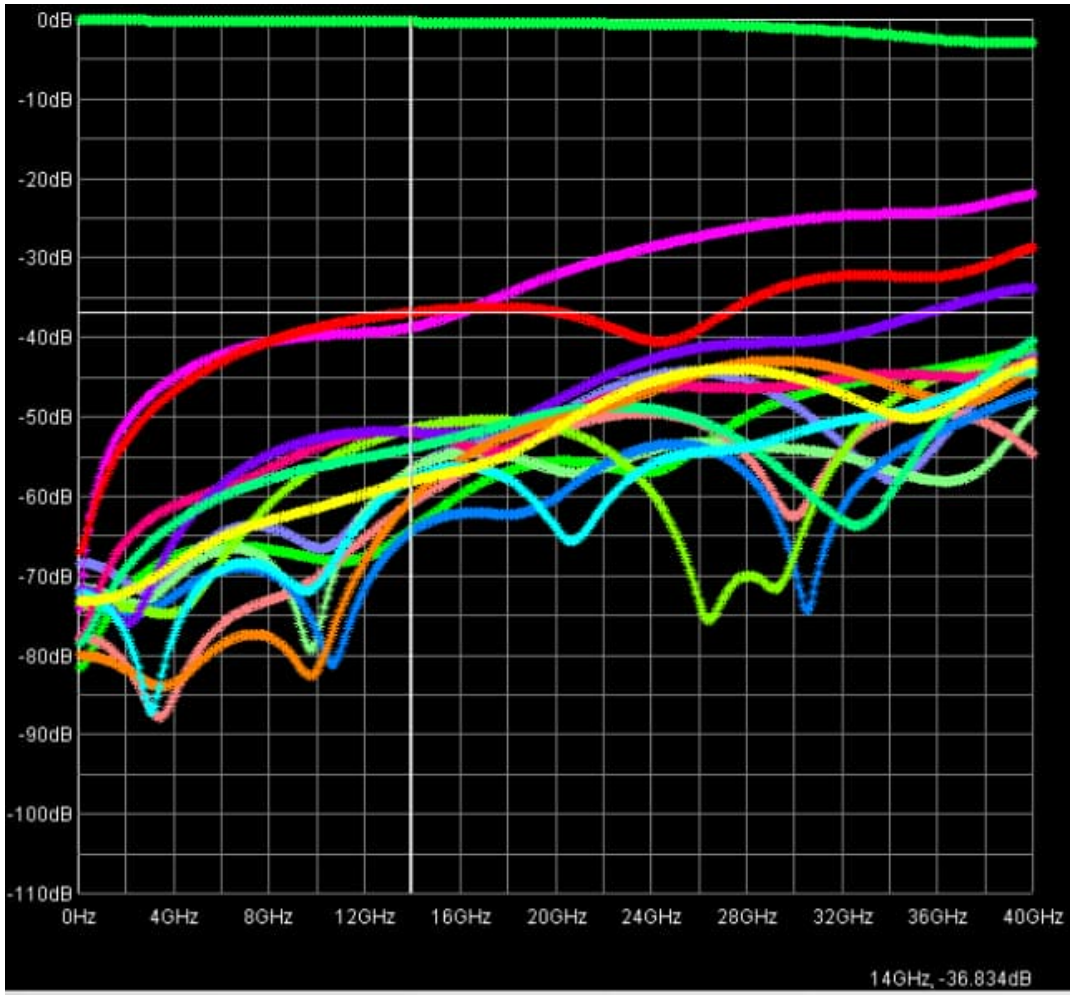
- 120 mm x 70 mm x 17 with 140 mm duct width
- Air flow: 500LFM
- Case temperature: 70.1 ℃ @ 160W
- Thermal resistance: 0.3 ℃/W

nVent SCHROFF ATCA shelf maximum air flow > 700LFM

GCM Signal Simulation

- Xilinx MGT Crosstalk Requirement for CEI-28G-VSR
  - Tx-Tx < -35dB
- GCM Tx-Tx < -36.8dB
  - Worst case





GCM Signal Simulation

- Xilinx Crosstalk Requirement for CEI-28G-VSR
  - Tx-Rx < -45dB
- GCM Tx-Rx < -60dB
  - Typical case