ETH zürich

Institute for Particle Physics and Astrophysics IPA

CMS ECAL VFE design, production and testing

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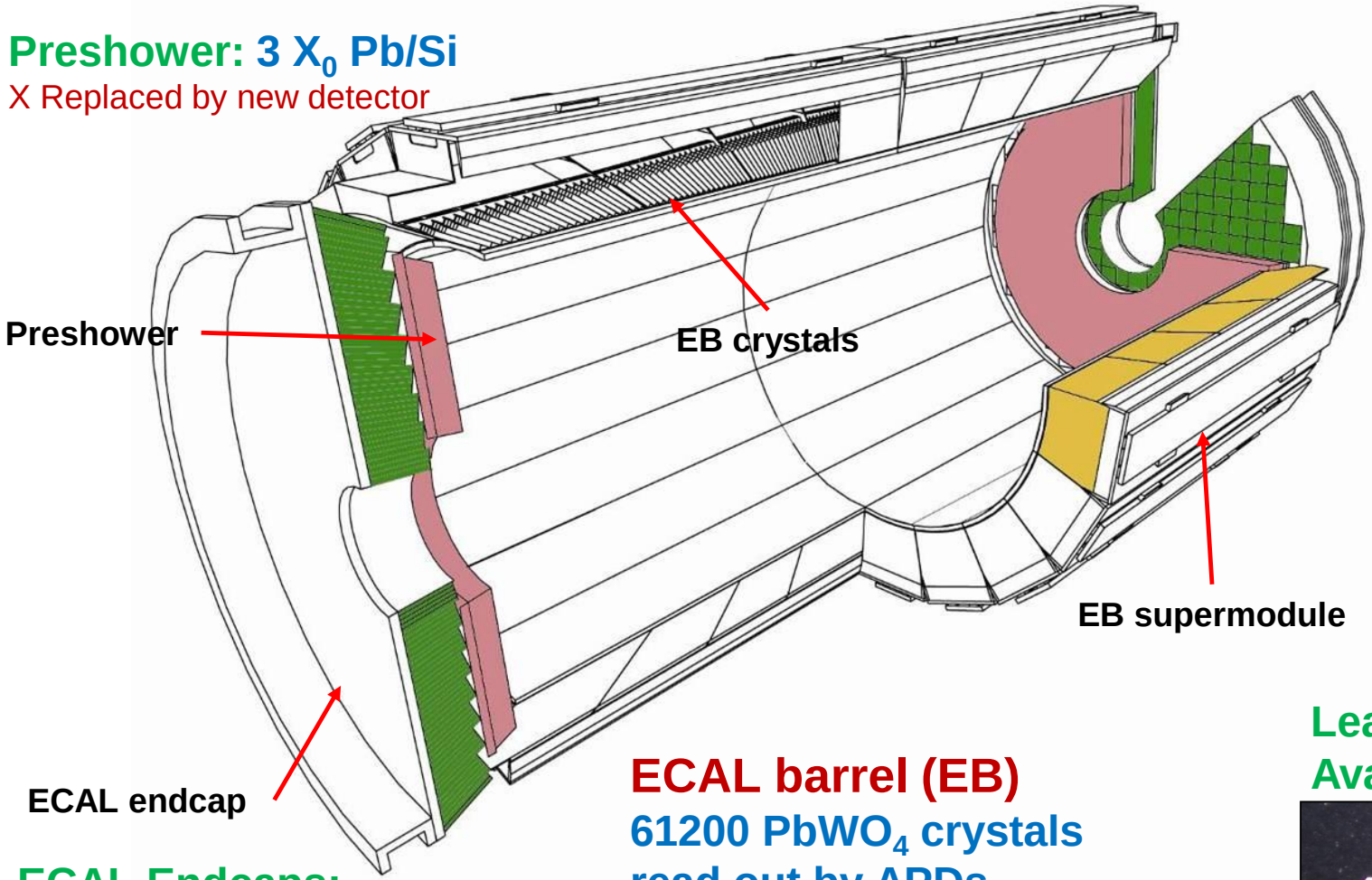
On behalf of the CMS collaboration

TWEPP2023, Geremeas, Italy

- Introduction
- VFE card
- Design, production and testing for reliability
- Production plan
- Test setup
- Environmental stress screening
- Summary

CMS Electromagnetic Calorimeter upgrade

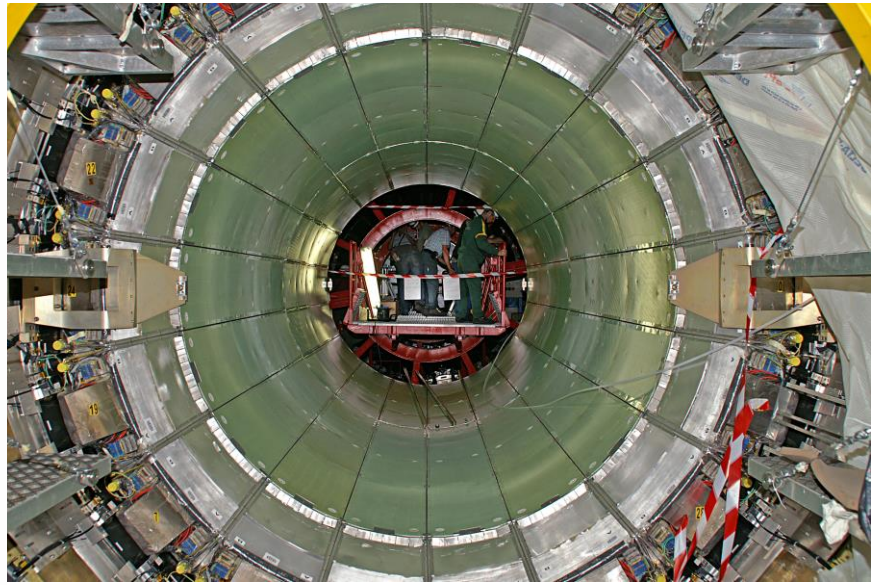
Preshower: 3 X_0 Pb/Si
X Replaced by new detector



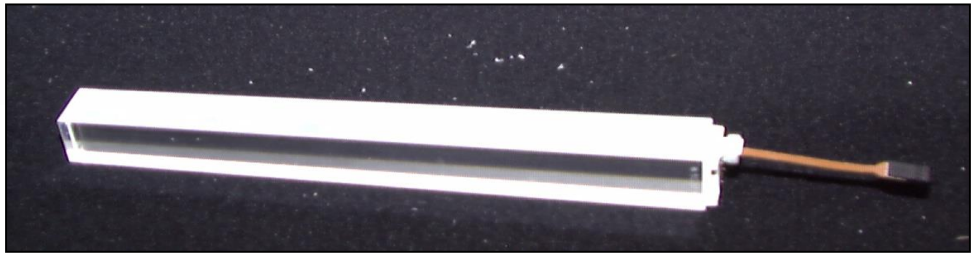
ECAL Endcaps:
14648 $PbWO_4$ crystals
read out by VPTs
X Replaced by new detector

ECAL barrel (EB)
61200 $PbWO_4$ crystals
read out by APDs
36 supermodules
Maintained - new electronics
Operation at lower temperature

ECAL barrel installed: July 27, 2007



Lead Tungstate ($PbWO_4$) crystal with Avalanche Photo-Diode attached



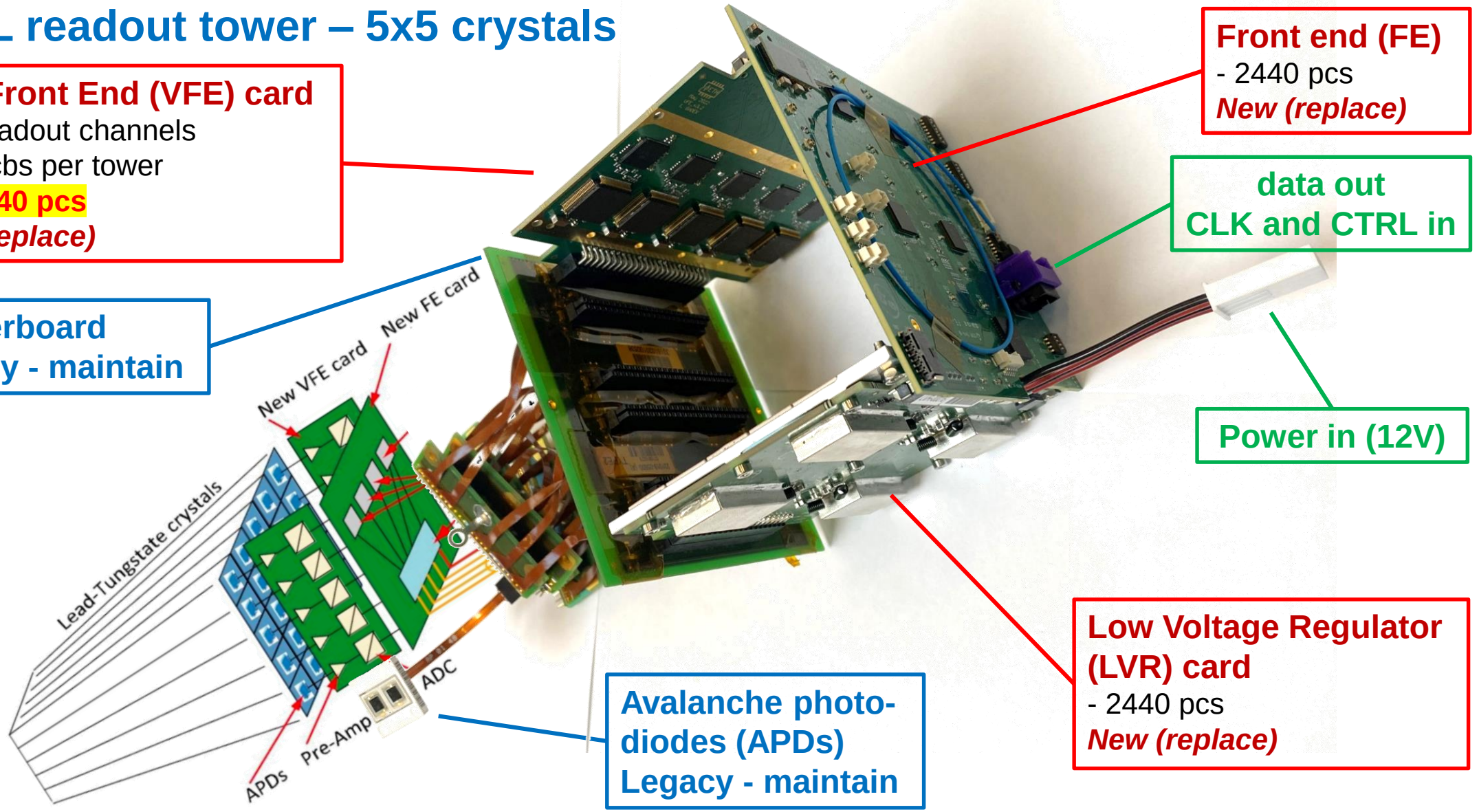
1 ECAL Barrel (EB) on detector parts – readout tower (RT)

ECAL readout tower – 5x5 crystals

Very Front End (VFE) card
- 5 readout channels
- 5 pcbs per tower
- **12240 pcs**

New (replace)

Motherboard
Legacy - maintain



Front end (FE)
- 2440 pcs

New (replace)

data out
CLK and CTRL in

Power in (12V)

Low Voltage Regulator (LVR) card
- 2440 pcs

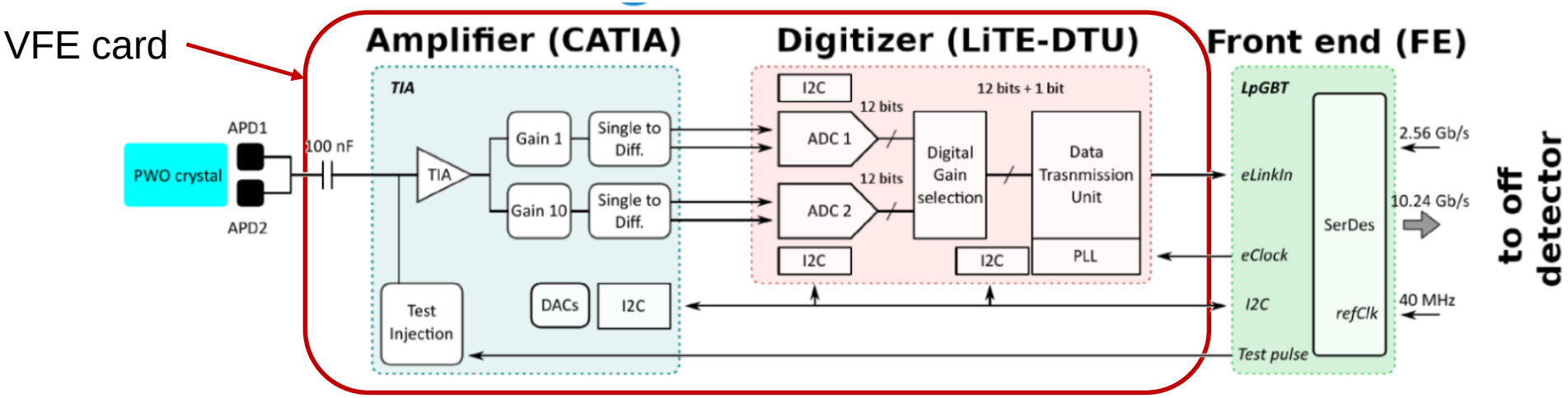
New (replace)

Avalanche photo-diodes (APDs)
Legacy - maintain

VFE card functionality - ASICs

New electronics – why:

- Longer level 1 trigger latency (12.5μs)
- Mitigates problems induced by high radiation levels at HL-LHC
- Introduces precision time measurement into ECAL: resolution 30 ps for E > 50 GeV
- Introduces data streaming: trigger primitives generation off-detector



CATIA (CEA Saclay)

- Trans-impedance amplifier ~35 MHz bandwidth
- Two gains differential outputs: 1 and 10
- Pedestal adjustment
- Internal test-pulse generator
- Internal temperature sensor
- I2C interface

LiTE-DTU (INFN Torino, LIP Lisbon)

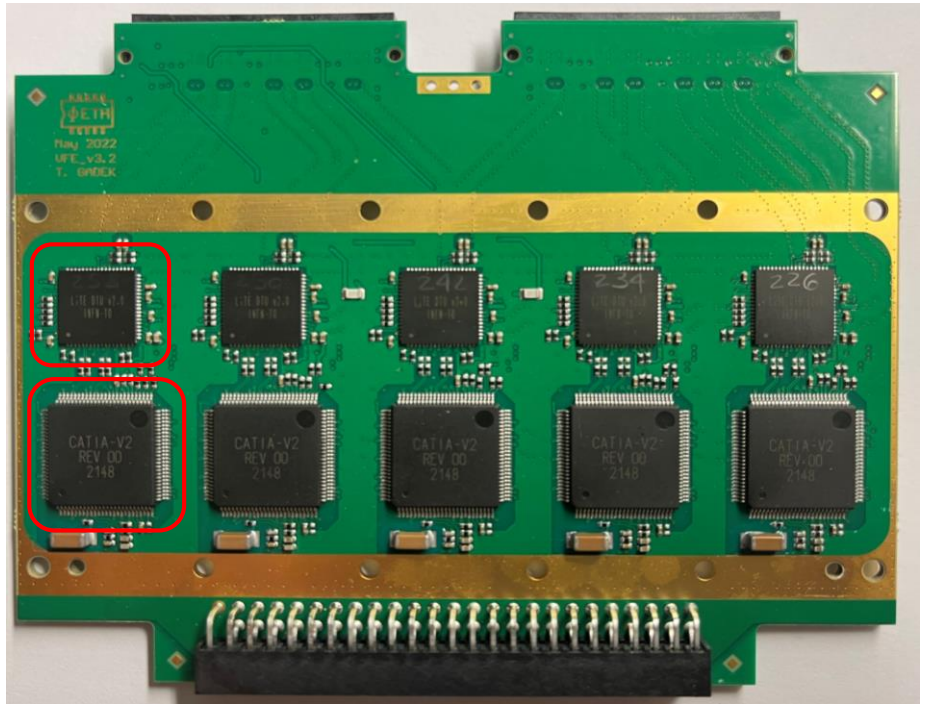
- Dual 12bit ADC, sampling at 160 MS/s
- 160 MHz CLK and fast control input
- internal PLL
- Lossless data compression
- Data streaming at 1.28 Gbit/s
- I2C interface

VFE card

- 5 identical channels: CATIA + LiTE-DTU
- 12240 pieces for CMS
- 340 pieces (spare supermodule)

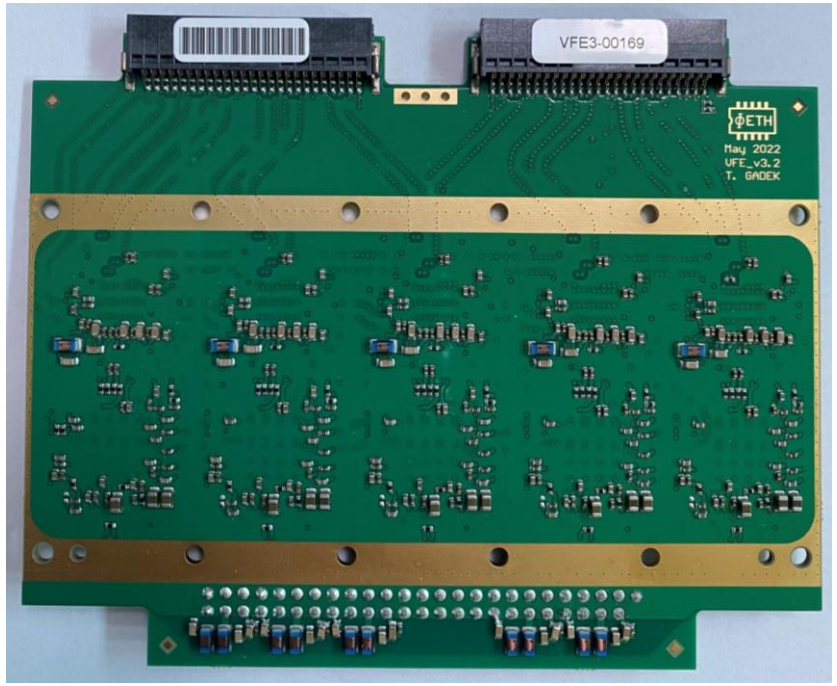
Production: 14600 cards
Including **pre-series: 400-500 cards**

- 8 layers, 35µm
- **626 components**, thereof:
  - 10 active (CATIA and LiTE-DTU)
  - Two SMD connectors (ERNI, TE connectivity)
  - One through hole connector (Samtec)
  - Connectors fit legacy system



Samtec connector

ERNI connectors



VFE life time and reliability desire

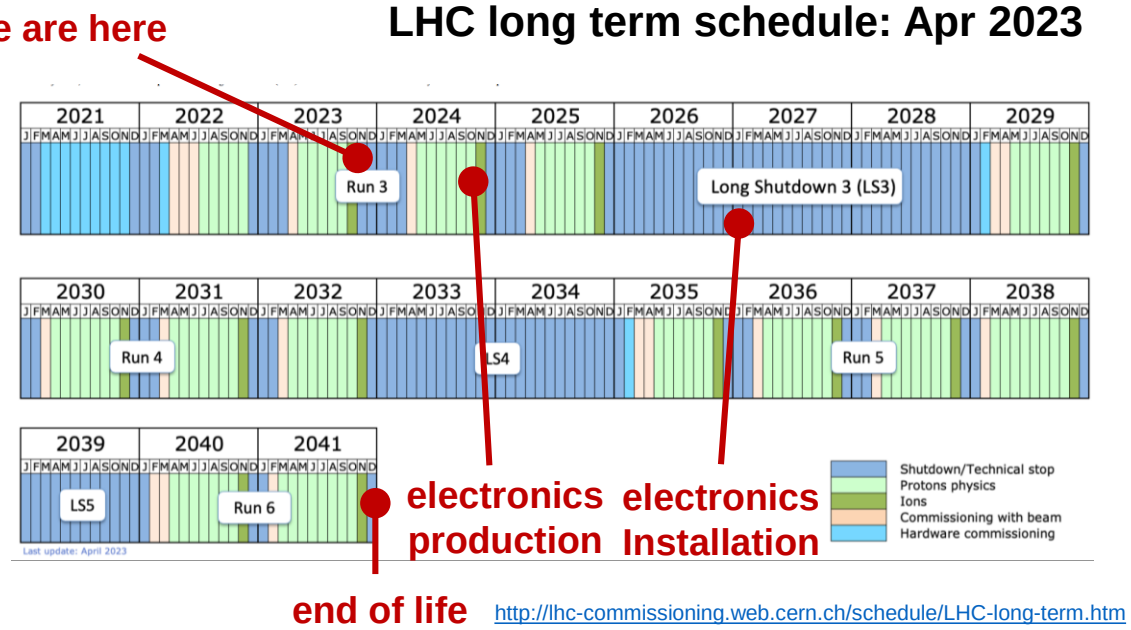
From (my) slide in 2005:

Life time: ~10 years
Maintenance: zero

Legacy electronics operational since 18 years
2 more years to come → total: 20 years

Just a miracle? How do we make it happen again?

LHC long term schedule: Apr 2023

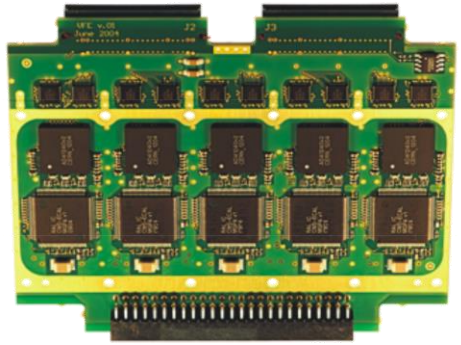


http://lhc-commissioning.web.cern.ch/schedule/LHC-long-term.htm

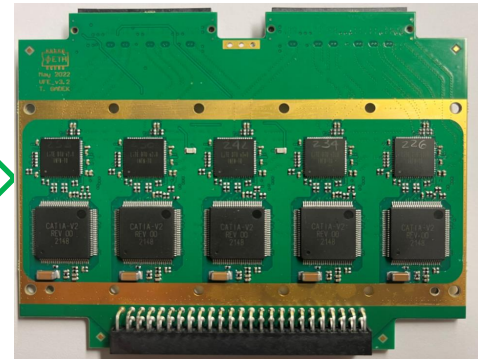
ECAL barrel:

- Single layer detector
- Missing channels impact energy resolution
- Missing readout towers permit electrons, photons to escape unidentified
- Repair practically impossible – not foreseen

OLD



Upgraded ECAL requirements:
Life time: ~20 years
Maintenance: zero
Goal: < 0.5% of failing channels at end of life



NEW

Design for reliability and manufacturing

Quality and Reliability start with the Design: PCB, PCB materials

Choice of PCB class standard:

Classes (IPC-6011)*: **require Class 3**

- Higher class: higher level of inspection and testing
- class 3/A (IPC-6012) – expensive (not used)
- Follow layout rules (or further relax), such as
  - Min. trace width and gap
  - Min. Via drill and pad diameter
  - Etc.
- More stringent requirements on annular rings
- Requirements on PCB dielectric
- Cross-sections of PCBs

IPC-A-600 Acceptability of Printed Circuit Boards

*Sierra circuits, IPC Class 3 Design Guide

PCB design and fabrication:

- Surface finish: **ENIG** (for solderability)
- Core and prepreg materials with **TG of 170°C**
- **Transmission line impedance: ±10%**
  - Tuned to standard materials
  - Control with test-coupons
- High speed signal guarding with **Via stitching**:
  CLK 160 MHz, 1.28 Gbit data, fast command
- **Through hole Vias only**
- Standard copper layers: **35µm**
- Design PCB panels (tbd with the assembler)
  - Add test coupons for impedance test

Design for reliability and manufacturing

Quality and Reliability start with the Design: components

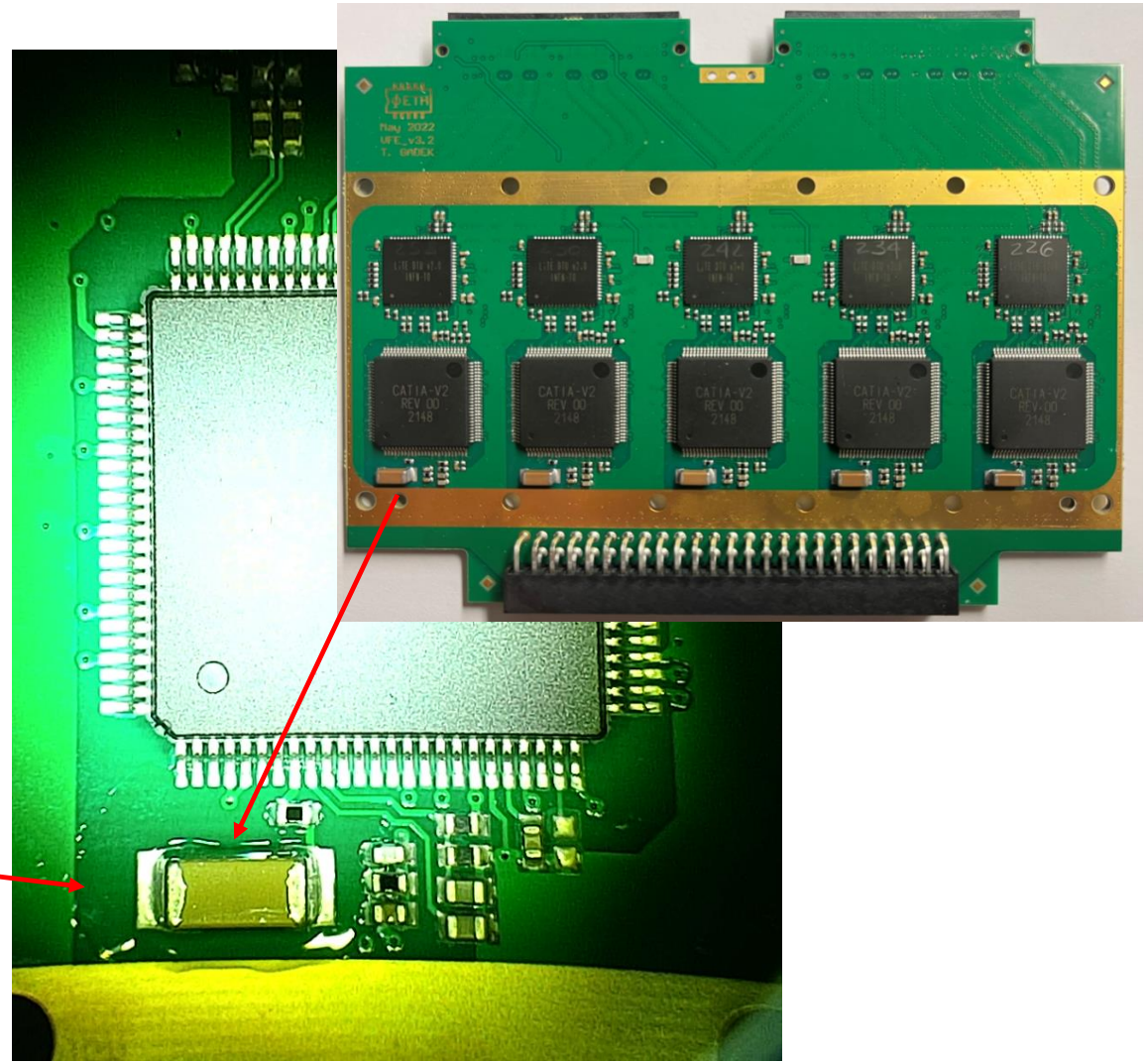
Components:

Automotive grade or better (AEC-Q200)

- SMD components: smallest **0402, 0603** where possible
- Gold plated connector pins
- No through hole technology (expect SAMTEC connector)
- Packaging for machines: **ESD trays, reels**
- **Derating** of components:
  - ~80% for voltage, current
  - ~50% for power
- **Coating** of higher voltage parts

Decoupling capacitor:

- **500V → 630V**
- **Coating**



Production for reliability of the VFE card

Quality and Reliability continue with: assembly standards, assembler and procedures

Choice of PCB assembly standard: Class 3

- Higher class: more stringent criteria on solder joints
- Less displacement of components tolerated:
  - <25% of component terminal off pad (class 3) vs <50% (class 2)
- Through hole filling >75% (class 3) vs >50% (class 2)

IPC-A-610 Acceptability of Electronic Assemblies

Required certification of Assembler

- ESD safe environment
- Assembler certified for quality assurance and control **ISO 9001** (or 13485)
- **Trained personal** for assembly following **IPC 610**
- **Trained personal** for rework and repair **IPC 7711/7721**
- Components management system

PCB assembly:

- Specified solder: SAC305 (standard, lead-free)
- Bake-out of components
- **Production in batches (500/week):**
  - Metallurgic cuts of few samples per batch
- Avoid (systematic) failure of large number of PCBs ➔ **Factory Acceptance Tests:** follows production pace
  - Automatic Optical inspection (AOI)
  - Electrical testing by the Assembler
  - Continuous monitoring of first pass yield: >95%
- Appropriate, established cleaning

Last but not least ➔ Environment protection

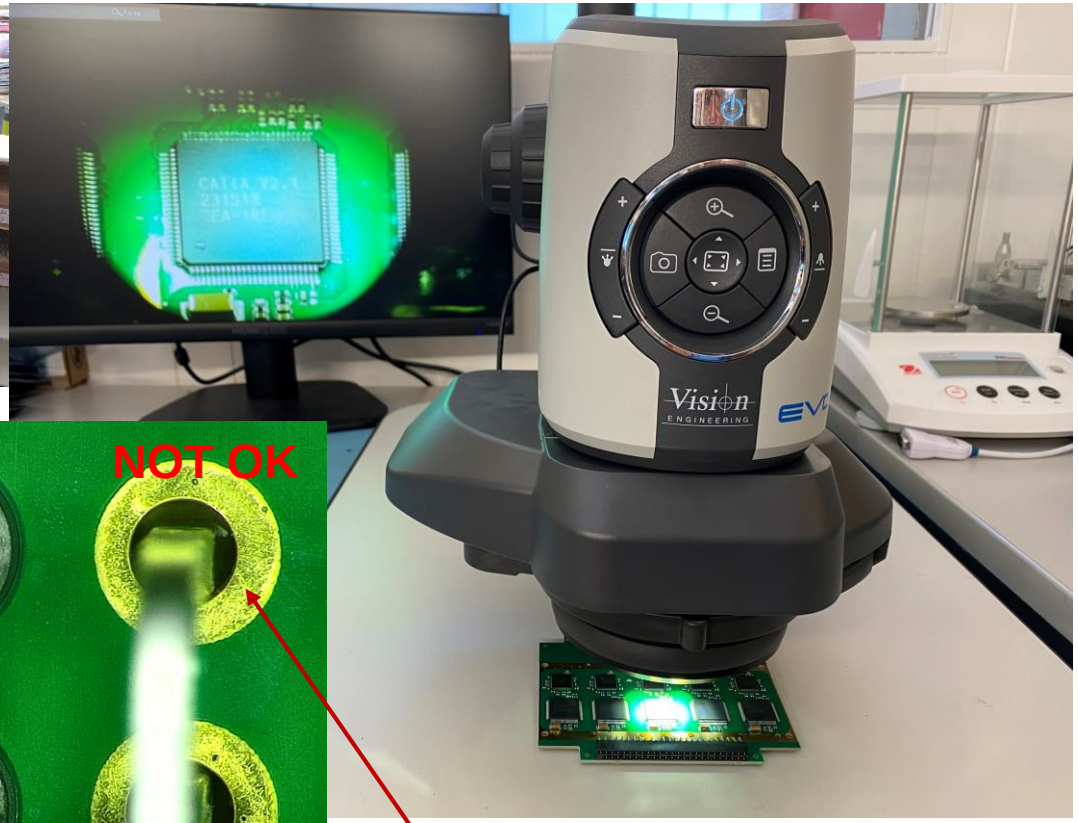
- **RoHS compliant** materials
- **ISO 14001** compliant

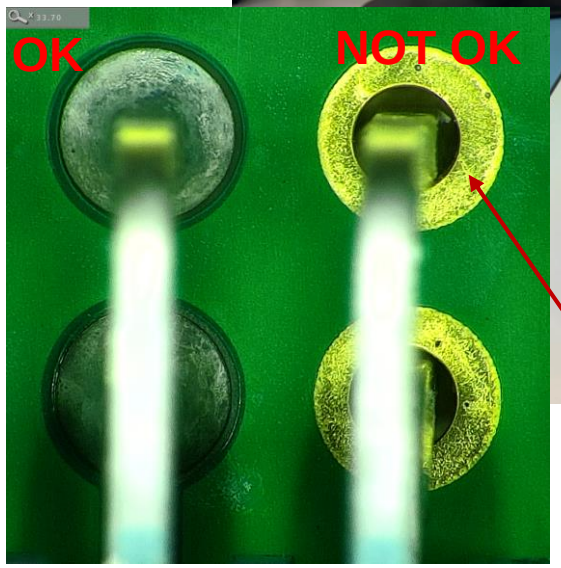
Testing for reliability

Quality and Reliability continue with: reception, testing and installation

Ensure ESD until the installation of the cards

Optical inspection tool – in house



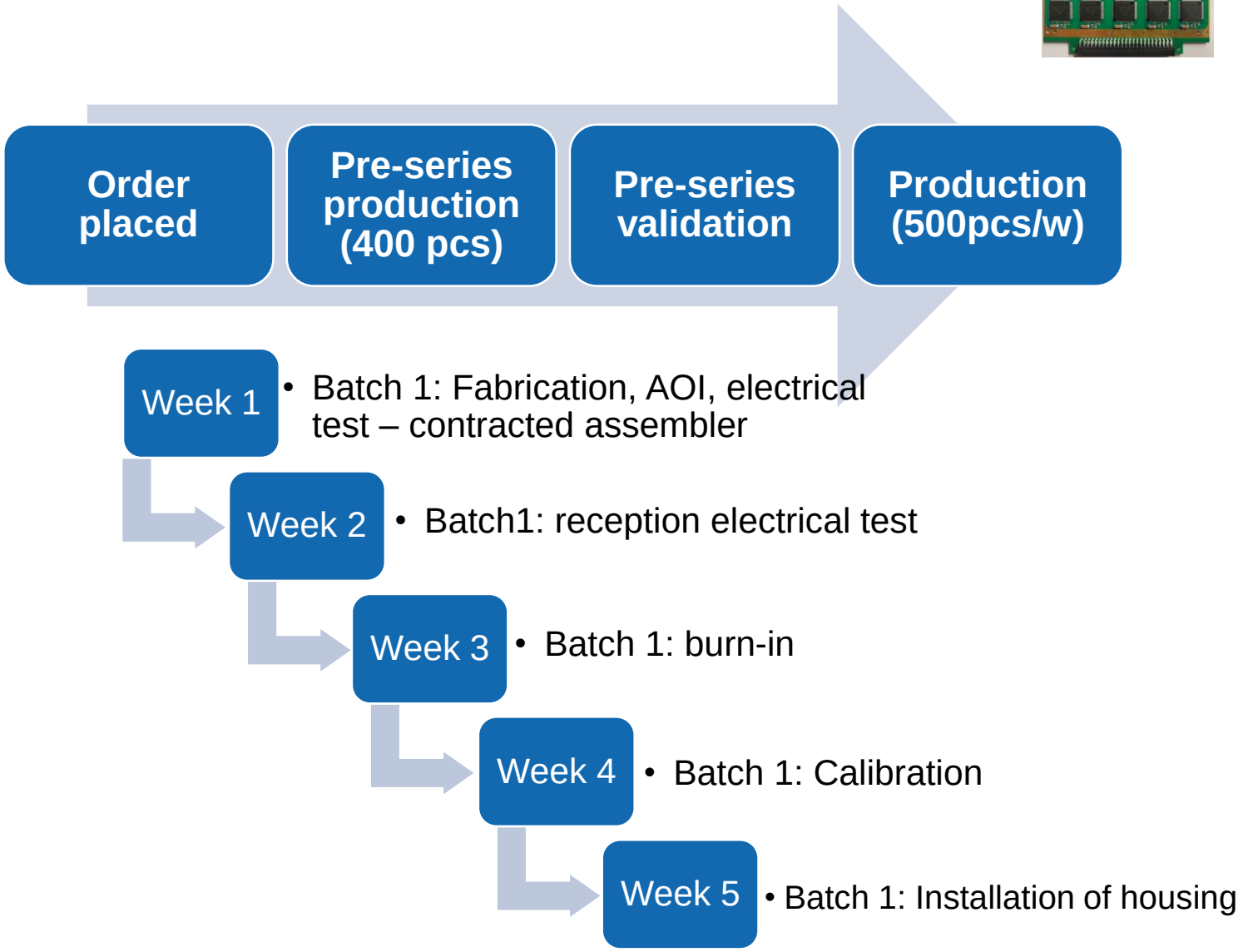


VIA not filled to 75%

2 VFE production plan – fabricate 14600 pcs

First there is a plan:

- Components:
  - All passives purchased by assembler, including PCB
  - Except: connectors, long lead time, already purchased
- Electrical Test-setups
- Manpower
- Pre-series qualification up to 3 months
- **ASIC testing done by industry:**
  - Launch VFE production with 10000 CATIA and 10000 LiTE-DTU in hand (4 weeks contingency)
- Testing, environmental stress screening, calibration and finalization follow the production pace



2 VFE test setup – easy to handle – fast test

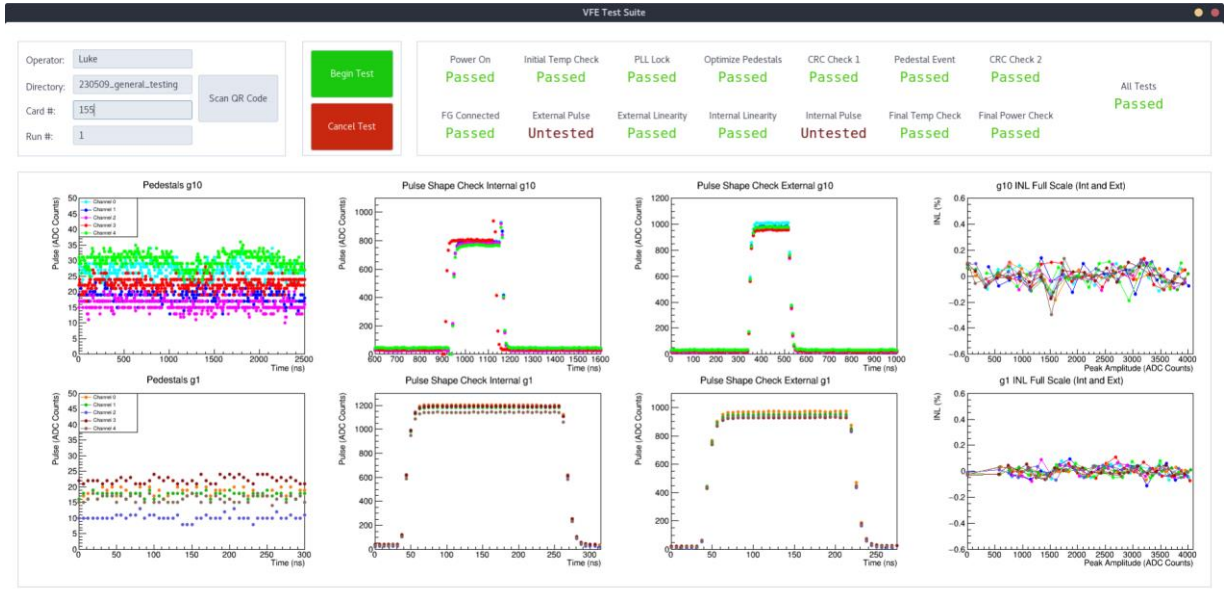
Test setup: 4 copies

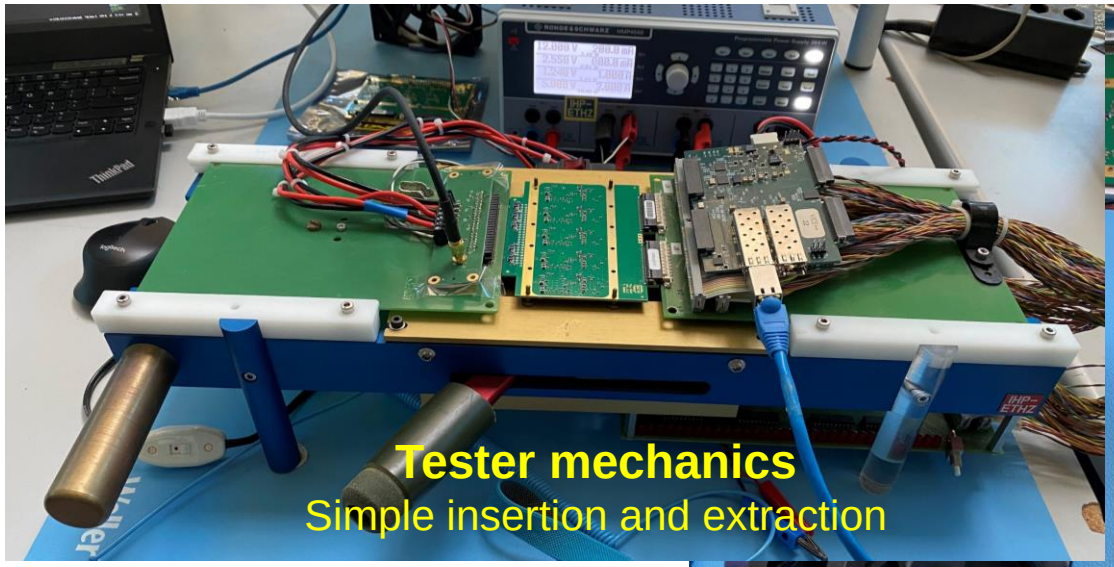
- Test by assembler
- Reception test at CERN
- Calibration in Torino
- spare

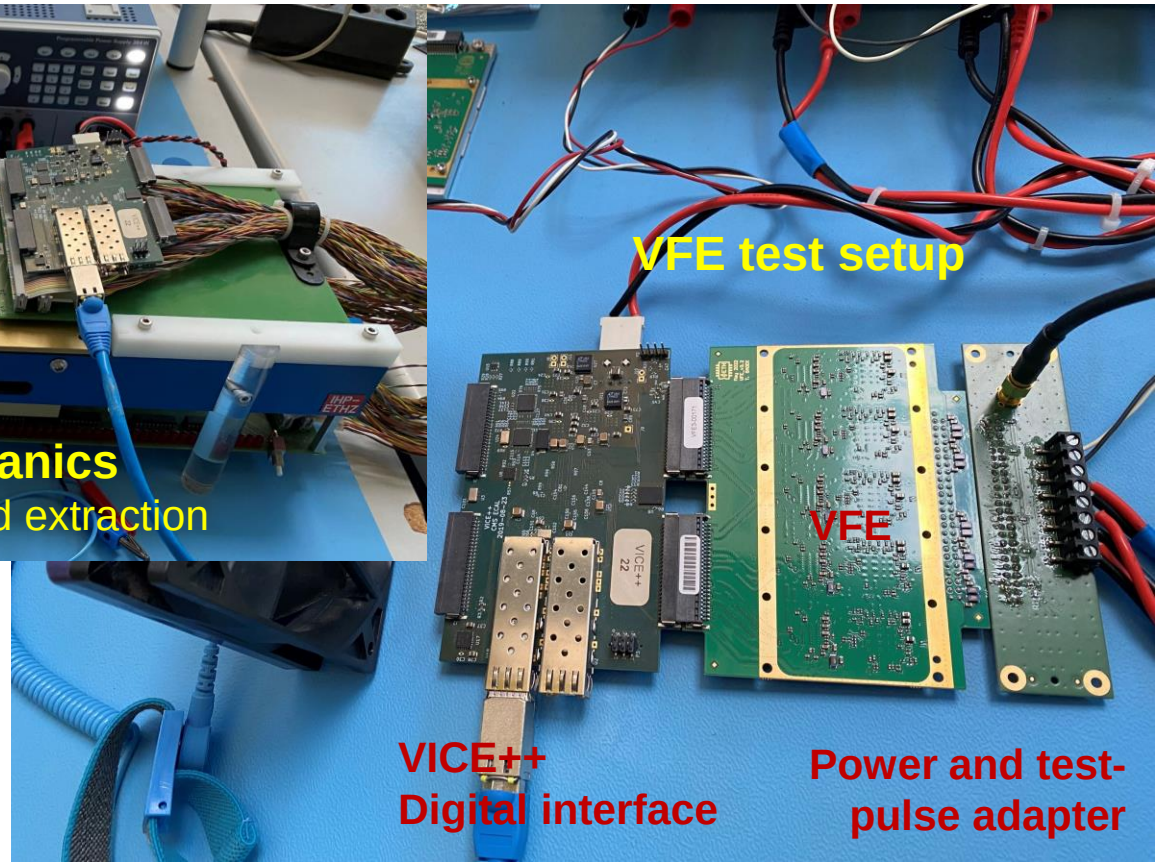
Features

- Fully automatized
- Data stored in DB

Test program GUI







Testing full functionality

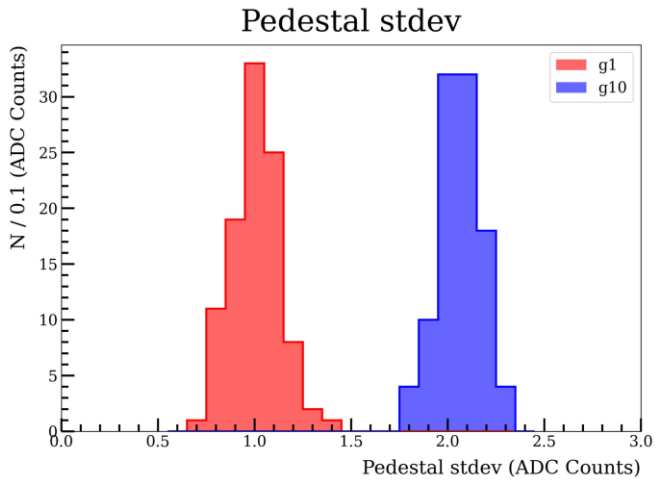
- PLL locking, CRC errors
- Pedestals, Test pulse
- More…

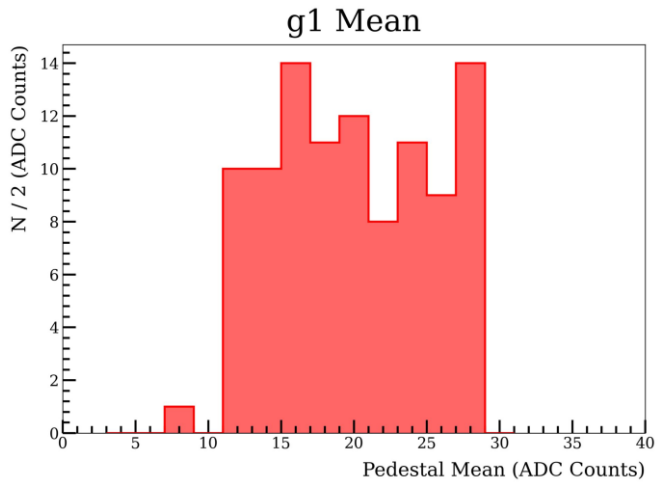
Test duration: ~1 min.

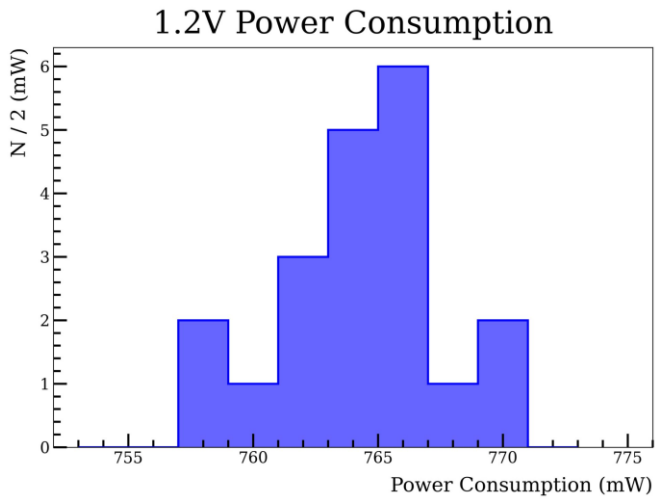
2 VFE test setup – results statistics - calibration

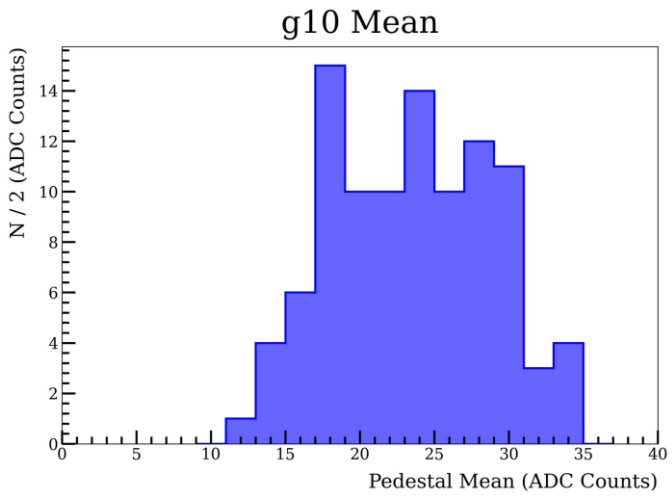
Measurement statistics identifies outliers

- Adjustment of pass/fail criteria



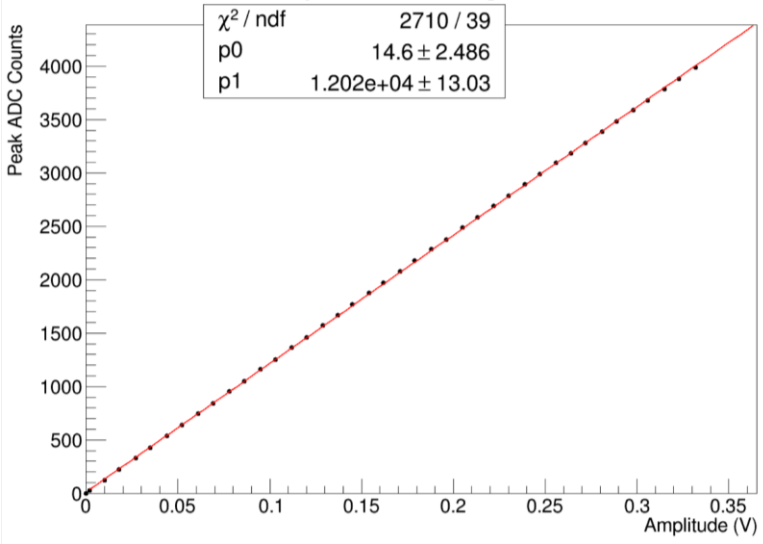






Optional pulse generator - precise calibration:

- Tektronix AFG31252
- 250MHz - 14bit – 2GS/s



6 Environmetal stress screening (burn-in)

Active burn-in setup for 500 VFE cards

- LVR and VFE cards simultaneously in the same setup:
  - safe powering of VFE
  - Correct load for LVR

Safety

- Siemens PLC system
- Two temperature sensors per box
- Interlock of power supplies

10V, 40A supplies **Keithley DAQ 6510**

Stable temperature ~70ºC reached

Test box

- PCB housing with extra fans
- 9 towers
- Total: 12 boxes

Monitoring and control

Monitoring: Keithley DAQ 6510

- Two temperatures per tower
- T_stability: ±1.5ºC
- T_spread: ~5ºC

Arduino microcontroller:

- Power good of LVRs
- Fan speed control

Laptop

- Power supply control
- Software

Dedicated aging study (50 VFE, 10 LVR):

- Temperature cycles: ambient - 70ºC (power OFF – ON)
- Identify end of infantile mortality and end of life
- Age all cards until after infantile mortality

Summary

Keys to success, for high quality high reliability VFE cards in a large scale production:

Design for Reliability and Manufacturing

- Application of appropriate standards

Components selection and ASIC testing

Production and testing have to go hand in hand

- Production, reception and qualification plan
- Selection of appropriate assembly company
- Production yield monitoring
- Factory acceptance tests

In house reception and qualification testing:

- Electrical testing, environmental stress screening, calibration

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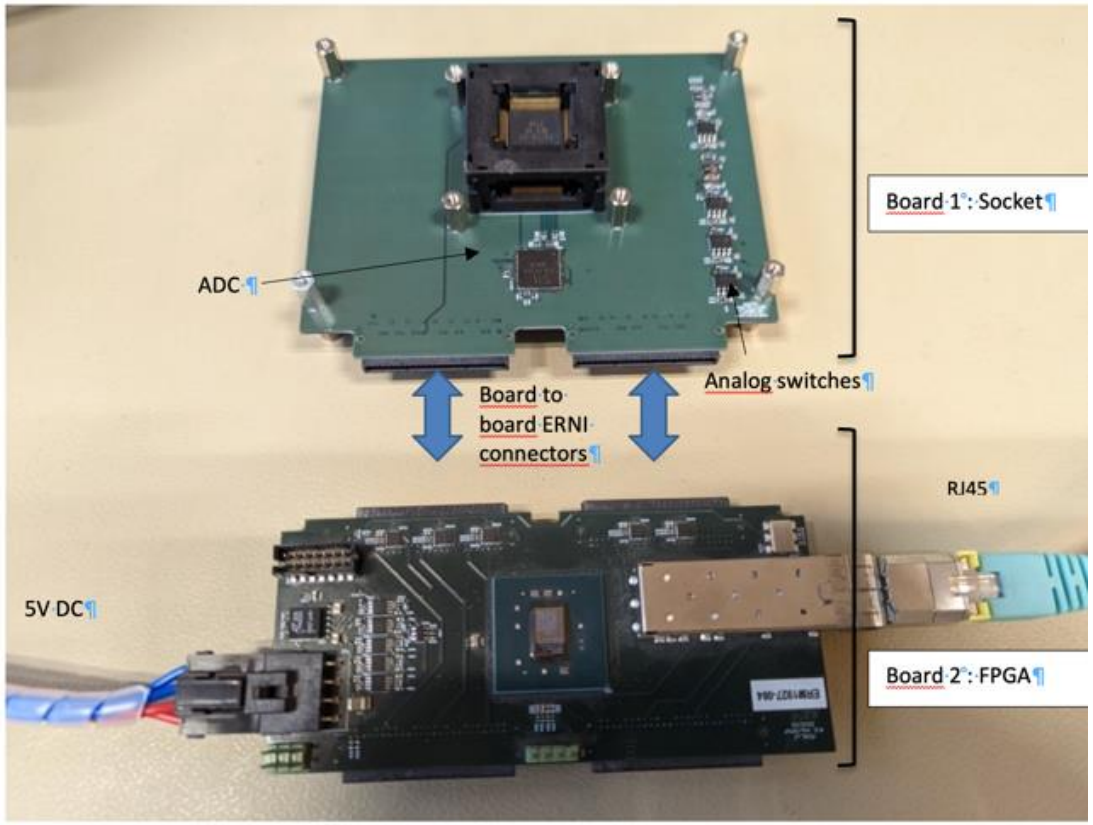
Additional material

2 Testing of ASICs

- **CATIA: CEA-Saclay**
  - Test setup prepared
  - To be done in industry



- **LiTe-DTU: INFN Torino**
  - Test concept defined,
  - Testing and setup preparation by industry partner