



Contribution ID: 47

Type: Oral

CMS ECAL VFE design, production and testing

Tuesday 3 October 2023 18:00 (20 minutes)

Maintaining the required performance of the CMS electromagnetic calorimeter (ECAL) barrel at the High-Luminosity Large Hadron Collider (HL-LHC) requires the replacement of the entire on-detector electronics. 12240 new very front end (VFE) cards will amplify and digitize the signals of 62100 lead-tungstate crystals instrumented with avalanche photodiodes. The VFE cards host five channels of CATIA pre-amplifier ASICs followed by LiTE-DTU ASICs, which digitize signals with 160MS/s and 12bit resolution. We present the strategy and infrastructure developed for the testing, burn-in, calibration and assembly of the VFE cards. Moreover, we summarize the test results obtained with 60 prototype cards.

Summary (500 words)

The electromagnetic calorimeter (ECAL) [1] barrel of the Compact Muon Solenoid (CMS) experiment [2] is made of 61200 lead-tungstate crystals read out by avalanche photodiodes (APDs). Its readout electronics are arranged into towers of 5x5 channels, comprising five very front end (VFE) cards (Fig. 1), one digital interface card (FE) and one low voltage regulator card (LVR) conditioning the power of one tower. Each VFE card hosts five channels of a pre-amplifier (CATIA) followed by an analog-to-digital converter (LiTe-DTU). The tower electronics will be replaced for operation at HL-LHC in order to maintain ECAL's performance under increased luminosity conditions. This involves the production and testing of ~14000 new VFE cards.

ECAL is a single layer detector. Missing readout channels degrade the energy resolution and missing towers may allow photons or electrons to remain unidentified. Extracting an ECAL module for repair requires several months and is not foreseen for the operation period of ~20 years. Another important aspect is the monitoring of the production yield, avoiding complete failures of production batches.

Therefore, quality control is of highest importance. We are aiming at <0.5% of all channels failing at end-of-life. We will achieve this applying a bundle of measures:

- We require class 3 for the VFE PCBs.
- ESD protection will be systematically implemented at all steps.
- We produce ~500 VFEs per week, fast enough to complete the production in ~6 months and slow enough to follow the production with testing and burn-in.
- VFE cards are tested first by the manufacturer, using automatic optical inspection and a ~1min electrical test. The same electrical test is repeated at the reception of the cards followed by accelerated aging with thermal cycling. Finally, the cards are electrically tested again and if fully operational, calibrated.
- Failing cards and outliers are excluded from further use. Healthy cards are assembled with their mechanical housing and the thermal interface materials.

An electrical test setup has been developed, comprising:

- An FPGA based interface card connecting the VFE via ethernet to a PC
- A signal and power interface card.
- A computer-controlled power supply.
- A precision test pulse generator (optionally).

We scan the pedestal setting of the CATIA, the PLL locking range of the LiTE-DTU and perform gain and linearity measurements with internal and external test-pulses (see figure 2). We develop test software with a graphical user interface (see figure 3).

The VFE card burn-in is done simultaneously with the LVR card burn-in. In this way we have correctly

conditioned power for the VFE cards and at the same time the LVR cards have the correct load. We are self-developing appropriate cabinets. Heating is provided by the dissipated power of the electronics under test and cooling is achieved by ventilation with ambient air. Three cabinets hosting up to 200 VFE cards each, will enable to follow the production pace. The detailed aging procedure will be defined in a dedicated test of pre-production cards.

Author: LUSTERMANN, Werner (ETH Zurich (CH))

Co-authors: SINGOVSKI, Alexander (University of Notre Dame (US)); DOLGOPOLOV, Alexandre (University of Notre Dame (US)); Mr ABADIJEV, Daniel (Northeastern University (US)); Prof. DISSERTORI, Guenther (ETH Zurich (CH)); STACHON, Krzysztof (ETH Zurich (CH)); MARTIN, Luke Thomas (Northeastern University (US)); DEJARDIN, Marc (Université Paris-Saclay (FR)); GADEK, Tomasz (ETH Zurich (CH))

Presenter: LUSTERMANN, Werner (ETH Zurich (CH))

Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability