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Best Practices in Design Verification of ASICs for High Energy Physics Experiments

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As the complexity and costs of ASICs designed for high-energy physics experiments continue to soar, verification emerges as a crucial factor in completing projects within reasonable timelines and budgets. Recognizing the escalating significance of verification, CERN and other high-energy physics institutes have invested significantly in enhancing the rigor of this essential process. In this talk, we emphasize the critical role of verification, delve into the unique challenges posed by ASIC designs in HEP, and discuss a set of best practices aimed at enhancing verification efficiency. By improving the quality of the verification process, these practices pave the way for predictable project execution and improved product outcomes. Drawing on successful experiences from ASIC verification at CERN and lessons learned from ineffective strategies, this talk provides valuable insights for achieving successful ASIC designs in high-energy physics experiments.

Summary (500 words)

FE readout ASICs are responsible for receiving analog signals from a sensor, converting them into digital signals, and transmitting the resulting values outside of the ASIC. Typically, a FE readout ASIC includes multiple readout channels, which can range from 1 to over 1,000,000, as well as a data transport layer that combines the data from all active readout channels and sends it to the outside world. Each readout channel is a mixed signal circuit that consists of an analog portion for signal shaping and discrimination and a digital module for measuring one or more characteristics of the digitized signal. The digital module also carries out functions such as filtering, data compression, and transmission of the resultant values.

FE readout ASICs perform similar functions with minor variations to meet detector requirements. Therefore, to achieve their verification goals, similar verification strategies can be used. Several best-known methods (BKMs) that are applicable to the verification of FE readout ASICs are presented in this paper to summarize these strategies.

The following is a brief list of BKMs discussed in this paper:
1. Design partitioning to handle longer simulation times during netlist verification
2. Greybox reference models to reduce reference model complexity
3. Approximate and precise scoreboarding
4. Readout data recording at a higher abstraction level for offline scoreboarding
5. AMS simulations at the channel level to identify issues at analog/digital boundaries that cannot be found in digital simulations
6. Define and capture Key Performance Indicators (KPIs) such as detection inefficiency, error rates, link losses, etc.
7. Readable register layer and test scenario dump to improve KPI tracking and debugging
8. Reuseable verification components that promote content reuse across projects and enable building complex verification environments with multiple ASICs

Although some of these BKMs are solely related to verification, several also address architectural and design partitioning aspects that significantly impact the verification process. All the BKMs discussed in this paper are based on our experiences of working on various FE readout ASIC projects at CERN. In the contribution, we will elaborate on each BKM and show examples from concluded and ongoing projects on how following them improved verification quality and efficiency.

While most of the BKMs discussed in this paper are already well-known among verification engineers, this article is the first attempt in the HEP community to summarize them for a wider audience. Future FE readout ASIC projects can use these BKMs as design and verification guidelines to avoid common pitfalls that were encountered during the development of various FE readout ASICs designed for HL-LHC upgrades. By following these relevant guidelines, design teams can increase productivity and prevent unforeseen project delays.

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