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FPGA Firmware design with High Level Synthesis: Methodology, gains, and pitfalls

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High Level Synthesis (HLS) of FPGA firmware using C/C++ has been popular in the design of upgrade trigger systems in High Energy Physics, allowing physicists with no previous firmware expertise to efficiently design digital systems. This presentation will describe the methodology of HLS designs, including comparison of basic building block design of HLS and Hardware Description language (HDL).
Design examples from the CMS L1 trigger system will be presented along with pitfalls to provide a proposed efficient approach to system design with these methods

Summary (500 words)

Firmware development using High Level Synthesis (HLS) of C/C++ code is a novel methodology that enables fast development of FPGA firmware by directly converting C++ code to Hardware Description language (HDL) using a set of conversion rules. The method has been sucessful in high energy physics experiments, allowing graduate students to contribute to firmware development, inreasing the effective personpower on the relevant projects.
This presentation will cover the basic methodology, the lessons learned from its application in Run-3 and HL-LHC trigger upgrade of CMS, and pitfalls to avoid when using HLS.
Initially, the methodology of writing C code while thinking in parallel will be explained, along with the code optimizations (pragmas) used to map the C code to HDL logic. Details will be provided on how to control the pipeline and map logic to specific hardware. Examples of simple modules will be provided comparing a direct HDL implementation with an HLS one comparing utilization, clock speed, and latency. The HLS gains in DSP related developments and in synchronization of different pieces of logic will be demonstrated. Examples where the method does not succeed in creating good logic will be shown, along with strategies on how to avoid these problems. The talk will be tailored to the level of young engineers and graduate students starting with HLS development for their projects.

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