ASIC validations using Cadence PROTIUM platform and application of PROTIUM Black Box flow on MIMOSIS-2 ASIC

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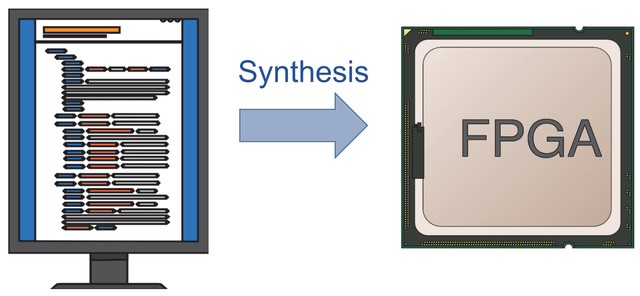
Goals

- Use of the Cadence Protium prototyping platform for ASIC functional validation and DAQ development.
- Application of PROTIUM's advanced Black Box flow to the MIMOSIS-2 ASIC (chip for the CBM experiment's micro vertex detector) to achieve the ASIC's nominal frequency between the DAQ and the prototype.

FPGA-Based Prototyping

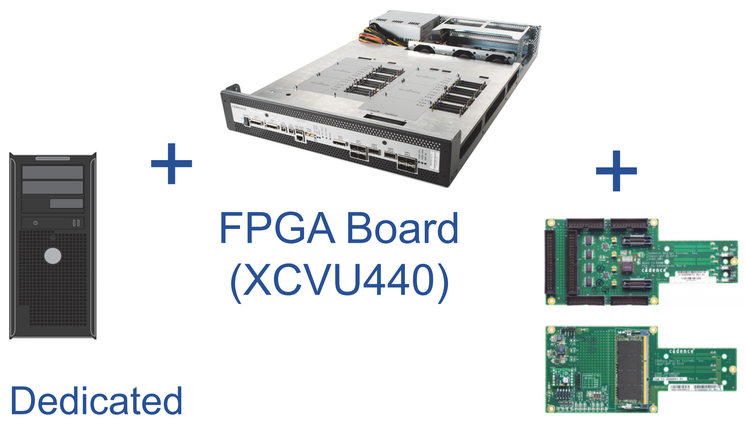
Principle

Map ASIC RTL code into FPGAs



Benefits of FPGA prototyping:
- Pre-silicon verification
- Firmware/Software verification
- Connect hardware

What is PROTIUM?

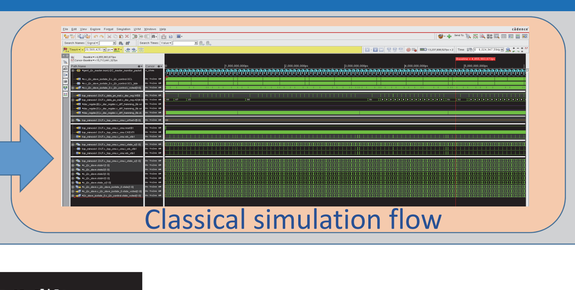


Benefits of PROTIUM Platform

Fast Bring-up:
- Little or no RTL modifications
- Fully automatic
- Faster verification runtime than classical simulations

Advanced PROTIUM Black Box flow:
- ASICs and IPs (custom or Xilinx) implemented inside the same FPGAs
- Achieves the ASIC's nominal readout frequency between PROTIUM and external hardware

Standard and Black Box PROTIUM environment



Standard PROTIUM flow:
- **Logic equivalence** between ASIC and PROTIUM prototype
- Automatic implementation (synthesis + PNR +STA) => **no need of special FPGA skills**
- **Full chain verification** of the Digital part of ASIC
- Ability to **connect external hardware** (DAQ, memories, ….)

Tools environment:
- Cadence software
- Tcl scripts
- Vivado Chipscope (JTAG access to FPGA register)

Prototyped ASIC frequency:
max 150 MHz for PROTIUM S1, **typ tens of MHz**

Black Box Flow:
=> Combination of **Std PROTIUM Flow** + Classic **FPGA flow**

Design of the Black Box:
Done as a FPGA project with Xilinx Vivado and mapped on XCVU440 FPGA

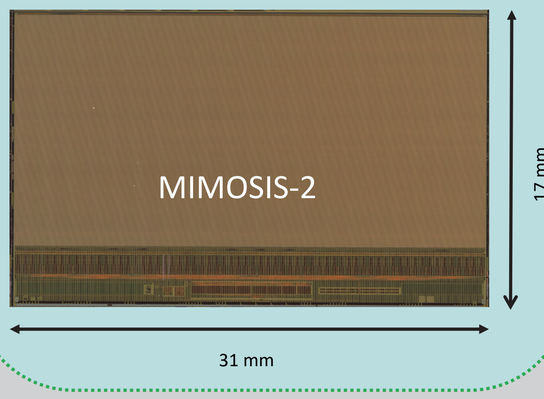
Access to full FPGA capabilities and IP
- PLL, RAM, DSP, ….
- normalized IP (PCI, Ethernet, USB,…)
- High speed link (up to 12,5Gps in differential)

Application on MIMOSIS-2 chip

MIMOSIS-2 (see F.Morel talk)

- Designed for **the CBM-MVD in a 180 nm CIS** technology
- **Reticle size** ASIC
- **0,5 M of pixels** (digital logic in each pixel)
- 1 to 8 LVDS links **@320 MHz** (Single Data Rate) for data outputs
- Produced in **2023**

New functionalities and improvements:
- Clocks, resets and FSM fully **tripled**
- ↗↗ of **radiation tolerance** of Hamming registers
- ↘↘ of **IR Drop in the matrix**
- Pixel **clusters finding** module



Std PROTIUM flow for MIMOSIS-2:

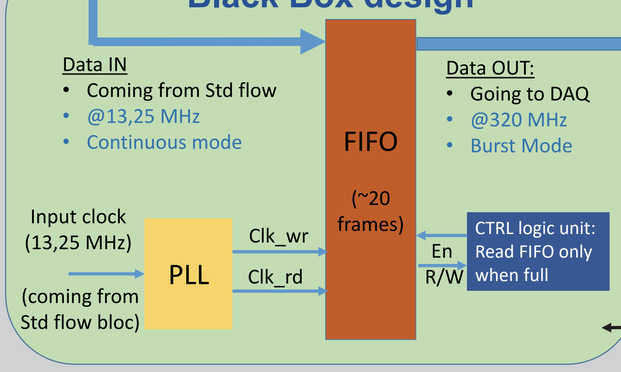
RTL code implemented : all the ASIC digital parts
- Matrix: 1 double column implemented with the column Priority encoder + Digital Part (Memory) of each pixel
- Digital periphery: data-readout, sequencer, slowcontrol, …
- Radiation hardness strategies (Triplication, Hamming) included

Test procedure
- **Digital Pulse** injection in the **pixels** for the matrix readout
- I2C R/W sequences for pattern injection in the digital periphery

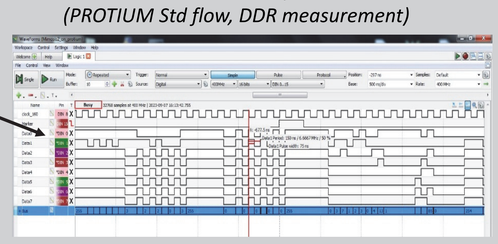
Results :

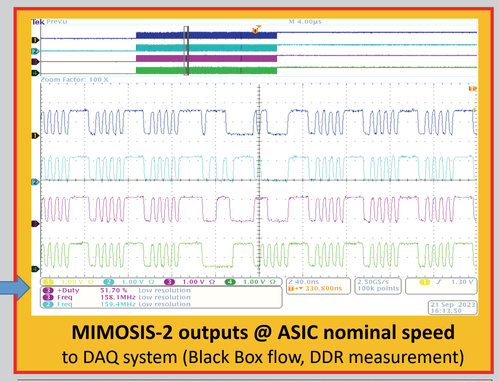
Validation of ASIC data readout and DAQ at reduced frequency (13,25 MHz)

Black Box design

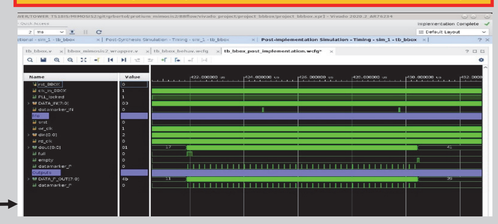


MIMOSIS-2 outputs (PROTIUM Std flow, DDR measurement)





MIMOSIS-2 outputs @ ASIC nominal speed
to DAQ system (Black Box flow, DDR measurement)



Vivado post-implementation simulation of the Black Box

Summary

PROTIUM Std flow:
- Easy integration of complex chip
- Early Development and verification of MIMOSIS-1 & MIMOSIS-2 DAQ systems

Black Box flow enables:
- Increase of the prototyped readout speed at ASIC's nominal frequency

=> 320 MHz vs 13,25 MHz in Std mode for MIMOSIS-2
- Integration of FPGA IPs

Next Steps:
- Development of generic matrix mapped on external memory => use real Physic data
- Development and integration of more complex Black Box (eg: DAQ firmware, RISC V , …)