Contribution ID: **135** Type: **Poster**

MIMOSIS2 validations using Cadence Protium platform and its Black Box flow

Tuesday 3 October 2023 15:00 (20 minutes)

FPGA prototyping enables hardware acceleration for ASIC verification. Cadence Protium, an FPGA based platform, enables ASIC designers to prototype their RTL code in an easy and automatically way. As the RTL codes stay untouched during the process, the Protium provides a reliable model of the ASIC for early developments of DAQ and control systems. Protium advanced Blackbox flow allows in addition using external FPGA IP and running parts of the design at much higher speeds than what can be achieved by standard Protium flow. Its role in the validation of MIMOSIS2, an ASIC developed for CBM experiment, will be presented.

Summary (500 words)

MIMOSIS2 is a full reticule size (31x17 mm²) monolithic pixel sensor prototype developed for the vertex detector of the CBM experiment (FAIR/GSI). It integrates a matrix of over ½ million pixels with Priority Encoders inside each column and a sparse data readout. The slow control, the steering logic and the clocks trees have been fully triplicated to match the radiation hardness requirement of the experiment (100 kGy). The ASIC control is driven by an I2C module and the data transmission is done by up to height 320 MHz LVDS pads. Compared to MIMOSIS1, a new data clusterisation feature have been implemented.

Cadence Protium is a prototyping solution based on hardware environment (mainly Xilinx Ultrascale VU440 FPGA) with dedicated software. Users do not need neither to adapt their RTL code neither to have FPGA knowhow. The Protium compiler generates scripts, which allow designers to perform automatically the FPGA synthesis and the Place and Route steps. The ASIC verification can be done with test bench running inside the Protium environment hardware or by connecting the prototype to external systems.

MIMOSIS2 digital periphery has been successfully prototyped inside a Protium S1. This implementation enables on the one hand the validation of the ASIC. The correction of a bug found in the MIMOSIS1 I2C watchdog has been checked easily and quickly (less than one hour). On the other hand, the Protium facilitates the early and robust development of the upgrades of MIMOSIS1 data acquisition (DAQ) and control systems, months before the chips comes back from foundry.

To enable an automatically implementation of the ASIC inside the Protium FPGA, the Protium compiler adds an extra hardware overlay to the ASIC RTL code. This introduces a timing limitation on the frequency at which the design will run inside the FPGA and communicate with the outside world. For MIMOSIS2, prototyped inside our Protium with a standard flow, the output data rate drops down to around 10 MHz. It is less than the nominal ASIC data output frequency (320 MHz), but user can perform ASIC functional verification at higher speed than using software simulation. It enables also the functional verification of the dedicated DAQ.

To solve this speed issue, we use the Protium BlackBox methodology. This advanced Protium flow allows splitting the Protium FPGA resources in two parts:

• the ASIC RTL code and the Protium overlay, running at lower frequency (10 MHz for MIMOSIS2);

• a BlackBox module which could be any IP (like PLL, ETHERNET or AXI USB module…) or custom designs (like accelerator modules or FPGA firmware of a DAQ), running at high FPGA frequency.

For MIMOSIS2, a dedicated FIFO was developed and used as a BlackBox. Acting as a gearbox between the slow clock domain of the MIMOSIS2 Protium model and the fast clock domain of the data acquisition system, this BlackBox allows us to speed up the data transmission within Protium to the nominal ASIC frequency.

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Session Classification: Tuesday posters session

Track Classification: ASIC