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A novel Front-End for Monolithic Active Pixel Detectors ASICs

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In this work, a low-power low-noise readout circuit for monolithic pixel detectors is presented. The design focuses on robustness and scalability for both reticle sized chips and stitched designs. The front-end includes a differential charge sensitive amplifier, a reset network and a two-stage discriminator. Threshold trimming is performed with a 3-bit DAC. The feedback capacitance is kept at 0.3 fF to boost the gain for low input charges. The gain is 0.4 mV/e-, the noise is 19 e- r.m.s. and the threshold dispersion after equalization is 68 e- r.m.s. Simulations at schematic level and post-layout extraction are presented.

Summary (500 words)

The EP R&D Work Package 1.2 aims to develop monolithic CMOS pixel sensors using the TPSCo 65 nm Image Sensor Process, with a small collection electrode. This process permits increased component density while reducing power consumption with respect to the previous node used by the High Energy Physics community (the 180nm node). Several possible applications of this process (e.g., ALICE inner tracker) impose strict constraints regarding power consumption to ensure the scalability to wafer level dimensions in stitched CMOS sensors. This requires the design to be robust for voltage drop and power supply variations. The low noise for the front end is another constraint in order to amplify the signal deposited in the small depletion region of the sensor.

This front-end includes a Charge Sensitive Amplifier (CSA). The CSA is based on a differential folded cascode amplifier (nominal gain of 50 dB), which allows for external baseline adjustment (nominal baseline at 300 mV). An nMOS transistor in weak inversion provides the feedback to discharge the feedback capacitance. This transistor is biased via a replica circuit, which keeps the baseline stable in case of temperature variations. The discriminator comprises a two-stage CMOS OTA that ensures speed and a high gain (nominal 55 dB). A 3-bit DAC is included to compensate for the pixel-to-pixel threshold variation.

These types of front-ends have two-time constants. The rise time constant depends on the transconductance of the input transistor, the feedback capacitance and the sum of the input, output, and feedback capacitance. The feedback capacitance, when the pulse is above ˜25mV, is discharged with a constant current, which leads to a linear time over threshold measurement. One of the particularities of this process is the small input capacitance of the sensor (˜ 1 fF). The strict requirement for lower consumption (10 nA CSA biasing current) reduces the transconductance of the input transistor, affecting the rise time. To keep the low power consumption and the benefits of the small input capacitance, the feedback capacitance has a nominal value of 0.36 fF. This allows for amplification of small input charges, working on a range from 100 e- to 2000 e- with a gain of 0.4 mV/e-, fast rise time (˜ 1 us) and low noise (19 e- r.m.s). Schematic simulations prove a linear ToT up to 1750 e- and a systematic ToA dispersion of 800 ns. The 3-bit DAC for threshold equalization reduces the minimum detectable charge from ˜165 e- to ˜68 e-. Corner simulations confirm the robustness of this amplifier against bias and temperature variations.

Simulations of this design demonstrate how this type of front-end, based on a transconductance amplifier, can be used in applications that require a low power consumption and where the focus is on detecting and amplifying Minimum Ionizing Particle (MIP) signals.

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