Contribution ID: **90** Type: **Poster**

28 nm front-end channels for the readout of pixel sensors in future high-rate applications

Tuesday 3 October 2023 15:00 (20 minutes)

This work is concerned with the design and the characterization of front-end channels, developed in a 28 nm CMOS technology, conceived for the readout of pixel sensors in future, high-rate applications at the next generation of large particle accelerators.
Two front-end architectures are discussed. In the first one, an in-pixel flash ADC is exploited for the digitization of the signal, whereas the second one features a Time-over-Threshold (ToT) conversion. A prototype including the ADC-based front-end has been submitted and the characterization of the chip is discussed in the conference paper. Simulation results relevant to the ToT-based architecture are reported.

Summary (500 words)

State-of-the-art readout channels for pixel detectors in high energy physics (HEP) experiments are being developed, in a 65 nm CMOS technology, by the RD53 collaboration, established at CERN in 2013. The RD53 efforts led to the submission of three families of readout chips optimized for the high luminosity (HL) upgrades of the ATLAS and CMS experiments. The RD53 chips have been extensively characterized, and proved to be able to withstand total ionizing doses (TIDs) up to 1 Grad(SiO2), while preserving the main performance parameters.
The HEP designers'community is now generally migrating to the 28 nm process for the development of new circuits. The 28 nm node is the major commercial successor of the 65 nm one, bringing along some interesting features. In particular, a number of test campaigns with TIDs in the Grad regime did show that properly sized 28 nm transistors can be operated with limited performance losses. Moreover, the scaling-down process intrinsically improves speed and density of digital circuits, allowing the designers to develop very compact pixel cells and fast readout logic and I/O circuits. This makes the 28 nm technology an ideal candidate for the design of next generation, high data rate readout chips to be operated in extremely harsh radiation environments.
This work discusses the design of two front-end circuits being developed in the framework of the INFN Falaphel project, aiming at the integration of silicon photonics modulators with high speed, rad-hard electronics in a 28 nm CMOS technology. The Falaphel project was conceived having in mind the challenging requirements set by the tracker of the hadronic Future Circular Collider. Nonetheless, the outcome of the project can be of interest for a potential replacement of the innermost pixel layers of the HL-LHC experiments after 2030.
The two architectures described in this work implement different digitization techniques. The first one relies on an in-pixel flash ADC, whereas the second one leverages the Time-over-Threshold method. Both the front-end channels include a charge sensitive amplifier (CSA) with detector leakage compensation. The CSA feedback includes two independent loops. A fast one, featuring a MOS device operated as a constant current source, provides a linear discharge of the CSA feedback capacitance. A slow loop was instead devised to compensate for the sensor leakage current. In the flash ADC-based channel, a set of three autozeroed comparators are connected to the preamplifier, providing a 2-bit resolution analog-to-digital conversion. On the other hand, in the ToT-based processor, the comparator is DC coupled to the CSA, and a digital counter is activated by the signal generated at the discriminator output.
A prototype including a matrix of 8x4 ADC-based channels has been submitted and the characterization of

the chip will be discussed in the conference paper. Simulation results relevant to the ToT-based architecture, whose submission is foreseen for October 2023, will be reported.

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Session Classification: Tuesday posters session

Track Classification: ASIC