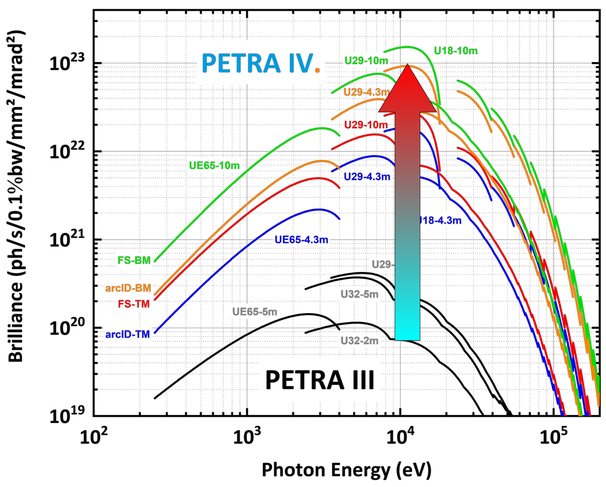
Development of the Continuous Readout Digitising Imager Array Detector.

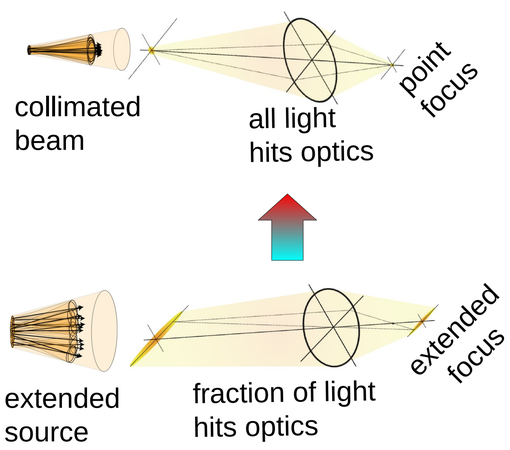
A. Marras[a,b], A. Klujev[a,b], S. Lange[a,b], T. Laurus[a,b], D. Pennicard[a,b], U. Trunk[a,b], C.B. Wunderer[a,b], H. Krueger[c] and H. Graafsma[a,b,d]

a) Deutsches Elektronen-Synchrotron (DESY), Hamburg, Germany
b) Center for Free Electron Laser Science (CFEL), Hamburg, Germany
c) University of Bonn, Bonn, Germany
d) Mid Sweden University, Sundsvall, Sweden

3rd → 4th generation Synchrotron Rings

Example: PETRA III → PETRA IV upgrade at DESY



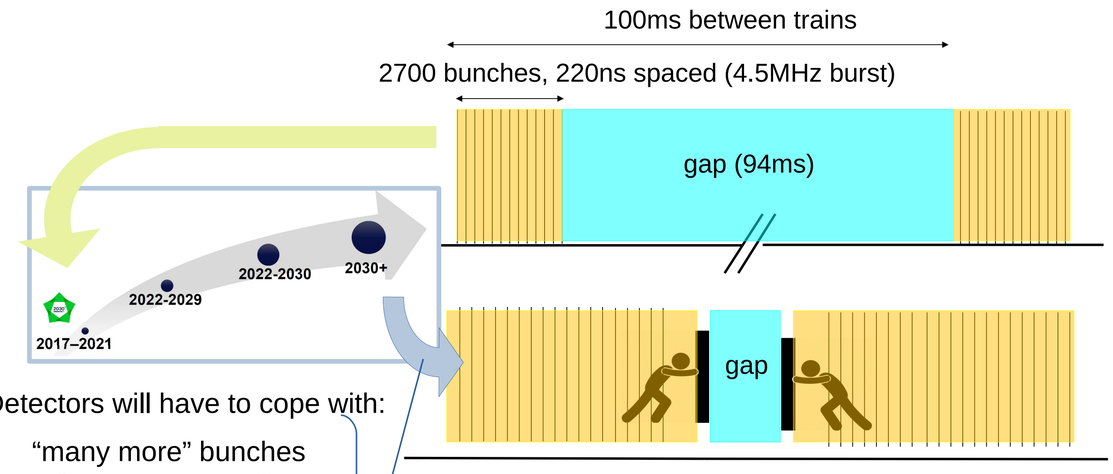


Synchrotron Rings are being upgraded to the diffraction-limited regime
Source technological improvements (Multi-Bend Achromat, on-axis injection) produce a more collimated beam, that can be better focused on the optics

→ more ph/s on the detector
→ Frame rate requirements in some experiments increase from kHz to >100 kHz

High-rep-rate FELs considering transition to long-train / CW operation

Example: EuXFEL roadmap



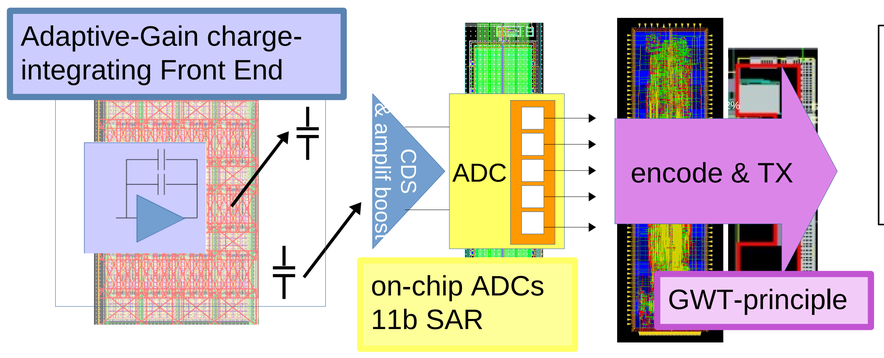
Detectors will have to cope with:

- "many more" bunches at a "slightly reduced" rate
- "much smaller" gaps between bunch trains
- users ask for smaller pixels

Traditional approach to detectors for high-rep FELs (images stored on internal memory, read during gaps) is no longer optimal the choice
→ continuous readout in excess of 100kHz needed

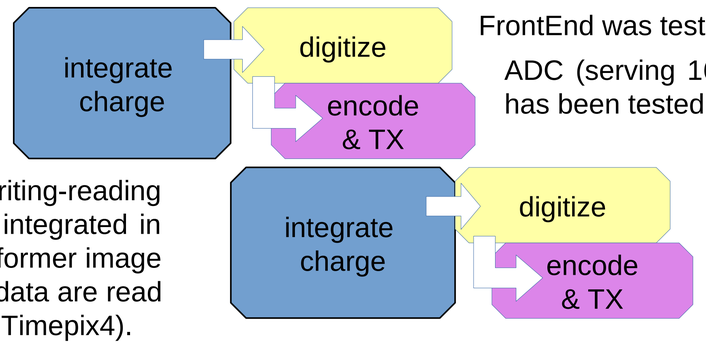
common need for:
– continuous readout
– > 100kHz frame rate

COntinuous Readout Digitising Imager Array (CoRDIA)



our objectives

- > 100 kframe/s (testing now at 150k), continuous readout
- 110 µm pixel size
- 1-photon sensitive at 12 keV
- significant dynamic range (now 2k ph/pix/img, aiming at 10k)
- compatible with Hi-Z & internal-amplification sensors



single circuit stages have been validated for continuous operation at the target frame rate:

FrontEnd was tested at: $>150\ kframe/s$

ADC (serving 16 Front Ends) has been tested @2.5MS/s: $\frac{2.5\ MS/s}{16\ FE} > 150\ kframe/s$

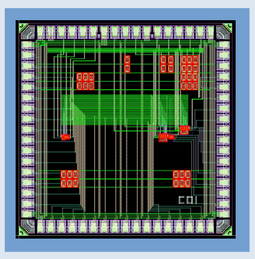
GWT was verified by NIKHEF at 5.12Gb/s and above. In our design this is enough stream out 2k pixels (each pixel is digitized to a number of less than 2 Bytes, and transmitted with 66/64b encoding).

$$\frac{5.12\ Gb/s}{16\ bits * \ 2k\ pixels\ * 66/64} > 150\ kframe/s$$

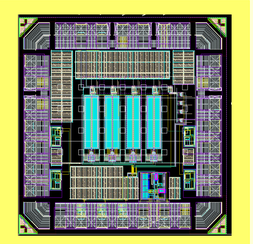
To achieve the desired frame rate, the detector adopts a Continuous Writing-reading scheme based on a 2-stage-pipeline structure. While incoming photons are integrated in an Adaptive Gain amplification stage (adapted from the AGIPD detector), the former image is digitized (through 11bit Successive Approximation Register ADCs) and the data are read out (using the Gigabit Wireline Transmitter principle developed by NIKHEF for Timepix4).

Prototypes

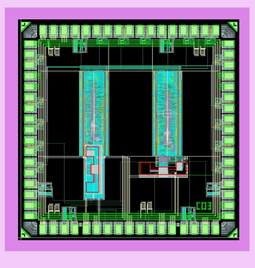
Several prototypes were designed in TSMC65nm technology, and manufactured by means of Multi-Project Wafer (MPW) runs, to test and validate circuit blocks and circuital chains.



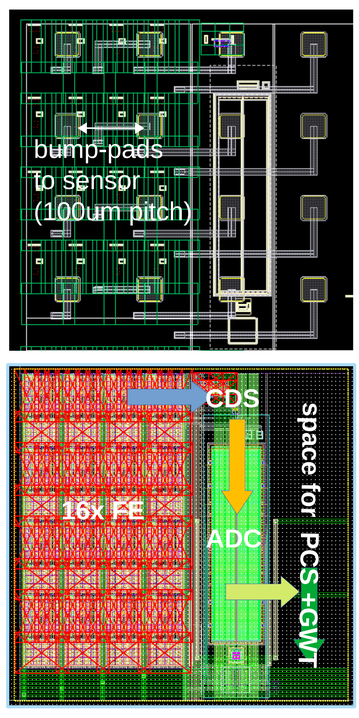
2021: CoRDIA_01 prototype.
Designed, manufactured, tested.
Used to validate at the expected frame rate the Adaptive Gain circuit, CDS block, the circuit to alternate between two readout sub-chains (to achieve continuous Write-Reading)

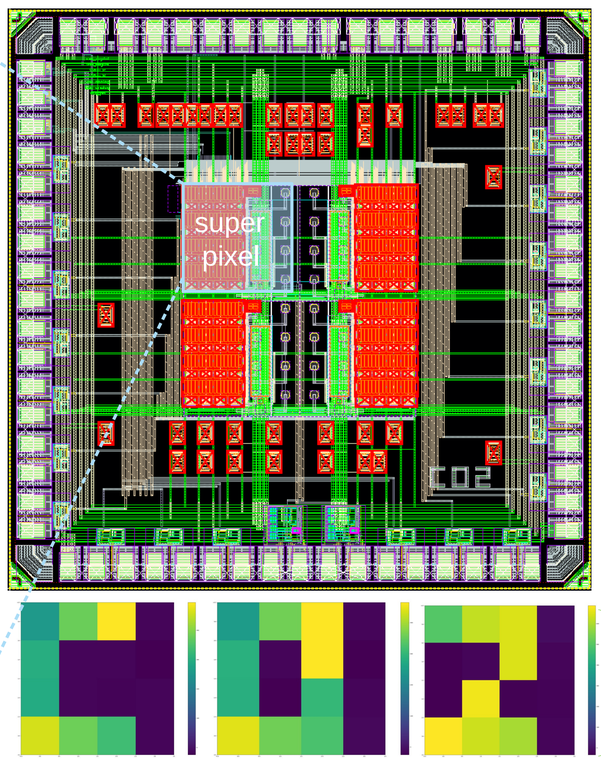


2021: HSI_ADC01 prototype.
Designed, manufactured, tested.
Used to to evaluate ADC variants based on SAR architecture (exploring redundancy and switching options), and confirm the image sampling capability at the expected frame rate



2023: CoRDIA_03 prototype.
Designed. Manufacturing in progress.
Test expected next year.
Will be used to explore/validate variants of the PCS+GWT circuits, optimized to the CoRDIA data flow and overall layout constraits.





2022: CoRDIA_02 prototype.
Designed, manufactured.
Test in progress.
It includes a circuital chain of multiple front-ends coupled to an analog-to-digital converter, and the silicon area reserved for transmission drivers.
The circuits are arranged in a repeatable "superpixel" structure.
The goal of the prototype is to verify the signal-processing of images in a pipeline fashion (so that one image is acquired at the same time the former one is digitized and streamed out).
The bump-bond pads interfacing to the sensor are redistributed to a uniform 2D array to facilitate bonding.
Calibration circuits, able to inject charge in in an arbitrary pattern of pixels, were used verify basic functionality (as shown in the images on the left)

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