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A High Time Resolution Monolithic Active Pixel Sensor with Node-Based, Data Driven and Parallel Readout for Vertex Detector in particle physics Experiments

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We present the design of a high-time resolution MAPS sensor prototype MIC6_V1 based on a 55nm Quad-well CMOS Image Sensor process for the high energy physics experiment vertex detector application. In order to achieve high-spatial resolution, fast readout, and low power consumption, MIC6_V1 has implemented a new node-based, data-driven parallel readout architecture. The integration time is 5us, and by sharing VCO in the pixel group, the hit arrival time resolution can reach 10ns. The pixel size of MIC6_V1 is 23.6μm × 20μm. The pixel matrix is 64 rows by 64 columns, and the size of MIC6_V1 is 2.8mm × 2.8mm.

Summary (500 words)

The vertex detector in high energy physics experiment requires high spatial resolution, fast readout, and low power consumption. The Monolithic Active Pixel Sensor (MAPS) is the most promising candidate technology to satisfy all those requirements. We have developed the MAPS sensor MIC6_V1 in a 55 nm quad-well CMOS image sensor process with a node-based data-driven readout scheme.

MIC6_V1 contains a pixel matrix of 64 rows by 64 columns with a pixel size of 23.6 μm 20 μm. Each pixel contains a sensing diode, an amplification, a discriminator, and a hit storage register connected to a node-based sparse readout circuitry. Every double-column of pixels share a readout circuit, and 42 pixels form a super pixel group. The 8 pixels in each super pixel share a VCO for hit arrival time measurement. The VCO oscillates only when the super pixel group is hit to reduce power consumption. The oscillation frequency of VCO can be configured between 100 ˜ 200 MHz. Each super pixel also includes a node of sparse readout logic circuit, and the hit information will be asynchronously transmitted to the bottom of the double-column through the readout nodes. Readout nodes transmit data based on request-acknowledge handshake protocol. When a super pixel group is hit, 22 bit data will be generated, including 4-bit super pixel group address, 10-bit time counter and 8-bit hit shape.

In the bottom of MIC6_V1, a periphery readout module also based on asynchronous readout node has been implemented to readout 22-bit data and 5-bit column address from each double-column. Then, a synchronizer module is connected to the peripheral readout module, which is responsible for processing handshake, data synchronization, data bit-width conversion, and finally outputting the data. In addition, an asynchronous handshake multiplexer module is implemented, through which any double-column can be tested independently.

The test system is being developed and consists of a test board, a Kinex-7 FPGA and control software. The test firmware and software are based on IPbus. The 1 Gbps Ethernet interface, IPbus master, and IPbus slavers are implemented in the FPGA. The test commands from the control software on PC are received by the 1 Gbps TCP/IP module and then transmitted to IPbus master. The commands from the IPbus master are sent to one of the IPbus slavers. The current DAC, voltage DAC and the MIC6_V1 are configured by the respective IPbus slaver. The data flow of the MIC6_V1 is opposite to the flow of test command. The output data of MIC6_V1 are transmitted to PC through ipbus slave, ipbus master and Ethernet interfaces in turn. The test results of MIC6_V1 will be presented in the workshop.

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