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The CMOS Pseudo-Thyristor: A Zero-Static Current Circuit for Pixelized Detector Front-End Stage

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A novel ultra-low-power front-end discriminator circuit for pixelized detectors, named pseudo-thyristor, is described. It is based on a positive feedback topology using regular CMOS transistors with zero static current, rather than constantly drawing current in typical discriminators. When a small charge is injected at the input, the circuit flips rapidly due to the positive feedback and output a logic transition for further digitization. Simulation shows that in 65 nm process, it is capable of detecting at a threshold of 5 fC while maintain the average power consumption below 10 micro-Watts when the hit occupancy is <10% for 40MHz operation.

Summary (500 words)

In contemporary high energy physics detectors, pixelized detectors such as silicon detectors or Low-Gain Avalanche Detectors (LGADs) are widely used for tracking, timing or calorimeters. As a large number of detector elements are used, very low power consumption of the front-end circuits required. In some applications, power consumption of as low as 10 micro-Watts per channel for the front-end is desired. In typical architectures today, the front-end circuits consist of pre-amplifiers and discriminators, each consuming about 1 milli-Watts implemented in 65-180 nm CMOS processes, which is a factor of 100 higher than what is desired in the future. To reduce the power consumption by up to two orders of magnitude, new topologies of the front end design are required. The Pseudo-Thyristor proposed here is a novel CMOS circuit with zero static current for LGAD-like frontend electronics with the potential to have ultra-low power consumption.

The circuit is a positive feedback topology (which is rarely used in analog frontend circuits) using regular PMOS and NMOS field-effect transistors (FET's). The core of the circuit consists of a pair of PMOS and NMOS FET's with their drain and gate terminals cross connected to form a positive feedback loop. When a small amount of electronic charges is injected into the NMOS gate, both the NMOS and PMOS FET's are turned from OFF to ON state similar to a thyristor, except that in both ON and OFF states, the static current of the circuit is almost zero (with small leakage currents in deep nanometer fabrication processes) as in most digital CMOS circuits. The proposed thyristor is capable of converting a small input charge into a logic level transition and afterward can be reset from ON to OFF state with a set of FET's.

In the typical front-end circuits being used today for HEP, both the preamplifiers and discriminators operate with a static current so that the transistors are in high conductivity region to follow the input pulse at high speed. The topologies used in amplifiers usually employs negative feedback to improve bandwidth and linearity.

However, in pixelized detectors, full waveforms are rarely needed. In many cases, single-bit hits indicating the coordinates of the passing points of charged particles in a tracking detector are sufficient. Beyond that, one may digitize the arrival times of the particle hits and sometimes digitize the pulse widths for time walk correction. In these situations, the requirement of the front-end circuit is nothing more than providing a logic transition. This requirement can be fulfilled using very low power circuits consuming zero static current. Also, since the detector elements produce only one type of charges (negative charges), symmetric topologies in the front-end circuits are not necessary, which further simplifies the circuits and results in lower power consumption.

While the circuit can be at least utilized for 1-bit hit detection in tracking pixel detectors, it is also feasible

to apply it for timing walk correction when the 4D detection is demanded, although further simulation and testing are needed.

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