# Test Result of the New ASD2 Chips for Phase-II Upgrade of the ATLAS MDT Chambers at HL-LHC

Katrin Penski
on behalf of the ATLAS Muon Spectrometer System

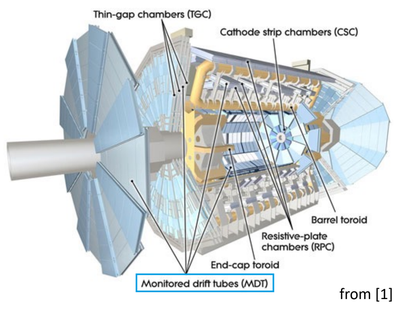
LMU LUDWIG-MAXIMILIANS-UNIVERSITÄT MÜNCHEN

ATLAS EXPERIMENT

**Motivation:** upgrade of the front-end electronics for ATLAS for High Luminosity LHC (HL-LHC)
**Aim:** providing test environment to find the best 50.000 ASD chips for ATLAS

**Challenges:**
- characterize performance of chip
- set and verify testing parameters and cut intervals for production testing
- reject non-working chips and achieve high uniformity among channels

## ATLAS Muon Spectrometer

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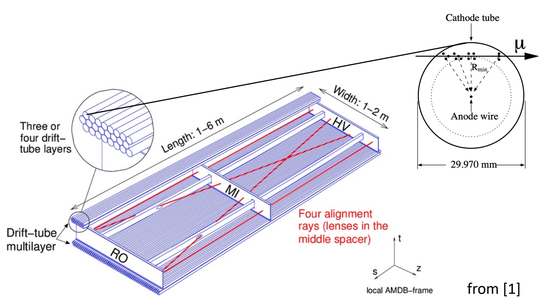



from [1]

### HL-LHC Upgrade (Phase-II)
- up to $\mathcal{L} = 7.5 \cdot 10^{34}\ cm^{-2} s^{-1}$
- requirement for 1.150 MDT chambers: efficient trigger and readout system

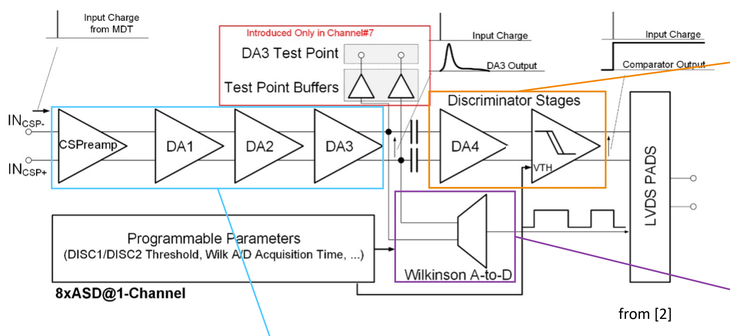
→ new ASD2 chips (about 50.000)

### Drift Tubes
- gas mixture: Ar:$CO_2$ (93:7 % vol)
- average resolution 3 tube-multilayer: ~ 40 µm

→ eight tubes are served by one ASD

## ASD2 Chip

- Amplifier/Shaper/Discriminator chip using 130 nm GF CMOS technology




from [2]

### Discriminator
- threshold for signal

→ set parameters such as threshold and hysteresis

### Wilkinson ADC
- time-slew correction
- voltage time conversion

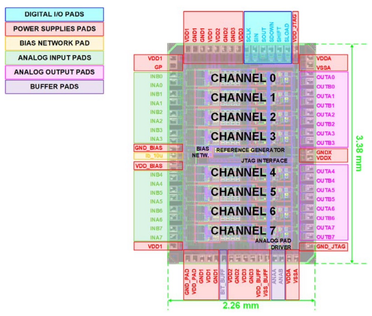
→ set programmable parameter such as deadtime, rundown current (rdc) or integration gate

### Analog Part
- charge-sensitive pre-amplifier and shaping

## ASD Chip Characterization and Functionality

### Testing Procedure
- testing 100 pre-production chips with the **prototype tester board** →
- investigate influence of programmable parameters

### Basic Health Test

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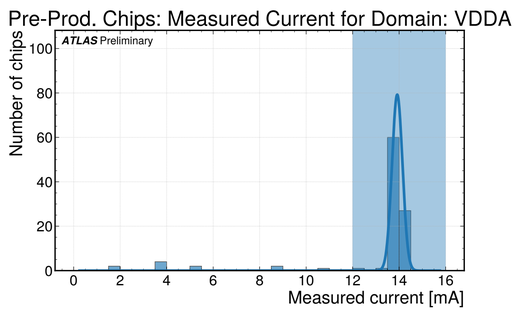
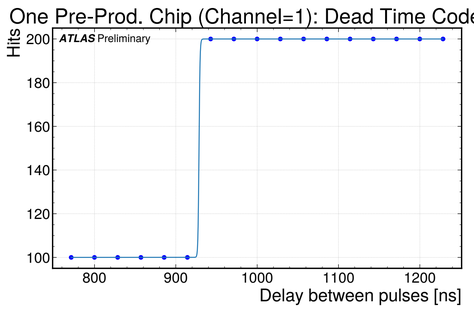
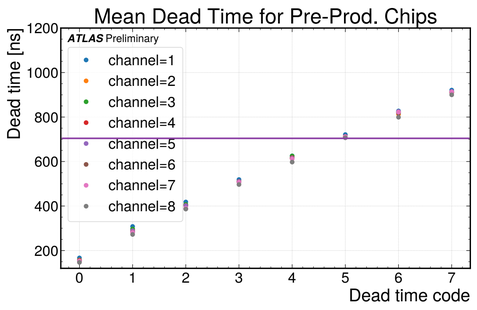



- drawn current for power domains VDD1, VDD2, VDD3 and VDDA
- rejection of chips drawing abnormal currents (accepted: 12 mA <$I_{VDDA}$<16mA)

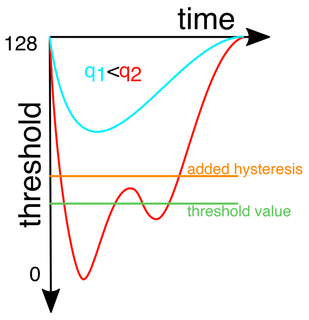
### Dead Time Measurement

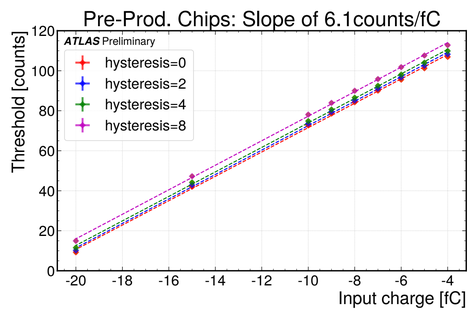



- single muon causes multiple threshold crossings → solved by dead time
- MDTs have drift time of about 700 ns → dead time code 6 or 7 needed

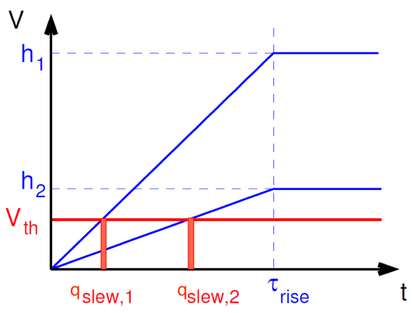
### Threshold Measurement




- set hysteresis avoids multiple threshold crossing due to noise
- detection of small charges → threshold value above 115 counts (-4 fC)

### Pulse Width Measurement

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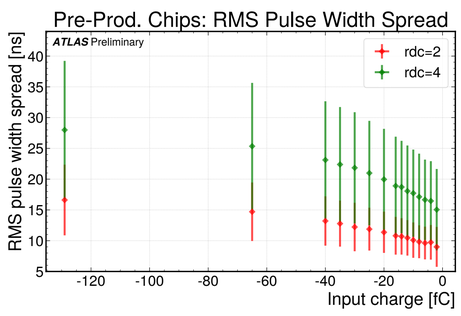


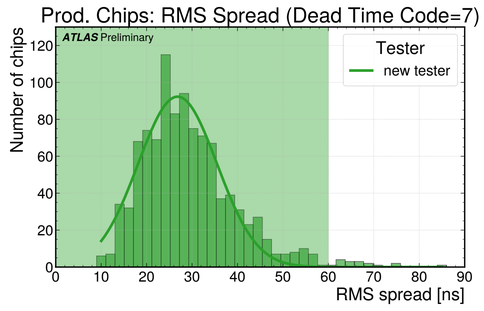

- MDT Time-Slewing Correction: encoding charge by pulse width
- RMS spread doubles for rdc=4 → rdc=2 preferable

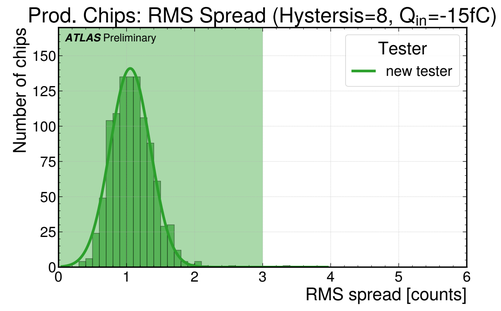
## Final Test Parameters - Categorization

### Testing Procedure
- testing **1175 production ASD2 chips** (test results show no difference to pre-production chips)
- usage of **new tester** (more rigid design for company testing, test results show no practical difference to old tester)

### Categorization
- **C:** non-working chips, e.g., abnormal currents or dead channels in S-curve scan
- **B:** working chips, but outside of accepted interval
- **A:** working chips and inside of accepted interval for homogenous chip performance
- **aim:** 70 % of chips in category A (ratio of needed ASD chips for ATLAS)

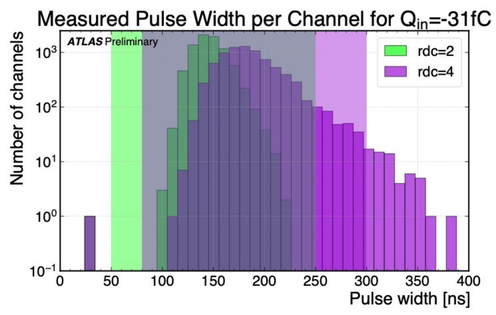
### Dead Time and Threshold Test

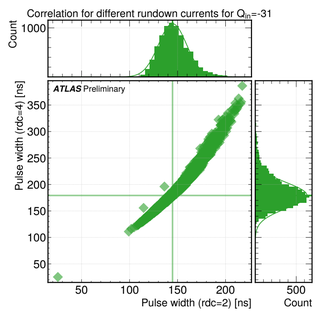



- cat. A: e.g. RMS cuts for dead time (< 60 ns) and threshold (< 3 counts), else cat. B

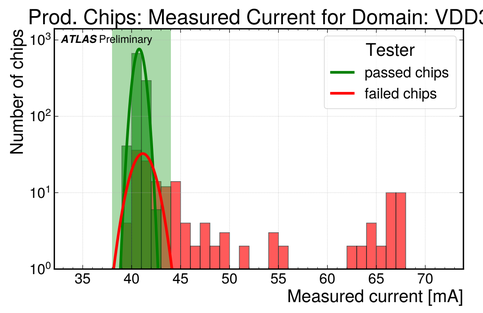
### Pulse Width Measurement

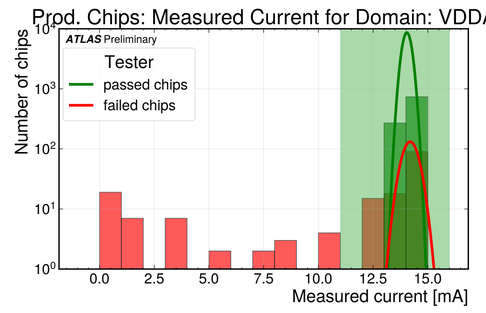



- cat. A: e.g. distribution cuts for rdc=2: [50, 250] ns and rdc=4: [80, 300] ns, else cat. B

### Basic Health Cut Verification




- verification: almost all chips that fail in later tests already fail the basic health test
- cat. A: e.g. 38 mA < $I_{VDD3}$ < 44 mA and 12 mA < $I_{VDDA}$ < 16 mA

### Conclusion
- successful investigation of programmable parameters on chip's performance
- optimized cut intervals for categorization to provide best chips to ATLAS
- **Finally: 71 % in category A, 15 % in B and 14 % in C**
- results were used for production testing of 70.000 ASD chips at company

[1]: The ATLAS Collaboration, 2008 The ATLAS Experiment at the CERN Large Hardon Collider, https://iopscience.iop.org/article/10.1088/1748-0221/3/08/S08003/pdf
[2]: S. Abovyan et al., MDT ASD2 User Manual, Version 8 – Draft – 03-Aug-2021, tech. rep.
[3]: Zhe Yang, Cosmic Ray Test with sMDT Prototype Chamber using modified miniDAQ system
https://indico.cern.ch/event/821237/contributions/3433359/attachments/1852150/3040996/sMDT-talk-Zhe-0528.pdf

Fakultät für Physik, Ludwig-Maximilians-Universität München
Particle Physics, LS Schaile
contacts: https://www.etp.physik.uni-muenchen.de/members/index.html

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