TWEPP 2023 Topical Workshop on Electronics for Particle Physics



Contribution ID: 41

Type: Poster

Test Result of the New ASD2 Chips for Phase-II Upgrade of the ATLAS MDT Chambers at HL-LHC

Tuesday 3 October 2023 15:00 (20 minutes)

For the

-II upgrade of the ATLAS Muon Spectrometer to the High Luminosity LHC (HL-LHC), a new first-level muon track trigger is needed to make use of the high momentum resolution of the Monitored Drift Tube (MDT). The current front-end electronics of the MDT chambers do not meet these conditions, they have to be replaced. Therefore, a new ASD2 ASIC chip has been developed. Finally, 50000 ASD2 chips are needed for the ATLAS experiment. The development of the final testing procedure and the reliability of a first batch ASD2 chips will be presented.

Summary (500 words)

A new first-level muon track trigger is installed for the -II upgrade of the ATLAS Muon

Spectrometer to the High Luminosity LHC (HL-LHC), which will make use of the high momentum resolution of the Monitored Drift Tube (MDT) chambers. Due to the long drift times in the MDT, a triggerless readout is needed. Since the current front-end electronics of the MDT chambers do not meet these conditions, they have to be replaced. For this purpose, a new ASD2 ASIC chip in 130 nm Global Foundries CMOS technology has been developed. For the ATLAS experiment, 80000 chips are produced and tested before integration, since in the end 50000 well-performing chips are needed. The overall goal of the ASD2 chip test procedure presented is to find optimized parameters and cut values that characterize the performance of the chip and are used for production testing in the company. Phase

First, the influence of the different programmable parameters on the chip's behaviour is investigated. For this purpose, 100 pre-production chips are tested with tester board prototype and analysed with respect to four measurement criteria: Basic Health, Threshold, Dead Time and Pulse Width. Cuts are introduced to reject non-functioning chips and achieve high uniformity among the channels and chips. In a second step, about 100 pre-production and production chips are compared. Both ASD2 chip types show no practical difference. In both cases, about 80 % of the chips work considering the introduced selection criteria and cut intervals.

For the production testing a new QAQC tester board was designed, and its performance is examined using the 100 production chips. The results are compared with those of the tester prototype. Despite of an offset in some values due to a larger bias current in the new tester, there is no difference of practical relevance.

Finally, in order to define final testing parameters and cut intervals for the production testing at the company

1175 production ASD2 chips are tested with the new tester. The yield of

well-performing chips is about 86%, with a homogeneous distribution for all channels and chips regarding all four measurement criteria. For finer differentiation, the cut criteria are further extended, and the chips are divided into three categories, with 14 % of the chips in C (non-working chips), 16 % in B (working chips outside some cut intervals) and 70 % in A (working chips inside all intervals). These results are used as input for the automized production chip testing which took place in spring 2023 using 80000 chips.

Author: IENGO, Paolo (CERN)

Presenter: PENSKI, Katrin Elisabeth (Ludwig Maximilians Universitat (DE)) **Session Classification:** Tuesday posters session

Track Classification: ASIC