Data transmission architecture of the ALICE ITS3 stitched sensor prototype MOSAIX

Piotr Dorosz Piotr.Dorosz@cern.ch
on behalf of the MOSAIX design team and ALICE collaboration

CONFERENCE TWEPP 2023 , Geremeas, Italy, 5.10.2023

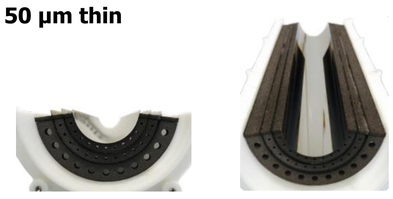
DESIGN CHALLENGES

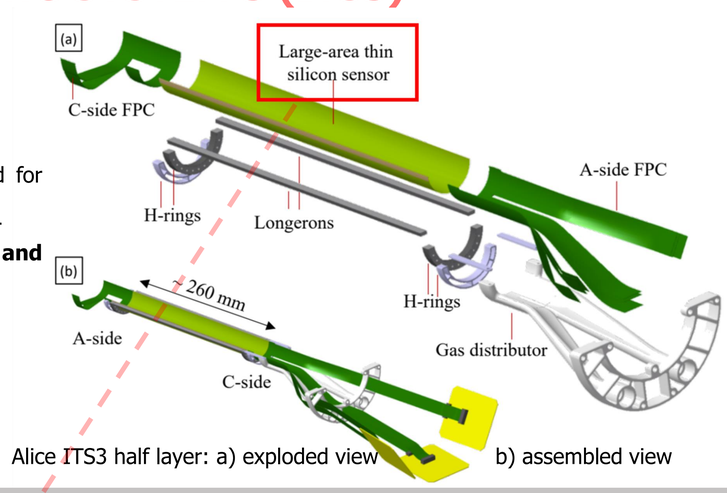
- **How to transmit data across a 26 cm long chip?**
  - 144 data sources evenly distributed along the 26 cm length
  - All data has to be transmitted to a single side of the chip (endcap)
  - Data from each source has different unknown phase (distance from the data source is changing) and accumulated jitter
- **How to transfer 30.72 Gb/s off-chip?**
  - Data needs to be grouped inside the endcap
  - Data needs encoding to reduce the transmission errors

ALICE INNER TRACKING SYSTEM 3 (ITS3)

Large-area thin silicon sensor is a **wafer size silicon sensor** that is bent to the half-ring shape

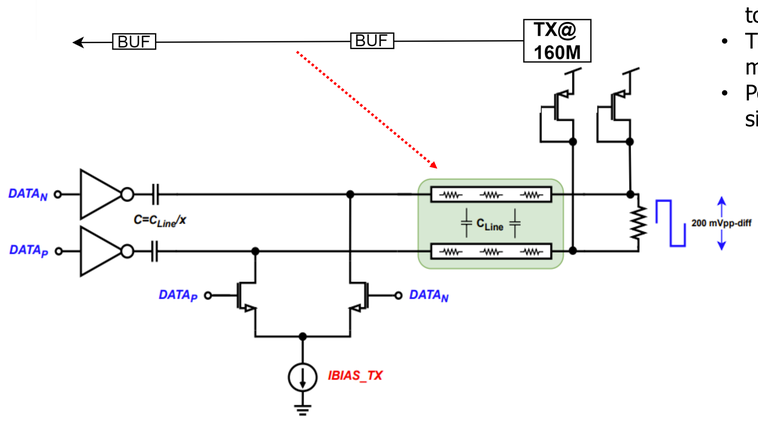
- A-side Flexible Printed Circuit (FPC) is used for data and powering transmission
- C-side FPC is used for powering of the sensor
- **The silicon sensor is over 260 mm long and 50 µm thin**





Alice ITS3 half layer: a) exploded view b) assembled view

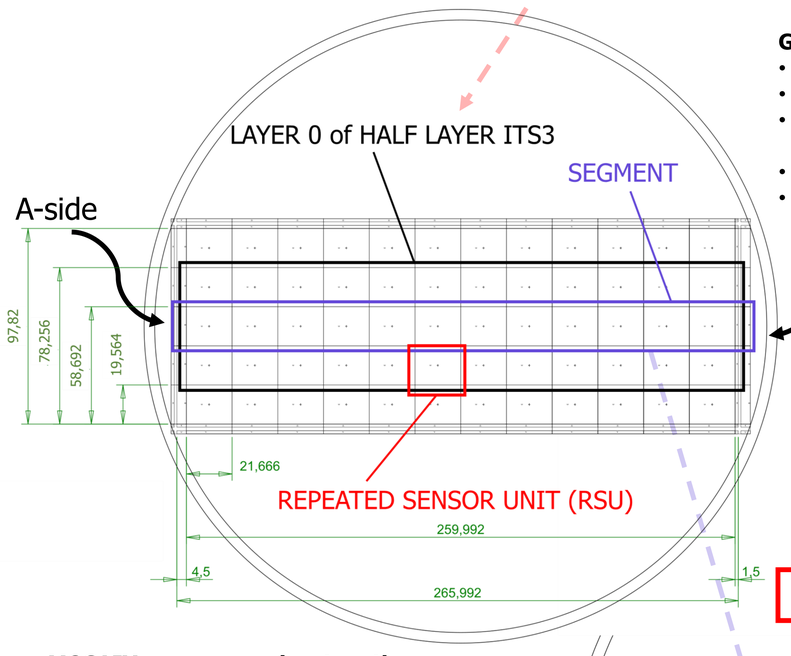
ON-CHIP TRANSMISSION LINK

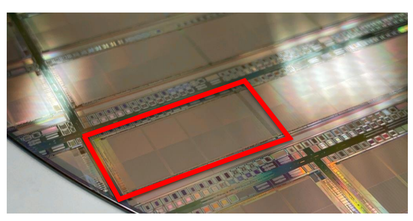


SIMPLIFIED SCHEMATIC OF THE TRANSMITTER AND ONE SECTION OF THE LINK

- Full-custom differential transmission link
- Voltage swing over the line is limited to 200 mV to reduce power consumption
- The length of transmission links varies from <1 mm to 26 cm (with a 11 mm pitch)
- Performance of the link according to schematic simulations:
  - Due to signal attenuation the link needs signal rebuffering by a receiver-transmitter module (BUF) every 3 Tiles (~11 mm)
  - The bandwidth of a 11 mm section is 200 MHz
  - The inter symbol interference jitter with a pseudo-random sequence is 12.5 ps peak-to-peak per section
  - The longest link consists of 24 segments:
    - Accumulated jitter of 5% of the eye opening @ 160 Mb/s
    - Propagation delay of the metal lines 2.5 ns in typical corner

MOSAIX – MONOLITHIC STITCHED PARTICLE DETECTOR



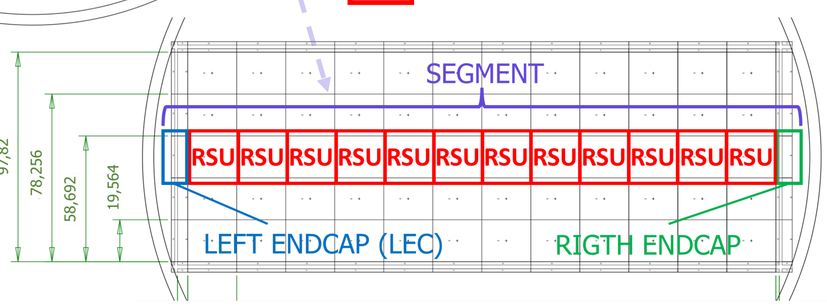


Repeated (Stitched) Sensor Unit

General parameters:
- 65 nm imaging technology
- Layers of ITS3 consist of segments
- Length and width of each segment: **266 mm x 19.6 mm**
- Thickness **≤ 50 µm**
- Pixel pitch 20.8 x 22.8 µm² (10.7 million pixels per segment)

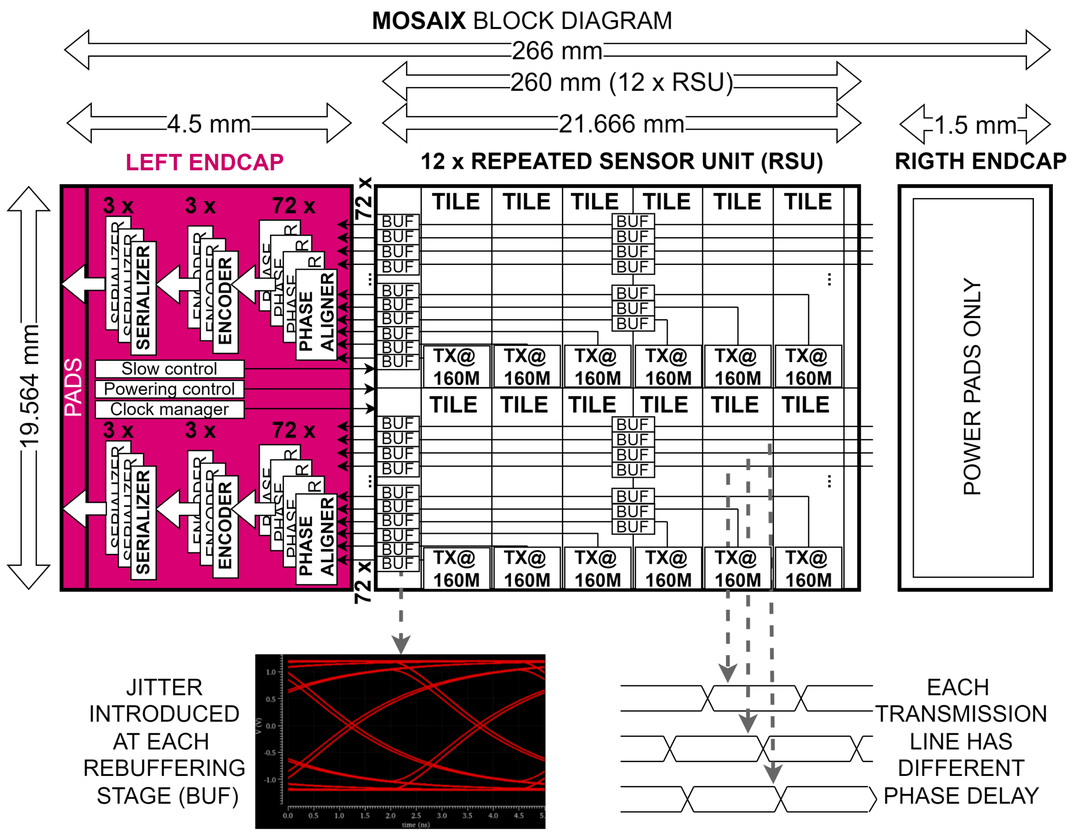
MOSAIX corresponds to the segment
- Full MOSAIX chip consists of:
  - **12** identical **repeated sensor units** (RSU)
  - **left endcap** (LEC) – collecting data from all RSUs for off-chip transmission
  - Right endcap (REC) – used only for powering

Detection characteristics:
- Binary readout
- Parametrizable strobe length



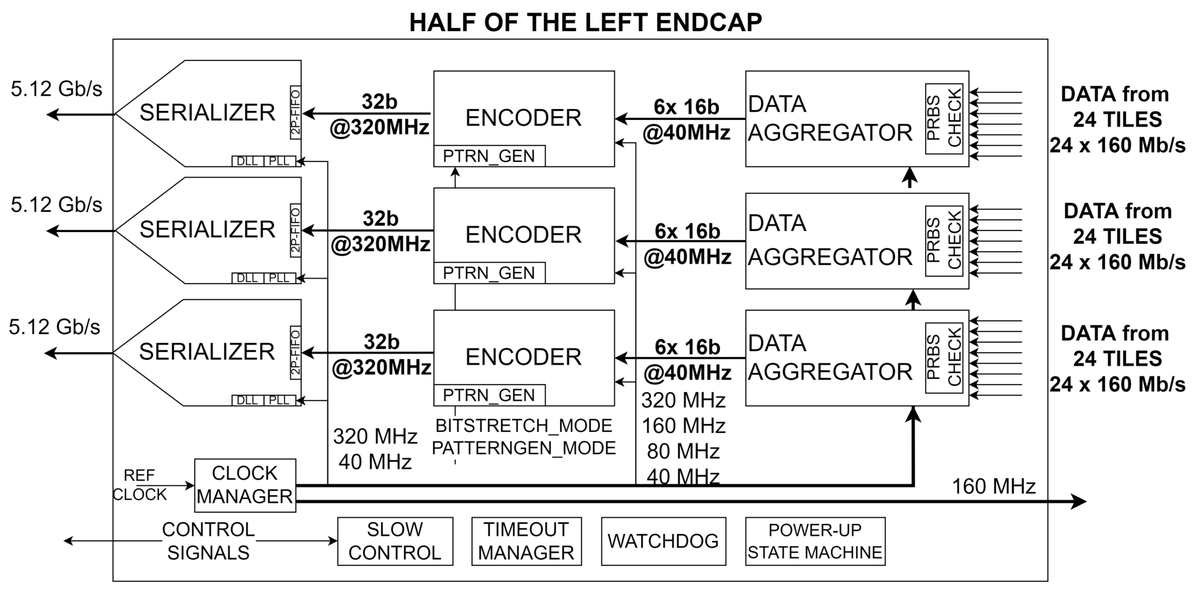
LEC is the only data interface between MOSAIX and off-chip domain

DATA FLOW – FROM TILES TO THE LEFT ENDCAP



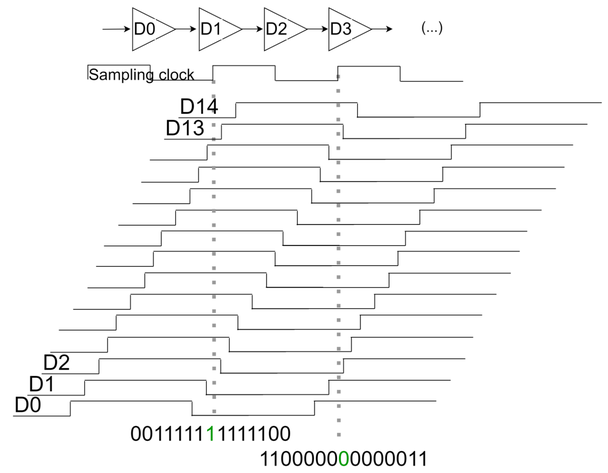
- RSU is divided into 12 TILES
- Each **TILE can be considered an independent pixel detector** with its own pixel array (460 × 162 pixels), biasing and data transmitter
- Tiles are located along the 26 cm length of the MOSAIX (the distance from the LEC varies)
- Each tile stores data from the pixel array in an internal memory, then serializes it at **160 Mb/s** rate and transmits over a dedicated on-chip link to the left endcap
- The number of transmission on-chip links is corresponding to the number of tiles (144 for the total MOSAIX design)
- One-to-one direct connection between tile and left endcap

SENDING DATA OFF-CHIP



How data is processed in the left endcap?
- Data arriving from the tiles is phase aligned first in data aggregator blocks (each link has a dedicated phase aligner)
- Afterwards, it is encoded in the lpGBTlink-TX (Encoder)
- The last stage is to seriallize the data and send it off-chip with a 5.12 Gb/s data rate
- After encoding and serializing the total data rate of the left endcap is 30.72 Gb/s

Why phase alignment?
- The length of transmission links varies from <1 mm to 26 cm (with a 11 mm pitch)
- Bit stream on each link arrives to the left endcap with a different phase because of various propagation delays
- Data needs to be sampled in the middle of the eye opening to prevent errors occuring

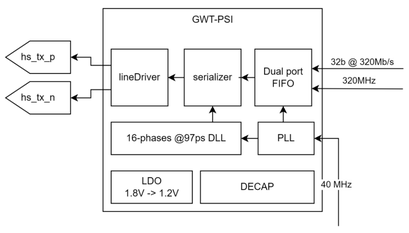


Extracting information about the phase from a delay line

Finding the correct phase
- Data from transmission link enters into a delay line
- The delay line generates a vector of 15 phases per every sampling clock cycle
- The digital logic around the delay line scans through this vector to find where the data is changing value (edges of data bit)
- Afterwards, the phase aligner locks itself to a phase which is in-between those edges (optimal phase in the middle of an eye opening)
- If the digital logic reports the same optimal phase for a number of data bits then the phase aligner asserts the lock signal and is using this phase from now on
- Block behaves as lpGBT ePort-Rx

Encoding the data
- The lpGBTlink-TX is ported directly from the lpGBT project (lpgbt.web.cern.ch)
- lpGBTlink-TX is collecting deserialized data from 24 transmisison links at once (after phase alignment)
- Data is encoded in the following manner:
  - To reduce transmission errors that appear due to noise, intersymbol interference or single event upsets the data volume is increased by the addition of parity bits with a Forward Error Correction (FEC) technique
  - Scrambling is used to keep the high density of transitions in the serial bit stream
  - Interleaving is used to increase the error correction capability
- GBTlink-TX has also a pseudo-random bit generator for testing the communication with the off-chip domain

Serializing data for off-chip transmission
- After encoding, data is serialized at 5.12 Gb/s rate and sent off-chip by a Giga Wire Transfer - Power Supply Immune (GWT-PSI) serializer
- There are 6 serializers in total (1 for 24 transmission links) to enable transmission from all 144 on-chip links
- GWT-PSI has a dual port FIFO for clock domain crossing
- Each GWT-PSI is a self-contained macrocell that has an internall phase-locked loop and delay-locked loop to generate all clock frequencies required by serialization process



POWER CONSUMPTION OF THE LEC

- Available power consumption of the left endcap is limited to 400 mW
- The components required for data transmission take up to 300 mW
- The remaining 100 mW is reserved for control and clock generation components: clock manager, slow control and powering control

Power [mW]	6 x	GWT-PSI	180
	6 x	GBT-TX	26.4
	6 x	DataAggr	90
		Headroom	103.6

References
ALICE ITS3: a bent stitched MAPS-based vertex detector by **Ola Slettevoll Groettvik**
Model and analysis of the data readout architecture for the ITS3 ALICE Inner Tracker System by **Manuel Vigueira Rodriguez**
Prototype of a 10.24Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector by **Arseniy Vitkovskiy**
Prototype measurement results in a 65nm technology and TCAD simulations towards more radiation tolerant monolithic pixel sensors by **Corentin Lemoine**