Contribution ID: **124** Type: **Poster**

FastRICH: a readout ASIC with precise time stamping for the LHCb RICH detector

Thursday 5 October 2023 18:40 (20 minutes)

The FastRICH is a readout chip designed by CERN and the University of Barcelona for the LS3 enhancements and the Upgrade II of the LHCb RICH detector. The 16-channel radiation-hard FastRICH will be capable of reading out MAPMTs, MCPs, and SiPMs, with peak hit rates up to 40MHz. The low-power readout, with 4 lpGBT/VTRx-compatible 1.28GHz SLVS output links, is optimized for bandwidth reduction, allowed by the use of a Constant Fraction Discriminator for timewalk compensation, a programmable hardware shutter, and a custom readout protocol. Preliminary simulations show ˜7ps timing resolution, with a total power consumption of <10mW per channel.

Summary (500 words)

The FastRICH is a readout chip that is being designed in the framework of the upgrade of the LHCb RICH detector to be installed during the LHC LS3. As the arrival of the Cherenkov photons to the photodetectors in the system can be predicted highly accurately, a fast timestamp of the hit improves accordingly the signal-to-noise ratio, pattern recognition, and particle identification performance, which would be critical in the foreseen 10ˆ34cm-2s-1 luminosity and high detector occupancy resulting from multiple primary vertices.

FastRICH builds on the experience of the design of the FastIC ASIC, designed by CERN and the University of Barcelona: an 8-channel generic detector readout ASIC that provides accurate timestamping and linear energy measurements of detected particles, and that is currently under an extensive campaign of measurements in order to evaluate its performance under the foreseen LHCb RICH conditions, with average hit rates ranging from 0.1MHz to 12.5MHz/channel.

FastRICH contains 16 channels designed with radiation-hardened electronics. The analog circuit is based on the analog front end of FastIC and will be capable of reading out MAPMTs during LHC Run4. Additionally, the ASIC will be able to read out candidate detectors for operation in Run 5, such as SiPMs and MCP-based sensors, with peak single-photon hit rates of up to 40MHz/channel. The FastRICH analog channel includes a Constant Fraction Discriminator to compensate for timewalk, which eliminates the need for off-chip post-processing, and consequently of measuring and sending out the energy information of the signals. Preliminary simulation results including the front-end and CFD circuit show an electronics jitter <40 ps rms for detector signals above 50uA, with a CFD residual timewalk of <150ps peak-to-peak for signals over the full 30uA-2mA range, which gets significantly reduced for signals over a smaller range.

The Time-of-Arrival (ToA) of incident photons will be measured with a ˜25ps time bin Time-to-Digital Converter (TDC), which can be programmed in a ˜50ps time bin mode. In normal operation, FastRICH will send only timewalk-corrected ToA information. A special mode with the leading-edge comparator ToA and high-resolution Time-over-Threshold (ToT) will also be supported, in order to debug and characterize the system performance.

Out-of-time background and sensor noise are filtered by a programmable hardware shutter, which allows selecting the signals of interest in a timing window that is foreseen to be in the order of a few ns per Bunch Crossing (BX), thus reducing the output data bandwidth. Data at a given BX is zero-suppressed and encoded in variable-length packets, which will in turn be transmitted by lpGBT/VTRx-compatible SLVS output links, which provide the chip a total maximum output bandwidth of up to 5.12Gbps. A framing protocol ensures DC

balancing and link self-recovery in case of readout errors. The number of active output links is configurable so that the chip can be optimized to operate in regions in the experiment with different occupancy.

The purpose of this presentation is to present a detailed description of the FastRICH chip architecture, design status, and expected performance.

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Session Classification: Thursday posters session

Track Classification: ASIC