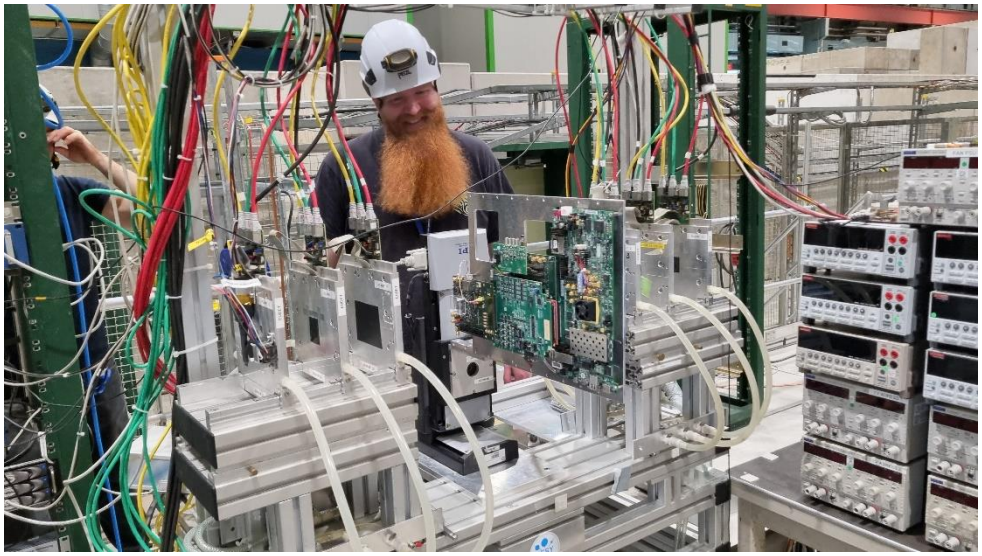
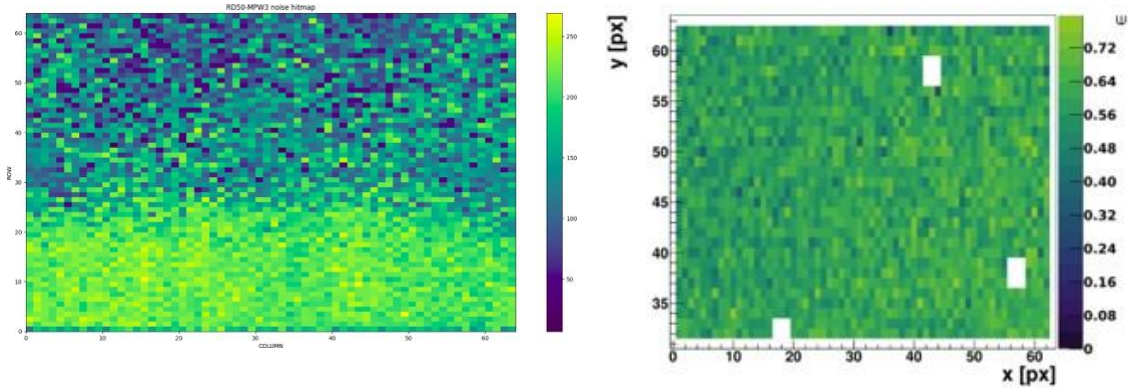


Fig. 1 RD50-MPW3 prototype in the Mimosa-26 telescope at the CERN 2022 test beam.



(a) **(b)**

Fig. 2 RD50-MPW3 noise hit map with a threshold voltage of 300 mV above the baseline voltage and a measuring time of 2 s (a), and efficiency measured at the CERN test beam (b).

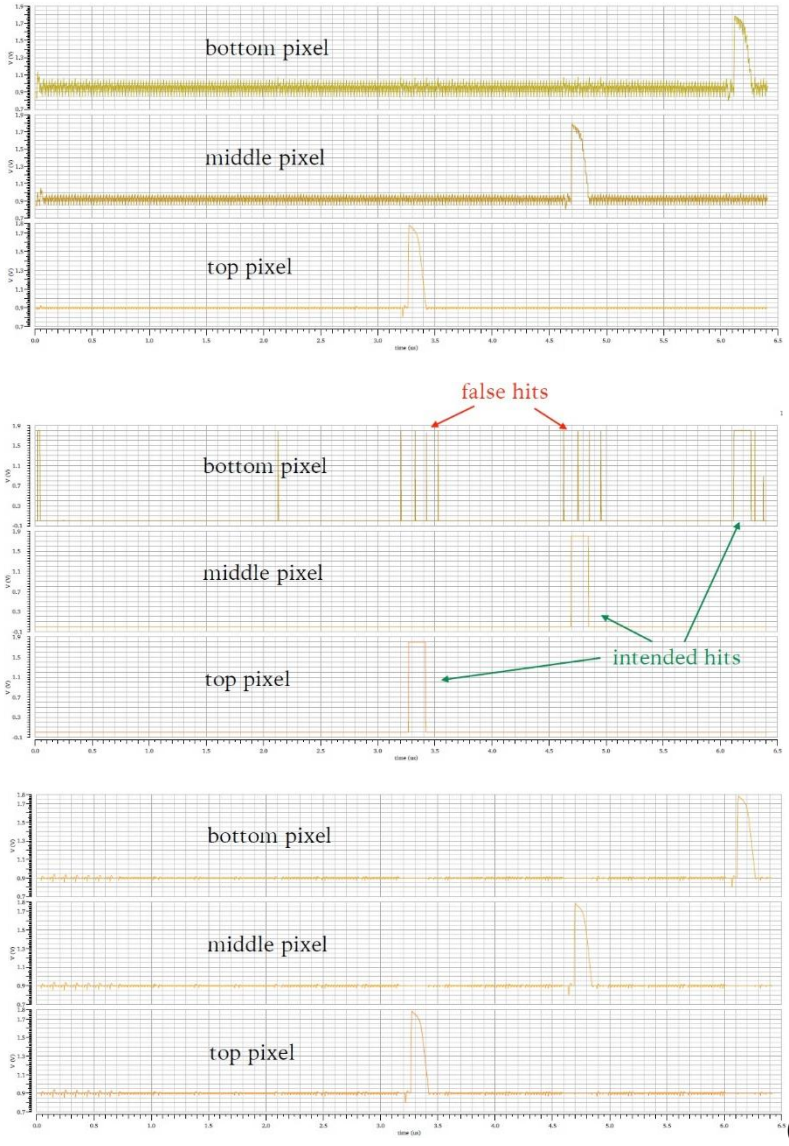


Fig. 3 Post-layout simulations of the amplifier (a) and comparator (b) for several pixels and part of the digital periphery when having joint digital in-pixel and digital peripheral power and ground domains, and of the amplifier (c) when having separate power and ground domains.

Table 1 Main design details and performance parameters of the RD50-MPW pixel chips. [(1)]Half of the chip has a pixel matrix for applications beyond physics; [(2)]anticipated values for RD50-MPW4.

Parameter	RD50-MPW1	RD50-MPW2	RD50-MPW3	RD50-MPW4
Device size [mm x mm]	5 x 5[(1)]	3.2 x 2.1	5.1 x 6.6	5.4 x 6.3
Pixel matrix size	40 x 78	8 x 8	64 x 64	64 x 64
Pixel size [µm x µm]	50 x 50	60 x 60	62 x 62	62 x 62
P-n spacing [µm]	3	8	8	8
In-pixel electronics	Analogue Digital	Analogue	Analogue Digital	Analogue Digital
Output data	Pixel address Time-stamp	Binary	Pixel address Time-stamp	Pixel address Time-stamp
Digital periphery	78 EOCs 2 LVDs lines	8 EOCs	32 EOCs, with 32-events 24-bit FIFOs 128-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line	32 EOCs, with 16-events 24-bit FIFOs 64-events 32-bit TX FIFOs I2C Wishbone bus 1 LVDs line
Chip guard ring frame	None	1 n-ring 6 p-rings	1 n-ring 6 p-rings	1 n-ring 5 n-/p-rings
Substrate biasing	Through p-stop contacts	Through p-stop contacts	Through p-stop contacts	Through chip edge or backside
Substrate resistivity [kΩ·cm]	0.5 – 1.1 1.9	Standard 0.2 – 0.5 1.9 3	Standard 1.9 3	Standard 3
Device thickness [µm]	280	280	280	280
V_{BD} [V]	56	120	120	> 400[(2)]
I_{LEAK} [µA/pixel]	1	1E-4	1E-6	1E-6[(2)]
Depletion depth [µm]	118	110	Not tested	Fully depleted[(2)]
ENC [mV]	50	2	< 140, > 50	50[(2)]
Efficiency [%]	Not tested	Not tested	60	> 99[(2)]