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RD50-MPW: A monolithic High Voltage CMOS pixel chip with high granularity and high radiation tolerance

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This contribution presents results from the RD50-MPW family of monolithic High Voltage CMOS (HV-CMOS) pixel chips, which are developed by the CERN-RD50 collaboration to study this technology in view of the harsh requirements imposed by future hadron colliders on tracking systems. Parameters especially considered in this programme are radiation tolerance, time resolution and granularity. This contribution reviews the design of RD50-MPW3, and presents its laboratory and test beam results. It also presents the design details of the latest prototype, RD50-MPW4. The prototypes developed so far are in the 150 nm High Voltage-CMOS (HV-CMOS) process from LFoundry S.r.l.

Summary (500 words)

RD50-MPW3 has a 64 rows x 64 columns matrix of 62 µm x 62 µm pixels with both analogue and column drain digital readout electronics embedded inside the large collection electrode. The pixel electronics also include logic to mask noisy pixels and an 8-bit SRAM shift register for serial configuration. RD50-MPW3 implements a double column scheme, which together with the 8-bit SRAM shift register, alleviates the routing congestion and facilitates means to minimise the crosstalk. This prototype has an advanced digital periphery for effective pixel configuration and fast data transmission, which consists of one EOC circuit per double column and a slow control system based on the I2C protocol for external communication using an internal Wishbone bus. The event data generated by the pixels is packed into frames, zero suppressed and encoded following the 8b/10b Aurora protocol. It is serialised over a single 640 Mb/s LVDS line.

We have evaluated RD50-MPW3 in the laboratory and also with particle beams at CERN SPS and MedAustron in Vienna, Austria (see figure 1). Electrical tests in the laboratory confirmed the functionality of the pixels and digital periphery, however the noise level was found to be too high especially for those pixels that are near the digital periphery. This forced us to increase the threshold voltage to 300 mV above the baseline voltage, which limits the efficiency of the sensor. The main goals of the test beams were to integrate RD50-MPW3 and its DAQ (i.e. chip carrier board, CaR board and Xilinx ZC706 evaluation board) into a reference system while enabling synchronisation between the chip and the reference with an AIDA2020 Trigger Logic Unit (TLU), and evaluate the chip with a particle beam. The average efficiency of the sensor, measured to be 60%, is low due to the high threshold voltage (see figure 2). We will evaluate RD50-MPW3 with a particle beam at DESY in July 2023, before and after irradiation to high fluence. Masking noisy pixels is a potential solution being currently explored to reduce the threshold voltage, and therefore improve the average efficiency at the price of reducing the sensitive area.

RD50-MPW4 essentially implements solutions to achieve a much higher breakdown voltage (> 400 V) and reduce the noise across the pixels of the matrix (< 50 mV), while maintaining the high granularity of 62 µm x 62 µm pixels. Unlike its predecessors, RD50-MPW4 uses floating p-stop style pixel-to-pixel isolation and has an optimised multi-guard ring chip frame. RD50-MPW4 implements topside edge biasing, and we will add backside biasing as a post-processing step on a subset of the fabricated samples. Unlike RD50-MPW3, the pixel matrix and peripheral readout use separate power and ground domains in RD50-MPW4. We expect this will allow us to reduce the threshold voltage and therefore increase the average efficiency across the whole

chip, as post-layout simulations have shown the noise is low and there are no fake events (see figure 3). Table 1 summarises the main design details and performance parameters of the RD50-MPW pixel chips.

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