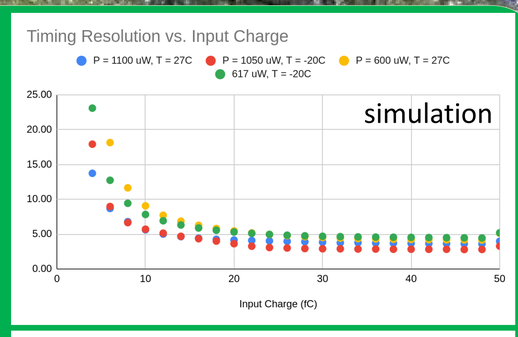
AS-ROC: SiGe integrated chip readout for fast timing

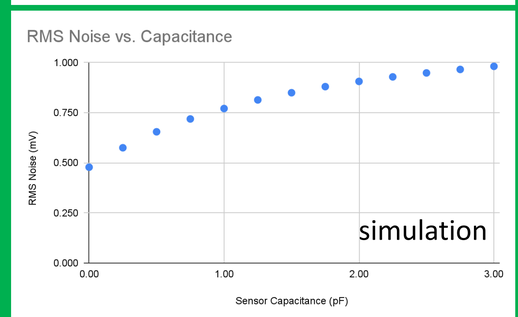
S.M. Mazza (simazza@ucsc.edu), J. Ott, (jeott@ucsc.edu), J. DeWitt, M. Gignac,
H. Sadrozinski, B. Schumm, A. Seiden, T. Shin, N. Nagel, M. Wilder. *SCIPP, U.C. Santa Cruz*
Z. Galloway, G. Saffier-Ewing. *Anadyne Inc.*

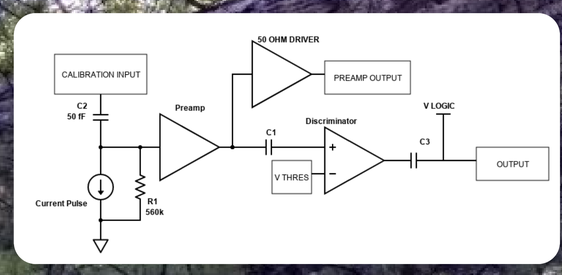
TWEPP 2023 Sardinia (Italy)

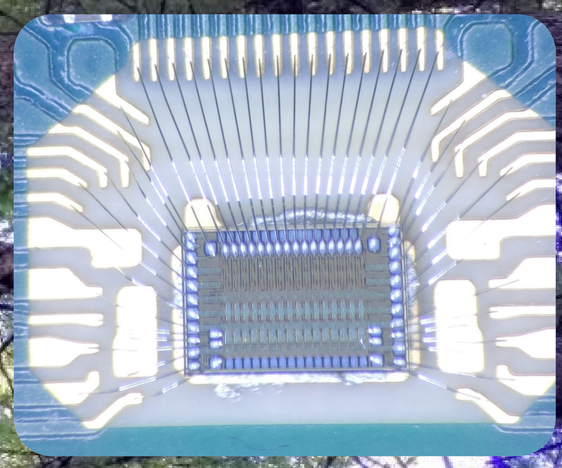
Introduction and Simulation

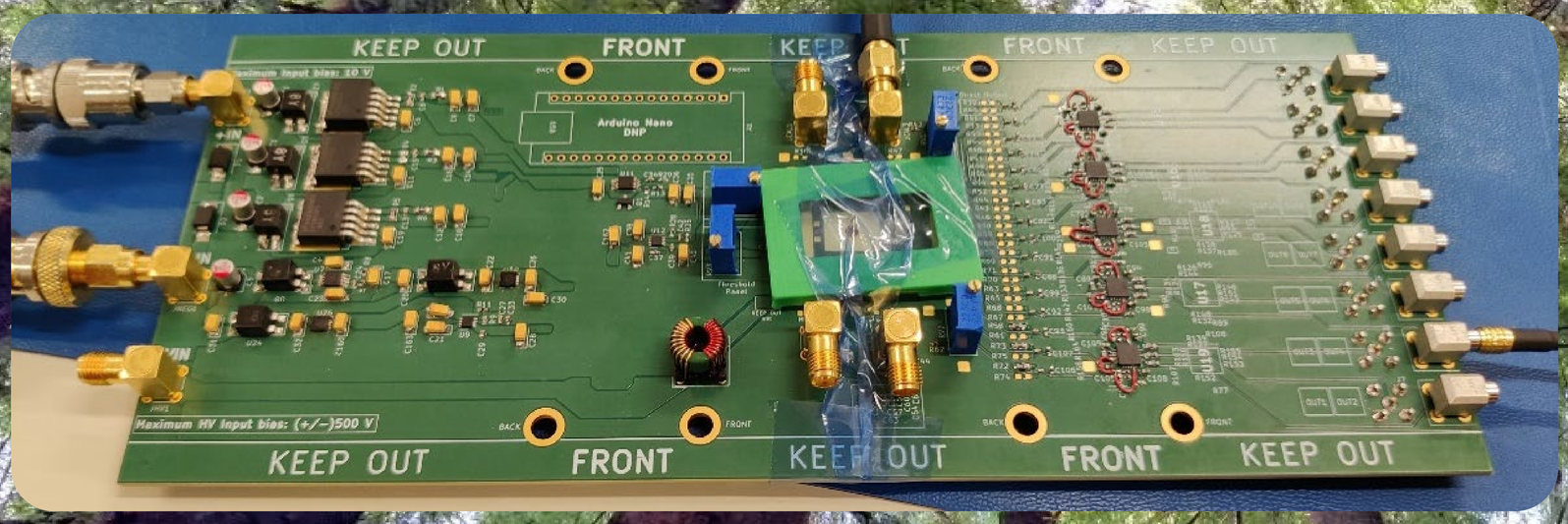
- Chip developed with a collaboration of SCIPP and Anadyne Inc.
  - Using Tower Semiconductors SiGe BiCMOS technology
- Goal: readout of AC-LGADs, aimed at the EPIC detector (Electron-ion collider)
  - **Low power consumption** (<1mW/ch)
  - Low jitter, fast rise time → **picosecond time resolution**
  - Both analog and discriminator output
- **Expected jitter <10ps** from simulation
- Two version of the chip: low and high power (low power version presented)
  - Designed for low input capacitance (100s of fF)
  - High power version should drain twice the power but have a better gain and rise time









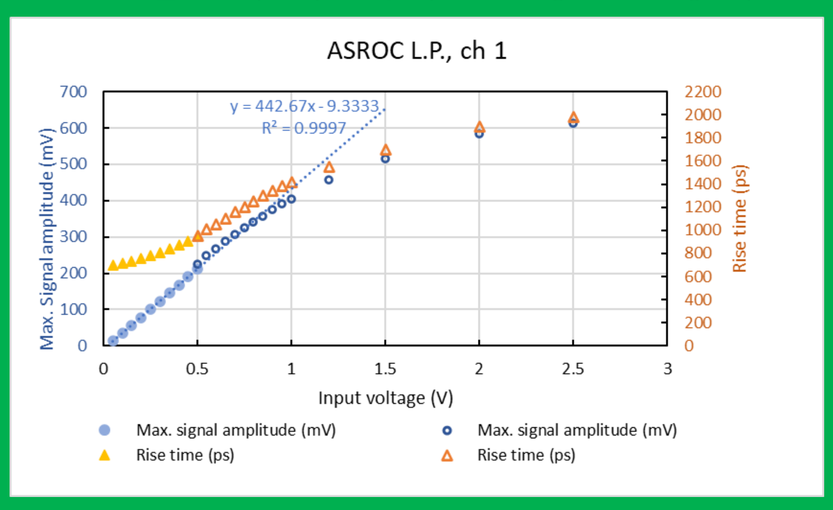


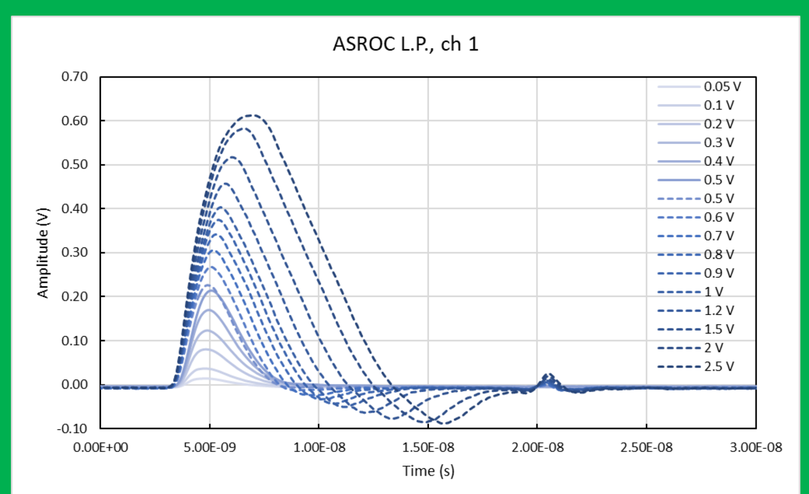
Discriminator performance

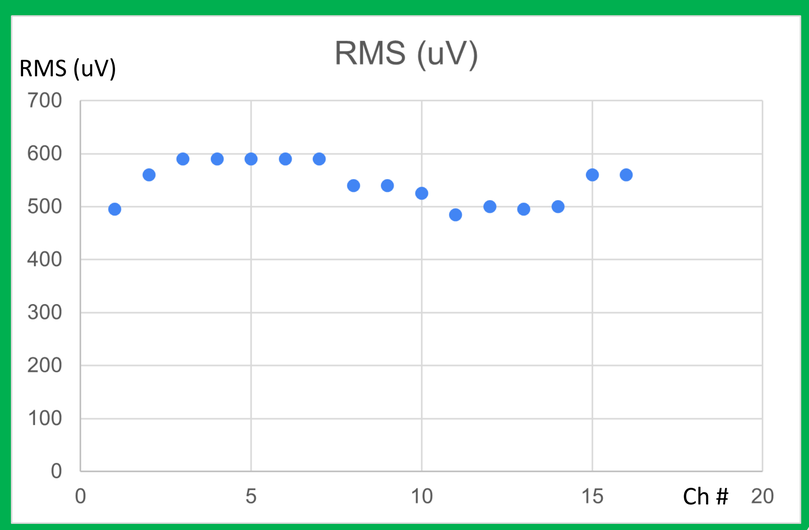
- Discriminator output is an adjustable (1.5V in the tests) step function with rise time < 1 ns
- Discriminator Jitter < 10 ps
- Discriminator level can be adjusted with external reference
- Width of the discriminator output is proportional to the pulse maximum
  - Can be used to correct arrival time for time walk

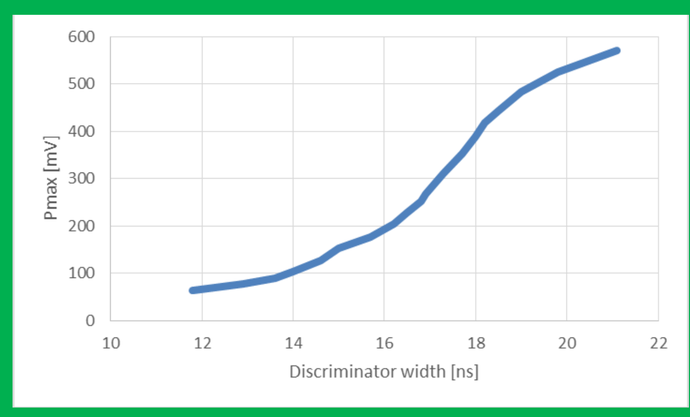
Pre-amplifier performance

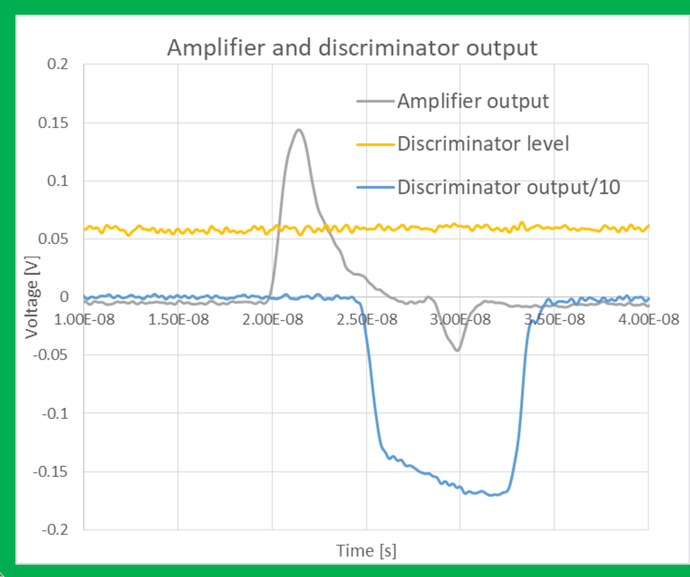
- RMS noise of unloaded chip around 500-600uV, similar for all channels (2.5 GHz bandwidth)
- Test the chip with square pulse input to a 50 fF calibration capacitor
- 50 mV input correspond to ~2 fC of collected charge
- Good pulse shape, minimal undershoot for most of the dynamic range
- Rise time ranging from 700ps to ~2ns (for large charge injection)
- Pulse duration of a few ns
- Linear behavior up to 400 mV
- Stable behavior across all 16 channels
- Jitter = rise_time/(S/N) ~10ps (assuming 50mV signal)

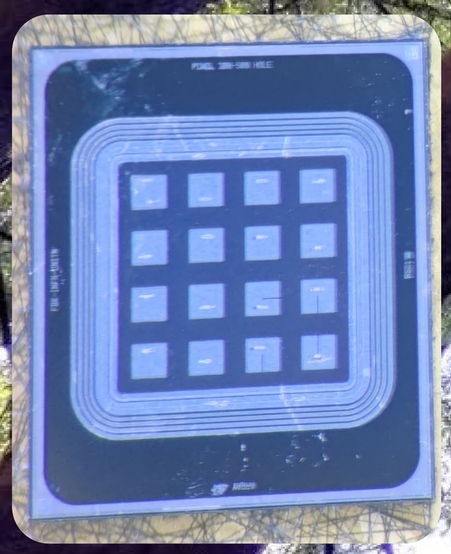








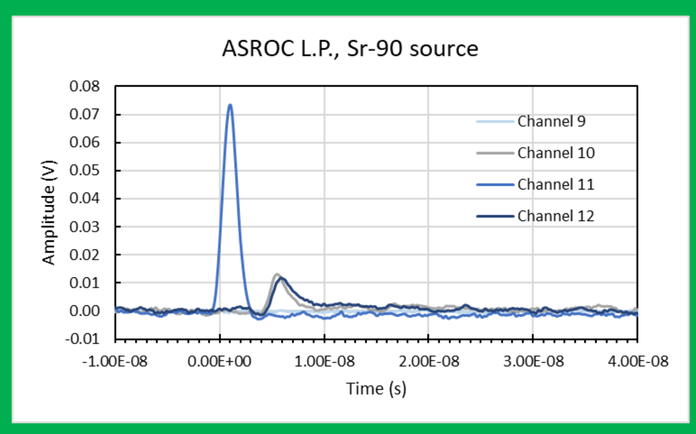




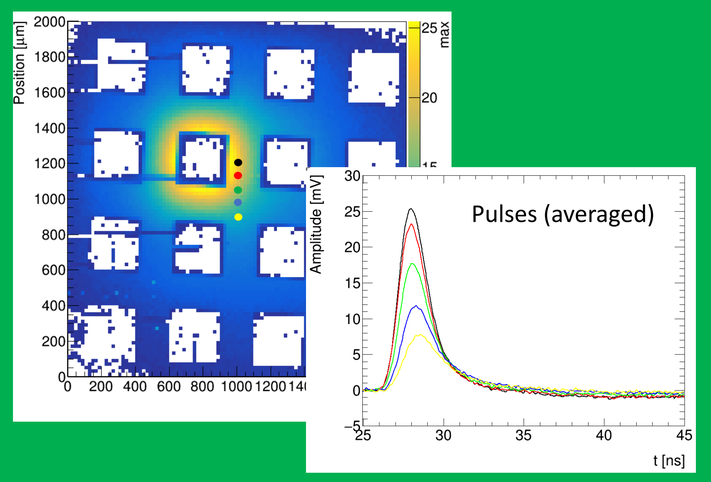
Performance with sensor

- Connected to a pad AC-LGAD (from FBK RSD1 production)
  - 500 um pitch, 300x300 um pads
- Noise level ~700 uV for input capacitance of 500 fF
- Tested with Sr90 beta source and TCT IR laser
- Very good S/N with sensor response
  - Observed AC-LGAD charge sharing

Single event Sr90



Laser TCT scan



Work supported by DoE SBIR program, grant DE-SC0021800