Contribution ID: **67** Type: **Poster**

SiGe integrated chip readout for fast timing

Thursday 5 October 2023 18:40 (20 minutes)

Advances in timing detector technology require new specialized readout electronics. Applications demand high rep rates, below 10 ps time of arrival resolution and, low power. A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with UC Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution (0.6 mW/channel, 10 ps of timing resolution for 8 fC). In this contribution the ASIC performance simulation and the results from the first prototype run will be shown.

Summary (500 words)

Advances in fast detector technology and the direction of HEP experiments and applications require the development of new specialized readout electronics. Experimental demands include some combination of high rep rates (order of ns dead time), below 10 ps time of arrival (TOA) resolution and low power (between 0.1 mW and 1 mW per channel. A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with University of California Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution, with 0.6 mW per channel (front end and discriminator) while retaining 10 ps of timing resolution for 8 fC of injected charge. Preamplifier output pulse and timing resolution vs charge and power dissipation are shown in Figure 1.

In the process some insight was developed into the challenges and potential performance of SiGe front end ASICs for future R&D effort. Channel matching to reduce calibration requirements and increase yield, timing resolution at the low end of the proposed detector dynamic range, and temperature stability were all considered during the design process to ensure the prototype performance would be deliverable in a full implementation. During this process we have developed some insight into the challenges and potential performance of SiGe front end ASICs if further R&D were undertaken. The developed single pre-amplifier stage and what is effectively a Time Over Threshold (TOT) discriminator topology is suitable for low repetition rate and quiescent power and sub 10 ps timing resolution applications. The TOT data is required to correct the TOA of pulses over the entire dynamic range of interest. These TOT discriminators are not literal TOT converters of the amplified analog input. The output pulse width of the discriminator is proportional to the input pulse height and have a dead time of up to 10 ns, an improved is necessary to increase the repetition rate capabilities. Some practical considerations for selecting a process for future R&D include the size and power efficiency of the CMOS transistors for the back-end electronics and diminishing performance gains of higher speed SiGe transistors. The currently available SiGe processes offer 130 nm CMOS at a minimum. Transistors faster than 25 GHz have little signal to noise or power improvements to offer when designing readout systems for signals in the 1-2 GHz regime ultra-fast silicon detectors operate in. Moving to faster and smaller SiGe transistors may only introduce unnecessary design challenges such as poor transistor matching, low breakdown voltages, higher Vbe, etc. The current prototype is designed in a 10 GHz process.

The chip production was submitted and will be ready by the end of May 2023, the chip schematic is shown in Fig. 2, Top. A readout board (Fig. 2, Bottom) was designed and will be submitted for production with the same time scale. In this contribution the simulated ASIC performance and the characterization of the first prototype will be shown.

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Session Classification: Thursday posters session

Track Classification: ASIC